Signetics
integrated circuits
1979

Bipolar and MOS memories

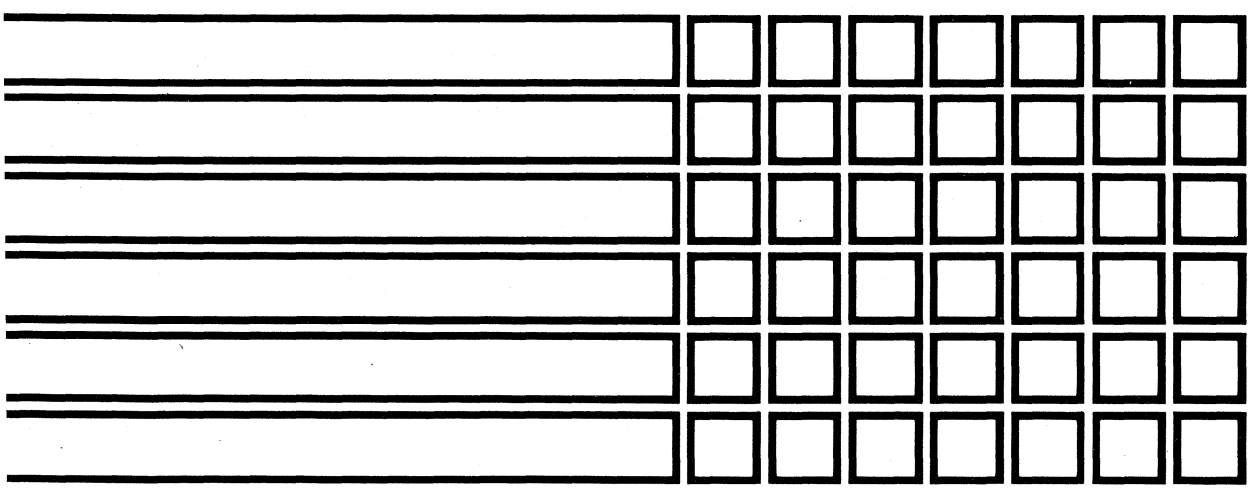
signetics

ERRATUM

On page 4 the last four lines of the Table of Contents should be replaced by the following:

SIGNETICS BIPOLAR & MOS MEMORY

DATA MANUAL



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INTRODUCTION

Rapid improvement in both the cost and performance of semiconductor memories has led to a dramatic increase in their usage in today's highly sophisticated electronic systems. Signetics has worked diligently over the last 15 years to develop the various technologies necessary to satisfy the broad range of users' semiconductor memory requirements. As a result, in 1979, Signetics is able to offer the broadest bipolar and MOS memory product lines available in the industry.

Signetics offers a complete line of bipolar Schottky RAMs, PROMs and other special memory products for high speed applications. These products are available with organizations ranging from 64 to 2304 bits for the RAM family and 256 to 16K bits for the PROM family. All Signetics' bipolar products are fabricated with double level metalization for maximum packaging density and low cost. PROM fuses are constructed with nichrome links for the highest reliability and programming yield in the industry. Signetics will continue to advance bipolar memory "state of the art" in 1979 with the introduction of our new low power Schottky and latched PROMs, 4K RAM and programmable array logic products.

The MOS memory standard product line spans the many diverse memory application requirements of today's industry. Signetics' dynamic RAMs offer high bit density coupled with low standby power, while our static RAM family offers speed and ease of use. Signetics' MOS 2600 series ROMs have a single +5V power supply and all industry standard pinouts are available.

The 1979 Signetics Memory Data Manual contains all necessary data on currently available products and those products which will be available in the future. In addition, the following pages provide product selection guides to aid the user in quickly selecting the optimum product for his particular system application.

Signetics reserves the right to make changes in the products contained in this book in order to improve design or performance and to supply the best possible products. Signetics also assumes no responsibilty for the use of any circuits described herein and makes no representations that they are free from patent infringement.

BIPOLAR MEMORY CROSS REFERENCE

AMD	SIGNETICS
2700/27LS00	82S16/LS116
2701/27LS01	82S17/LS117
27S02/3101A	3101A
54S289	82S25
27S08	82S23
27S09/ 27LS09	82S123
27S12	82S130
27S13	82S131
27S15	82S115
27S20	82S126
27S21	82S129
27S28	82S146
27S29	82S147
27S30	82S140
27S31	82S141
27S32	82S136
27S33	82S137
93415A	82S10
74S289	74S89
27S03/ 74S189	74S189

FAIRCHILD	SIGNETICS
10145A	10145
10410	10144
10415	10146
10416	10149
93403	82S25
93404	3101A
93405	74S189
93410	74S200/201
93411	82S17
93411A	82S117
93415/A	82S10/110
93417	82S126
93419	82S09
93421	82S16
93421A	82S116
93425	82S11
93425A	82S111
93427	82S129
93431	82S23
93436	82S130
93438	82S140
93446	82S131
93448	82S141
93452	82S136
93453	82S137
93L415	82LS10
93L425	82LS11
93477	82S208
93478	82S210
93479	82S212

NATIONAL	SIGNETICS
74S188	82S23
74S189	74S189
74S200	74S200/201
74S206	82S17
74S287	82S129
74S288	82S123
74S387	82S126
74S472	82S147
74S473	82S146
74S570	82S130
74S571	82S131
74S572	82S136
74S573	82S137
85S228	82S181
85S229	82S180
87S295	82S140
87S296	82S141
54S289	82S25

MMI	SIGNETICS
5560	82S25
6275	82S290
6276	82S291
6300-1	82S126
6301-1	82S129
6305-1	82S130
6306-1	82S131
6330	82S23
6331	82S123
6340-1	82S140
6341-1	82S141
6348	82S146
6349	82S147
6352-1	82S136
6353-1	82S137
6380	82S180
6381	82S181
6530	82S17
6531	82S16
6560	3101A
6561	74S189
H6555	82S09

INTEL	SIGNETICS
3101	82S25
3101A	3101A
3106/A	82S16/116
3107/A	82S17/117
3601	82S126
3602	82S130
3604	82S140
3605	82S136
3608	82S180
3621	82S129
3622	82S131
3624	82S141
3625	82S137
3628	82S181

INTERSIL	SIGNETICS
5501	82S25
5523	74S201
5523A	82S16
5533	74S301
5533A	82S17
5600	82S23
5603A	82S126
5604	82S130
5605	82S140
5610	82S123
5623A	82S129
5624	82S131
5625	82S141
56S06	82S136
56S26	82S137

MOTOROLA	SIGNETICS
4064	82S25
4069	74S89
4256	82S16
5005	82S126
7640	82S140
7641	82S141
7642	82S136
7643	82S137
93415C	82S10
93425C	82S11
10139	10139
10144	10144
10149	10149

HARRIS	SIGNETICS
HM7602	82S23
HM7603	82S123
HM7610	82S126
HM7611	82S129
HM7620	82S130
HM7621	82S131
HM7625	82S114
HM7640	82S140
HM7641	82S141
HM7642	82S136
HM7643	82S137
HM7647	82S115
HM7648	82S146
HM7649	82S147
HM7680	82S180
HM7681	82S181
HM7680R	82S182
HM7681R	82S183
HM7684	82S184
HM7685	82S185

T.I.	SIGNETICS
54S289	82S25
74S188	82S23
74S189	74S189
74S200	74S200
74S201	74S201
74S287	82S129
74S288	82S123
74S289	3101A
74S301	74S301
74S387	82S126
74S472	82S147
74S473	82S146
74S474	82S141
74S475	82S140
74S476	82S137
74S477	82S136
74S478	82S181
74S479	82S180

Parts are pin for pin functional replacements except where noted. Signetics supplies most devices in both commercial and military temperature ranges.

BIPOLAR MEMORY SELECTION GUIDE

DEVICE	ORGANI-ZATION	OUTPUT CIRCUIT[1]	OUTPUT LOGIC[2]	ACCESS TIME [ns][4]	TEMPERATURE RANGE[3]	PACKAGE	NO. OF PINS	MAX. I_{CC} [mA][4]
CAMS								
10155	8X2	OE	—	13	C	F,N	18	140
SAMS								
82S12	8X4	OC	T	40	C	F,N	24	160
82S112	8X4	TS	T	40	C	F,N	24	160
RAMS								
82S25	16X4	OC	B	50	M,C	F,N	16	105
3101A	16X4	OC	B	35	M,C	F,N	16	105
54/74S89	16X4	OC	T	50	M,C	F,N	16	105
54/74S189	16X4	TS	B	35	M,C	F,N	16	110
82S21	32X2	OC	T	50	C	F,N	16	130
82S16	256X1	TS	T	50	M,C	F,N	16	115
82S116	256X1	TS	T	40	C	F,N	16	115
82LS116	256X1	TS	T	40	C	F,N	16	70
82S17	256X1	OC	T	50	M,C	F,N	16	115
82S117	256X1	OC	T	40	C	F,N	16	115
82LS117	256X1	OC	T	40	C	F,N	16	70
54/74S200	256X1	TS	B	50	M,C	F,N	16	130
54/74S201	256X1	TS	B	50	M,C	F,N	16	130
54/74S301	256X1	OC	B	50	M,C	F,N	16	130
82S09	64X9	OC	T	45	M,C	I,N	28	190
82S09A	64X9	OC	B	35	M,C	I,N	28	190
82S10	1024X1	OC	B	40	M,C	F,N	16	170
82S110	1024X1	OC	B	30	C	F,N	16	170
82S11	1024X1	TS	B	40	M,C	F,N	16	170
82S111	1024X1	TS	B	30	C	F,N	16	170
82LS10	1024X1	OC	B	45	M,C	F,N	16	65
82LS11	1024X1	TS	B	45	M,C	F,N	16	65
82S208*	256X8	TS	B	60	C	F	22	185
82S210*	256X9	TS	B	60	C	F,N	24	185
82S212*	256X9	TS	B	45	C	F	24	185
8X350*	256X8	TS	B	N/A	M,C	F	22	185
82S400*	4096X1	OC	B	45	C	I	18	155
82S401*	4096X1	TS	B	45	C	I	18	155
ROMS								
82S290	2048X8	OC	—	110	M,C	F,N	24	170
82S291	2048X8	TS	—	110	M,C	F,N	24	170

*To be announced

NOTES

1. Output circuit:
   OE = Open emitter
   OC = Open collector
   TS = 3-state
2. Output logic:
   T = Transparent—input data appears on output during Write
   B = Blanked—output is blanked during Write
3. Temperature range:
   C = Commercial (0°C to +75°C)
   M = Military (−55°C to +125°C)
   All ECL 10,000 series (−30°C to +85°C)
4. Commercial (0°C to +75°C)

BIPOLAR MEMORY SELECTION GUIDE (cont'd)

DEVICE	ORGANI-ZATION	OUTPUT CIRCUIT[1]	OUTPUT LOGIC[2]	ACCESS TIME [ns][4]	TEMPERATURE RANGE[3]	PACKAGE	NO. OF PINS	MAX. I_{CC} (mA)[4]	EQUIVA-LENT ROM
PROMS									
82S23	32X8	OC	—	50	M,C	F,N	16	77	—
82S123	32X8	TS	—	50	M,C	F,N	16	77	—
10139	32X8	OE	—	20	C	F	16	145	—
82S27	256X4	OC	—	40	C	F	16	140	—
82S126	256X4	OC	—	50	M,C	F,N	16	120	—
82S129	256X4	TS	—	50	M,C	F,N	16	120	—
10149	256X4	OE	—	20	C	F	16	150	—
82S114	256X8	TS	—	60	M,C	F,N	24	175	—
82S130	512X4	OC	—	50	M,C	F,N	16	140	—
82S131	512X4	TS	—	50	M,C	F,N	16	140	—
82S115	512X8	TS	—	60	M,C	F,N	24	175	—
82S140	512X8	OC	—	60	M,C	F,N	24	175	—
82S141	512X8	TS	—	60	M,C	F,N	24	175	—
82S146	512X8	OC	—	45	C	F,N	20	155	—
82S147	512X8	TS	—	45	C	F,N	20	155	—
82S136	1024X4	OC	—	60	M,C	F,N	18	140	—
82S136A	1024X4	OC	—	45	M,C	F,N	18	140	—
82S137	1024X4	TS	—	60	M,C	F,N	18	140	—
92S137A	1024X4	TS	—	45	M,C	F,N	18	140	—
82LS180	1024X8	OC	—	175	M,C	F,N	24	80	—
82LS181	1024X8	TS	—	175	M,C	F,N	24	80	—
82S180	1024X8	OC	—	70	M,C	F,N	24	175	—
82S181	1024X8	TS	—	70	M,C	F,N	24	175	—
82S182	1024X8	OC	—	60	M,C	F,N	24	175	—
82S183	1024X8	TS	—	60	M,C	F,N	24	175	—
82S2708	1024X8	TS	—	225	M	F	24	85	—
82S184	2048X4	OC	—	100	M,C	I,N	18	120	—
82S185	2048X4	TS	—	100	M,C	I,N	18	120	—
82S190	2048X8	OC	—	80	M,C	I,N	24	175	82S290
82S191	2048X8	TS	—	80	M,C	I,N	24	175	82S291
FPLAS									
82S100	16X48X8	TS	—	50	M,C	F,I,N	28	170	—
82S101	16X48X8	OC	—	50	M,C	F,I,N	28	170	—
82S106	16X48X8	OC	—	70	M,C	F,I,N	28	170	—
82S107	16X48X8	TS	—	70	M,C	F,I,N	28	170	—
PLAS									
82S200	16X48X8	TS	—	50	M,C	F,I,N	28	170	—
82S201	16X48X8	OC	—	50	M,C	F,I,N	28	170	—
FPGAS									
82S102	16X9	OC	—	35	M,C	F,I,N	28	170	—
82S103	16X9	TS	—	35	M,C	F,I,N	28	170	—
FPLS									
82S104	16X48X8	OC	—	90	M,C	F,I,N	28	170	—
82S105	16X48X8	TS	—	90	M,C	F,I,N	28	170	—

*To be announced

NOTES

1. Output circuit:
   OE = Open emitter
   OC = Open collector
   TS = 3-state
2. Output logic:
   T = Transparent—input data appears on output during Write
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3. Temperature range:
   C = Commercial (0°C to +75°C)
   M = Military (−55°C to +125°C)
   All ECL 10,000 series (−30°C to +85°C)
4. Commercial (0°C to +75°C)

MOS MEMORY CROSS REFERENCE

	SIGNETICS		
	RAMs	ROMs	CHARACTER GENERATORS
AMD			
AM9216		2617	
AM9218/8316E		2616	
AM9208		2608	
AMI			
6830		2608	
EA			
2308/8308		2608	
4600		2600	
FAIRCHILD			
F16K	2690		
4027	4027		
GI			
9316A/B		2616	
INTEL			
2104A	4027		
2114	2614		
2308		2607	
2316E		2616	
2141	2613		
2117	2690		
INTERSIL			
IM7114	2614		
IM7141	2613		
IM4027	4027		
IM7116	2690		
MOSTEK			
MK4027	4027		
MK4116	2690		
MK30000		2607	
MK34000		2616	
MK32000		2632	
MK36000		2664*	
MOTOROLA			
6605A	4027		
6830		2608	
6570			2609
6616	2690		
NATIONAL			
MM5290	2690		
TI			
TMS4027	4027		
TMS4116	2690		
TMS4700		2607	
TMS4044	2613		
TMS4045	2614		

MOS MEMORY SELECTION GUIDE

DEVICE	ORGANIZATION	OUTPUT CIRCUIT[1]	ACCESS/CYCLE TIME (ns)	TEMPERATURE RANGE[2]	PACKAGE	NO. OF PINS	CLOCK/CE/TTL COMPATABILITY	POWER SUPPLIES (V)
RAMS								
Static								
2613-15	4096X1	TS	150/150	C	F, I, N	18	Yes	+5, Gnd
2613-20	4096X1	TS	200/200	C	F, I, N	18	Yes	+5, Gnd
2613-25	4096X1	TS	250/250	C	F, I, N	18	Yes	+5, Gnd
2613-45	4096X1	TS	450/450	C	F, I, N	18	Yes	+5, Gnd
2614-15	1024X4	TS	150/150	C	F, I, N	18	Yes	+5, Gnd
2614-20	1024X4	TS	200/200	C	F, I, N	18	Yes	+5, Gnd
2614-25	1024X4	TS	250/250	C	F, I, N	18	Yes	+5, Gnd
2614-45	1024X4	TS	450/450	C	F, I, N	18	Yes	+5, Gnd
Dynamic								
4027-2	4096X1	TS	150/320	C	F, I, N	16	Yes	+12, ±5, Gnd
4027-3	4096X1	TS	200/200	C	F, I, N	16	Yes	+12, ±5, Gnd
4027-4	4096X1	TS	250/250	C	F, I, N	16	Yes	+12, ±5, Gnd
2690-2	16,384X1	TS	150/375	C	F, I, N	16	Yes	+12, ±5, Gnd
2690-3	16,384X1	TS	200/375	C	F, I, N	16	Yes	+12, ±5, Gnd
2690-4	16,384X1	TS	250/410	C	F, I, N	16	Yes	+12, ±5, Gnd
ROMS								
Static								
2607	1024X8	TS	500/500	C	F, I, N	24	Yes	+5, Gnd
2608	1024X8	TS	550/550	C	F, I, N	24	Yes	+5, Gnd
2608-1	1024X8	TS	450/450	C	F, I, N	24	Yes	+5, Gnd
2600	2048X8	TS	500/500	C	F, I, N	24	Yes	+5, Gnd
2600-1	2048X8	TS	300/300	C	F, I, N	24	Yes	+5, Gnd
2616	2048X8	TS	450	C	F, I, N	24	Yes	+5, Gnd
2616-1	2048X8	TS	350	C	F, I, N	24	Yes	+5, Gnd
2617	2048X8	TS	450	C	F, I, N	24	Yes	+5, Gnd
2617-1	2048X8	TS	350	C	F, I, N	24	Yes	+5, Gnd
2632	4096X8	TS	450/450	C	I, N	24	Yes	+5, Gnd
2664*	8192X8	TS	450/450	C	I, N	24	Yes	+5, Gnd

STANDARD ROM CODE

DEVICE	CODE NO.	DESCRIPTION
STATIC ROM		
2608	CN0000	10X7 Upper and Lower Case ASCII Character Generator
CHARACTER GENERATOR		
2609	CN6571	128 ASCII Characters in 7X9 Matrix Count Down
	CN6571A	128 ASCII Characters in 7X9 Matrix Count Up
	CN6575	128 ASCII Characters in 7X9 Matrix Count Up with Special Characters

*To be announced

NOTES

1. Output circuit:
   TS = 3-state
   OD = Open drain
   BD = Bare drain
   PD = Pull down
   PP = Push-pull
2. Temperature range:
   C = Commercial (0°C to +75°C)
   M = Military (−55°C to +125°C)

BIPOLAR MEMORY DATA SPECIFICATIONS

signetics

DESCRIPTION

The 10155 is a 16-bit ECL Content Addressable Memory (CAM) organized as an array of 8 words by 2 bits. Each cell of the array consists of a D-type latch and an exclusive-OR comparator, along with control logic for reading, writing and masking.

The modes of operation possible with the 10155 are associate, masked associate, read, write, and hybrid. Lines Y_0-Y_7 are used for linear word select in the read/write mode, and are used as outputs for match/mismatch information in the associate mode.

In associate operation, I_0 and I_1contain information to be compared. If the latches at a particular Y location are in a state matching the input data, that Y line goes low.

The Y outputs are open emitters, allowing expansion in multiples of 2 bits by tying additional 10155's to the Y bus lines. To inhibit comparison of a particular bit, the corresponding A_0 or A_1 line is held low.

In the read mode, the state of the selected cells appears on outputs D_0 and D_1. In the write mode, these outputs are transparent, following the state of I_0 and I_1.

In Hybrid mode, one of the I_0 or I_1 data inputs may be associated with the Q_{n0} or Q_{n1} cells respectively. If a match exists, the corresponding Y_n line(s) will go low, and can be used to address the other half of the memory for writing new data. Thus, it is possible to write I_1 in Q_{n1} where I_0 matches Q_{n0} or vice versa.

FEATURES

- **12ns associate time (max.)**
- **Linear address select**
- **Single bit masking**
- **50 Ω output drive**
- **ECL 10K compatible**
- **Open emitter match lines for easy bit expansion**
- **50k Ω input pulldown resistors (except on Y lines)**

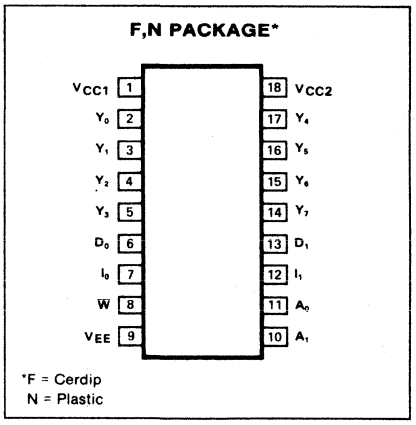
APPLICATION

- **Content addressable memory systems**

RECOMMENDED OPERATING VOLTAGES

- $V_{CC1} = V_{CC2} = 0V$
- $V_{EE} = -5.2V \pm 5\%$

PIN CONFIGURATION



*F = Cerdip
N = Plastic

TRUTH TABLE (POSITIVE LOGIC)

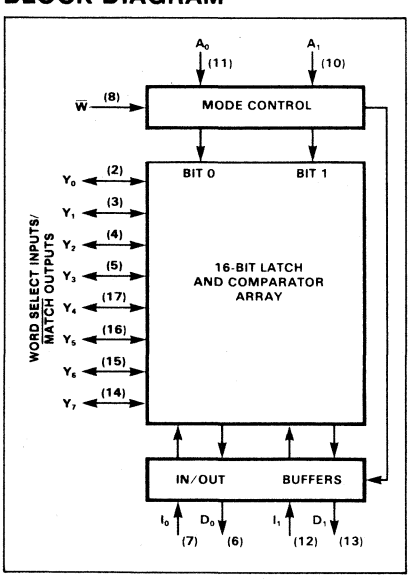
MODE	A_0	A_1	I_0	I_1	$\overline{W}$	D_0	D_1	Q_{n0}	Q_{n1}	Y_n
Associate[1]	1	1	1/0	1/0	X	0	0	Q_{n0}	Q_{n1}	$Q_{n0} \oplus I_0 + Q_{n1} \oplus I_1$
Associate[1,2] (masked)	1	0	1/0	X	1	0	D_1	Q_{n0}	Q_{n1}	$Q_{n0} \oplus I_0$
Associate[1,2] (masked)	0	1	X	1/0	1	D_0	0	Q_{n0}	Q_{n1}	$Q_{n1} \oplus I_1$
Read[3]	0	0	X	X	1	D_0[2]	D_1[2]	Q_{n0}	Q_{n1}	0 (Selected address)
Write[3,4]	0	0	1/0	1/0	0	I_0	I_1	I_0	I_1	0 (Selected address)
Hybrid[5]	1	0	1/0	1/0	0	0	I_1	Q_{n0}	$I_1 \bullet \overline{Y_n}$	$Q_{n0} \oplus I_0$
Hybrid[5]	0	1	1/0	1/0	0	I_1	0	$I_0 \bullet \overline{Y_n}$	Q_{n1}	$Q_{n1} \oplus I_1$

X = Don't care
Q_{n0} = Contents of address n, Bit 0 (n = 0 to 7)
Q_{n1} = Contents of address n, Bit 1

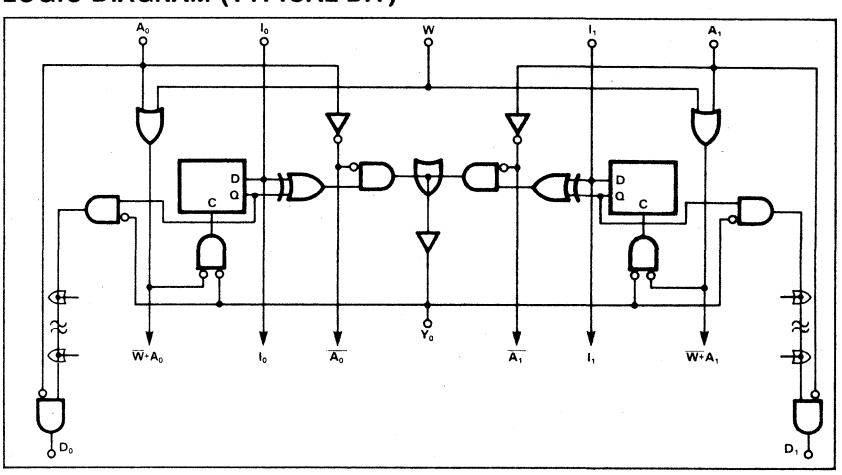
NOTES

1. 1 (high) = Mismatch, 0 (low) = Match
2. Read mode: $D_0 = Q_{00} \bullet \overline{Y_0} + Q_{10} \bullet \overline{Y_1} + \bullet \bullet \bullet + Q_{70} \bullet \overline{Y_7}$
   $D_1 = Q_{01} \bullet \overline{Y_0} + Q_{11} \bullet \overline{Y_1} \bullet \bullet \bullet + Q_{71} \bullet \overline{Y_7}$
3. In normal operation a single Y address is selected for read or write
4. Write is transparent
5. Simultaneous Associate and Write at all "Match" addresses.

BLOCK DIAGRAM



LOGIC DIAGRAM (TYPICAL BIT)



ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2} = 0V$

PARAMETER		RATING	UNIT
V_{EE}	Supply voltage	-8	Vdc
V_{IN}	Input voltage	0 to V_{EE}	Vdc
I_O	Output source current	40	mAdc
	Temperature Range		°C
T_A	Operating	-30 to +85	
T_J	Operating junction	125	
T_{STG}	Storage	-55 to +125	

DC ELECTRICAL CHARACTERISTICS[1] $V_{CC1} = V_{CC2} = 0V$, $V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2V$

PARAMETER		TEST CONDITIONS	-30 °C			+25 °C			+85 °C			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Input voltage											V
V_{IL}	Low		-1.890			-1.850			-1.825			
V_{IH}	High				-0.890			-0.810			-0.700	
V_{ILA}	Low threshold				-1.500			-1.475			-1.440	
V_{IHA}	High threshold		-1.205			-1.105			-1.035			
	Output voltage											V
V_{OL}	Low	V_{IH} = Max, V_{IL} = Min	-1.89		-1.675	-1.65	-1.70	-1.85	-1.825		-1.615	
V_{OH}	High		-1.06		-0.89	-0.96	-0.89	-0.81	-0.89		-0.70	
V_{OLA}	Low threshold				-1.655			-1.63			-1.595	
V_{OHA}	High threshold	V_{IHA} = Min, V_{ILA} = Max	-1.08			-0.98			-0.91			
	Input current											μA
I_{IL}	Low	A,I,W = V_{IL} Min				0.5						
I_{IH}	High	A = V_{IH} Max						220				
		I,W = V_{IH} Max						200				
		Y = V_{IH} Max						50				
I_{EE}	Supply current	V_{IH} Max					115	140				mA

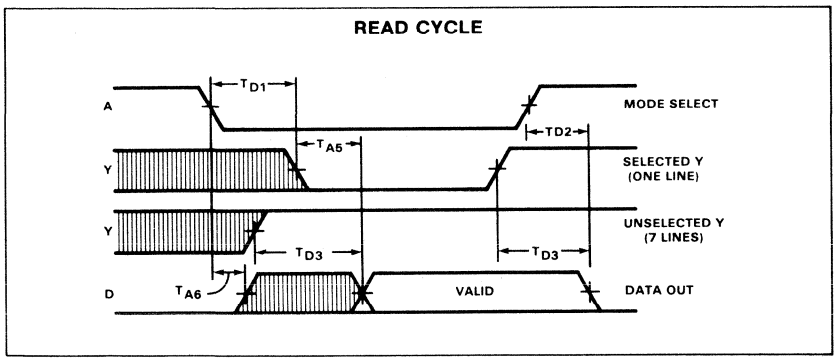
AC ELECTRICAL CHARACTERISTICS[2] $-30°C \le T_A \le +85°C$, $V_{CC1} = V_{CC2} = +2V$, $V_{EE} = -3.2V$, $R_L = 50\Omega$ to ground

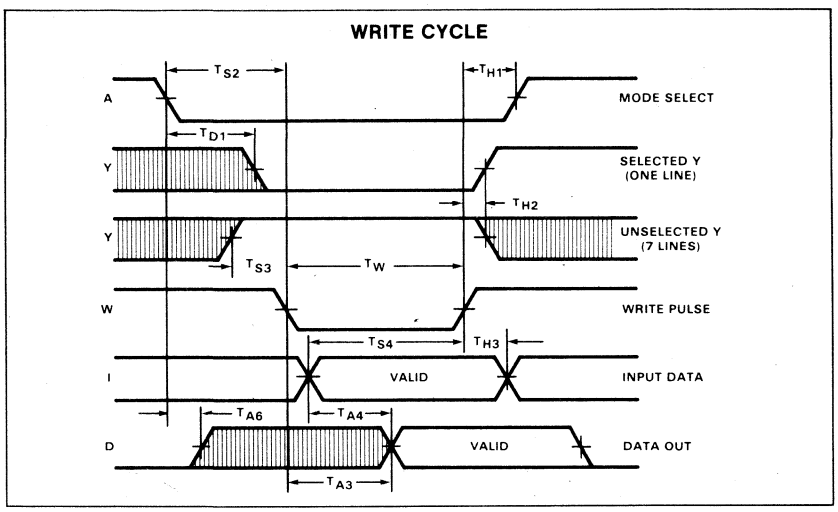
PARAMETER		FROM	TO	TEST CONDITIONS	LIMITS			UNIT
					Min[3]	Typ[4]	Max	
	Associate time							ns
T_{A1}		I±	Y±			8	12	
T_{A2}		A+	Y+			9	12	
	Disable time							ns
T_{D1}		A-	Y-			8	12	
T_{D2}		A+	D-			4	7	
T_{D3}		Y+	D-			9	13	
	Setup and hold time							ns
T_{H1}	Hold time	$\overline{W}$+	A+		1	0		
T_{S2}	Setup time	A-	Y-		15	11		
T_{H2}	Hold time	$\overline{W}$+	Y±		3	1		
T_{S3}	Setup time	Y+	$\overline{W}$-		3	2		
T_{H3}	Hold time	$\overline{W}$+	I±		3	1		
T_{S4}	Setup time	I±	$\overline{W}$+		5	3		
T_W	Write pulse width				10	5		ns
	Access time							ns
T_{A3}	Write	$\overline{W}$-	D±	$T_{S4} \ge T_W$		13	17	
T_{A4}	Write	I+,-	D+,-			9	13	
T_{A5}	Read	Y-	D+			6	10	
T_{A6}	Read	A-	D+			4		

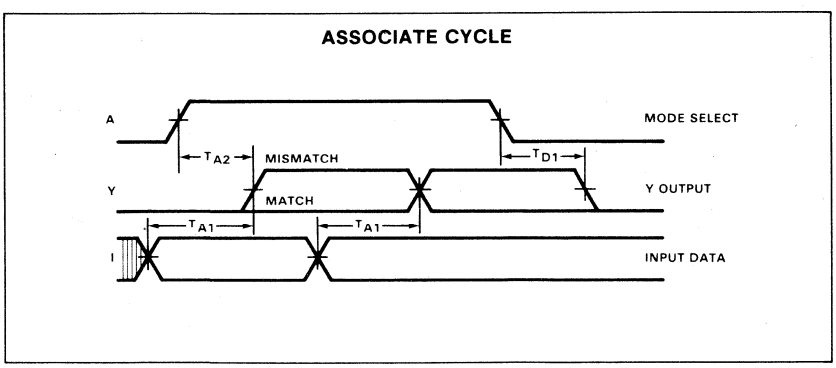
NOTES

1. Each ECL 10K series device has been designed to meet the dc and ac specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.
2. Refer to dc characteristics.
3. Minimum allowed.
4. All typical values are at $T_A = +25°C$.

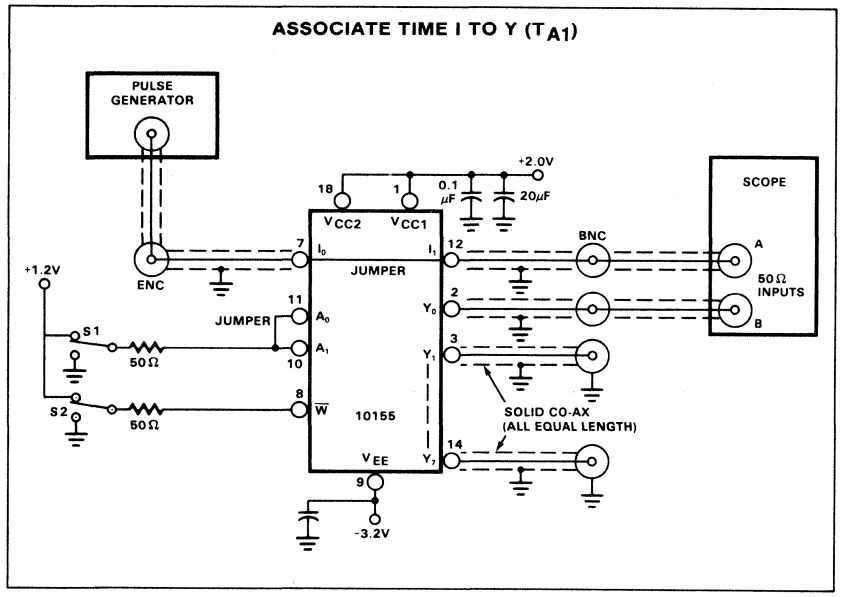
VOLTAGE WAVEFORMS







MEASUREMENT CIRCUIT



DESCRIPTION

Data is stored in a single storage matrix which is addressed via 2 independent sets of address inputs, designated respectively as Port A and Port B.

Data can be read from memory via either Port A or B, through their respective output sets. However, input data (latched on the leading edge of write enable in the input data latches) is written only in memory locations specified by the address on Port A, regardless of Port B.

When both Port addresses are equal, data from the same location can be read in either or both Port output sets by means of output select lines S_A and S_B. During Write, new data stored in memory is immediately transferred on both Port output sets.

When both Port addresses are different, 2 different locations can be simultaneously read from memory. It is also possible to simultaneously read through Port B while writing new input data through Port A by utilizing the "A_N" address to specify the location of the word to be written, and the "B_N" address to specify the word to be read.

Both devices are ideally suited for high speed accumulator and buffer memories, and can be readily expanded to form larger arrays by means of their output select and write enable lines.

Both the 82S12 and 82S112 are available over the limited temperature range of +10°C to +75°C. Over this temperature range, specify N82S12/82S112F,N.

FEATURES

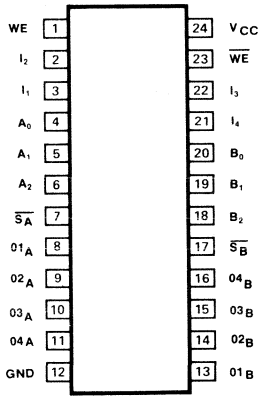
- **Address access time: 40ns max**
- **Write cycle time: 65ns max**
- **Power dissipation: 8.5mW/bit typ**
- **Input loading: -250μA max**
- **On-chip address decoding**
- **Output options:**
  - **82S12 Open collector**
  - **82S112 Tri-state**
- **Non-inverting outputs**
- **Input data latches**
- **Two write enable lines**
- **Separate output enable lines**
- **Output follows data input during write**
- **TTL compatible**

APPLICATIONS

- **Buffer memory**
- **Accumulator register**
- **Data routing/shifting**
- **ALU control**
- **Multiprocessor memory management**
- **Bandwidth increase by multi-operand fetch**
- **Communication controllers**
- **I/O data packing/unpacking**
- **Large FIFO memories**

PIN CONFIGURATION

F,N PACKAGE*



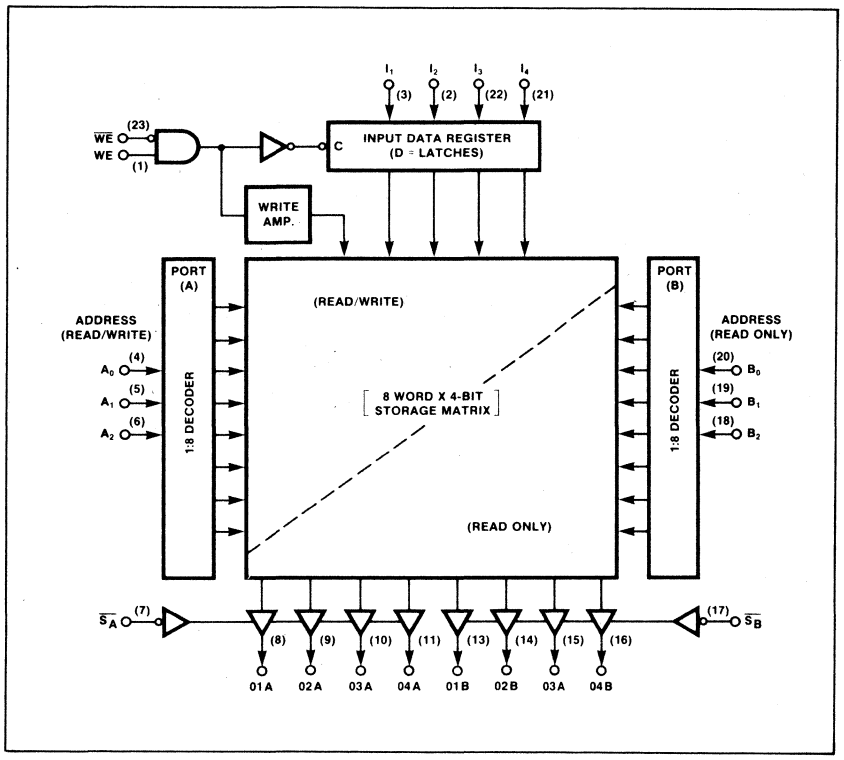
*F = Cerdip
N = Plastic

TRUTH TABLE

MODE	WE	$\overline{WE}$	I_N	$\overline{S_A}$	$\overline{S_B}$	PORT ADDRESS	82S12 $(O_N)A$	82S12 $(O_N)B$	82S112 $(O_N)A$	82S112 $(O_N)B$
Disabled				1	1	X	1	1	Hi-Z	Hi-Z
Read	0 or X	X or 1	X	0	1	A = B	Stored Data	1	Stored Data	Hi-Z
				1	0		1	Stored Data	Hi-Z	Stored Data
				0	0		Stored Data	Stored Data	Stored Data	Stored Data
				0	1	A ≠ B	[A_N]	1	[A_N]	Hi-Z
				1	0		1	[B_N]	Hi-Z	[B_N]
				0	0		[A_N]	[B_N]	[A_N]	[B_N]
Write	1	0	1/0	1	1	A = B	1	1	Hi-Z	Hi-Z
				0	1		I_N	1	I_N	Hi-Z
				1	0		1	I_N	Hi-Z	I_N
				0	0		I_N	I_N	I_N	I_N
				1	1	A ≠ B	1	1	Hi-Z	Hi-Z
				0	1		I_N	1	I_N	Hi-Z
				1	0		1	[B_N]	Hi-Z	[B_N]
				0	0		I_N	[B_N]	I_N	[B_N]

X = Don't care
[ ] = Contents of

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S12)	+5.5	
V_O	Off-state (82S112)	+5.5	
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS $+10°C \le T_A \le 75°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER[1]		TEST CONDITIONS	82S12			82S112			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IH}	High[1]	V_{CC} = 5.25V	2			2			
V_{IL}	Low[1]	V_{CC} = 4.75V			0.85			0.85	
V_{IC}	Clamp[1,3]	V_{CC} = 4.75V, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage	V_{CC} = 4.75V							V
V_{OH}	High[1,4]	I_{OH} = -2mA				2.4			
V_{OL}	Low[1,5]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.45	
	Input current								μA
I_{IH}	High	V_{IN} = 5.5V		1	25		1	25	
I_{IL}	Low	V_{IN} = 0.45V		-10	-250		-10	-250	
	Output current	V_{CC} = 5.25V							
I_{OLK}	Leakage[6]	V_{OUT} = 5.25V		1	40				μA
$I_{O(OFF)}$	Hi-Z state[6]	V_{OUT} = 5.25V					1	40	μA
		V_{OUT} = 0.45V					-1	-40	
I_{OS}	Short circuit[3,7]	V_{OUT} = 0V				-20		-70	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = 5.25V		110	160		110	160	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
V_{OUT}	Output	V_{OUT} = 2.0V		8			8		

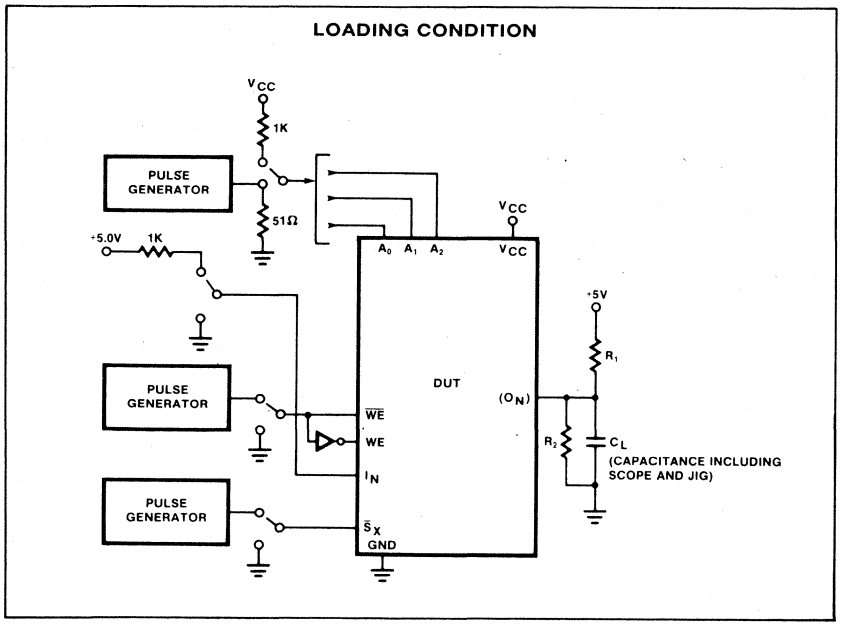
AC ELECTRICAL CHARACTERISTICS $+10°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ[2]	Max	
	Access time						ns
T_{AA}	Address	Output	Address			40	
T_{SE}	Port select	Output	Output enable			30	
	Disable time						ns
T_{SD}	Port deselect	Output	Output enable			30	
T_{WD}	Valid time	Output	Write enable			40	ns
	Setup and hold time						ns
T_{WSA}	Setup time	Write enable	Address	15	10		
T_{WHA}	Hold time			5	0		
T_{WSD}	Setup time	Write enable	Data in	15			
T_{WHD}	Hold time			10			
	Pulse width						ns
T_{WP}	Write enable			45			

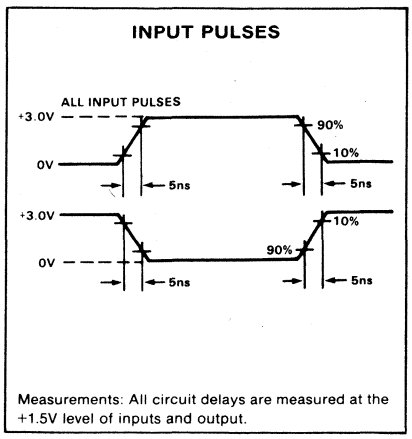
NOTES

1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Test one at the time.
4. Measured with V_{IL} applied to $\overline{S_X}$ and a logic high stored.
5. Measured with a logic low stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to $\overline{S_X}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with all inputs at 4.5V and the outputs open.

TEST LOAD CIRCUIT

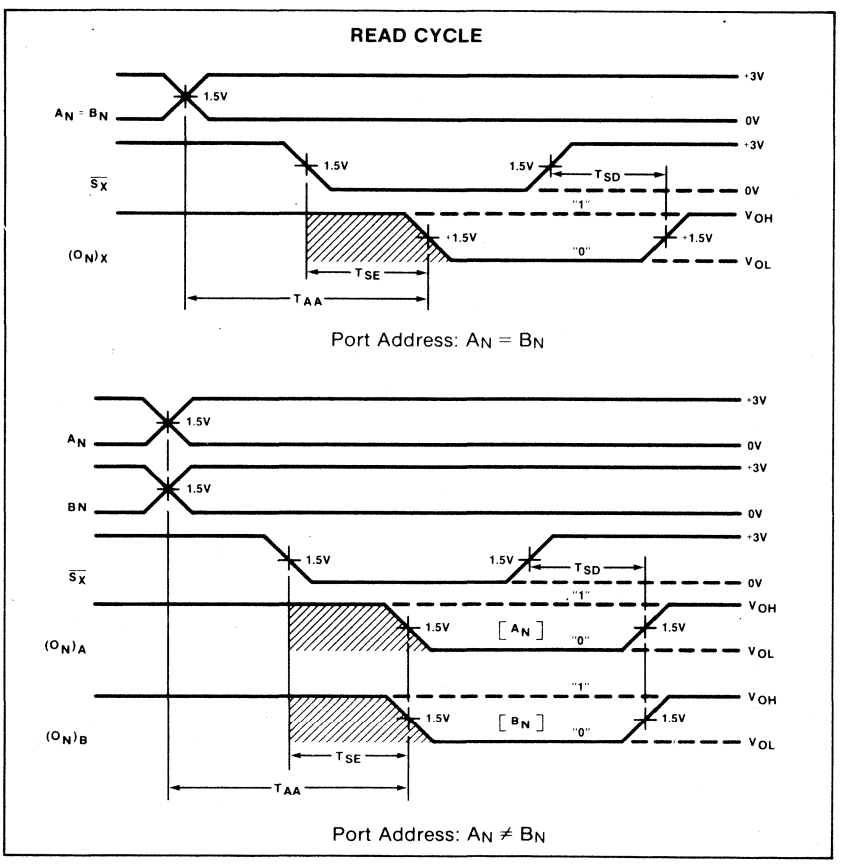


VOLTAGE WAVEFORM



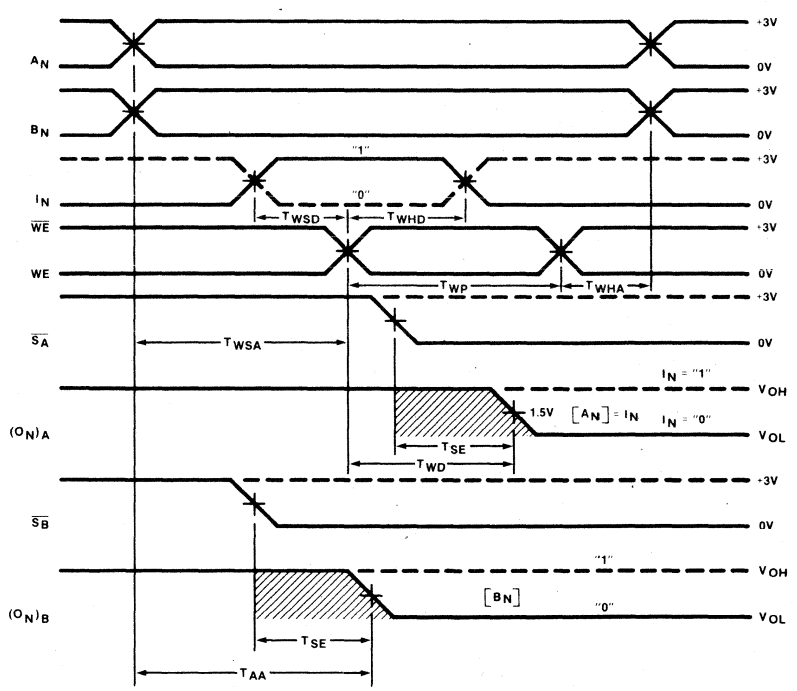
Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

TIMING DIAGRAMS



TIMING DIAGRAMS (Cont'd)

SIMULTANEOUS READ/WRITE CYCLE

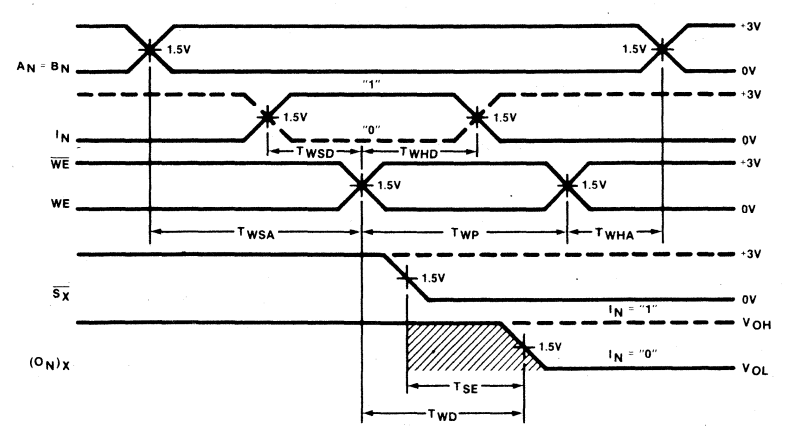


Port Address: $A_N \neq B_N$

A_N = Write

B_N = Read

PORT A WRITE CYCLE



Port Address: $A_N = B_N$

MEMORY TIMING DEFINITIONS

T_{SE}	Delay between beginning of Output Enable low (with Address valid) and when Data Output becomes valid.
T_{SD}	Delay between when Output Enable becomes high and Data Output is in Hi-Z or high state.
T_{AA}	Delay between beginning of valid Address (with Output Enable low) and when Data Output becomes valid.
T_{WHD}	Required delay between end of Write Enable pulse and end of valid Input Data.
T_{WP}	Width of Write Enable pulse.
T_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
T_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
T_{WD}	Delay between beginning of Write Enable pulse and when Data Output reflects the Data Input.
T_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.

DESCRIPTION

This family of Read/Write Random Access Memories is ideal for use in scratch pad and high-speed buffer memory applications.

These products are fully decoded memory arrays with separate input and output lines. They feature pnp inputs and 1 chip enable line for ease of memory expansion.

During Write, the outputs of each product assume the logic state defined in the truth table.

The family is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify the N prefix, and for the military temperature range (-55°C to +125°C) specify the S prefix. The 54/74S89/189 military temperature range product is ordered as S54S89/189. The S grade product is supplied in the F package only.

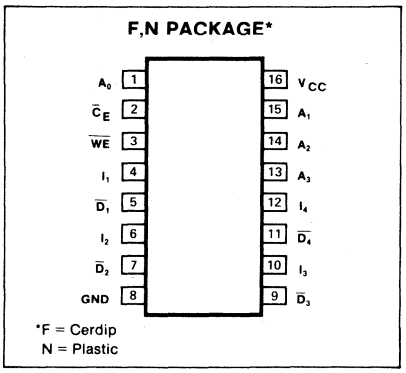
FEATURES

- **Output access time:**
  N82S25: 50ns
  N3101A: 35ns
  N54/74S89: 50ns
  N54/74S189: 35ns
- **Power dissipation: 6.25mW/bit, typ**
- **Input loading:**
  N grade: -100μA max
  S grade: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S25: Open collector
  3101A: Open collector
  54/74S89: Open collector
  54/74S189: Tri-state
- **Schottky processed**
- **TTL compatible**

APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Push down stacks**
- **Control store**

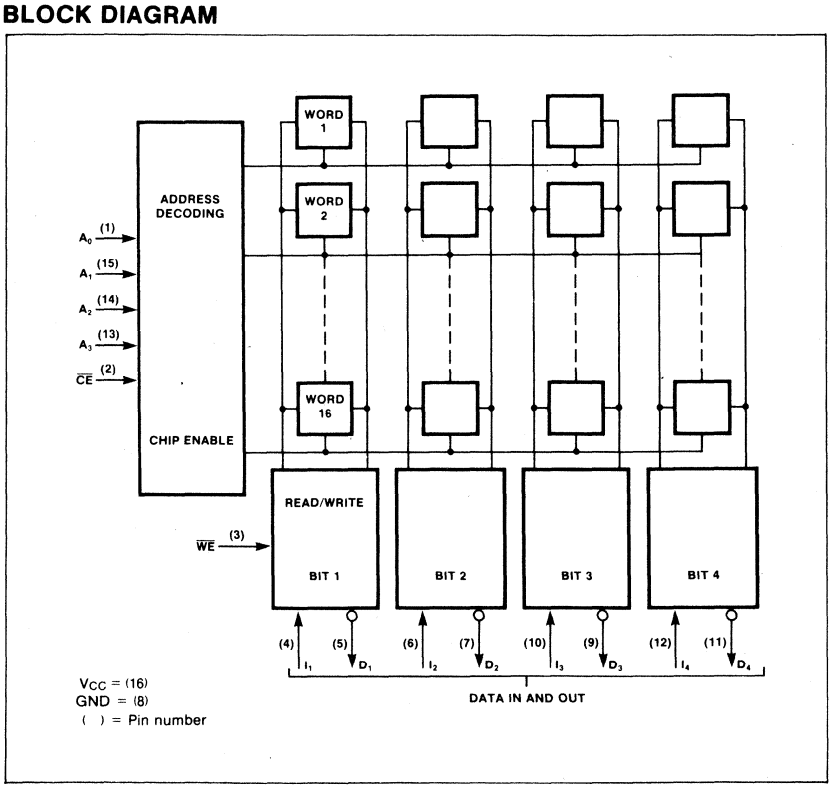
PIN CONFIGURATION



TRUTH TABLE

	$\overline{CE}$	$\overline{WE}$	D_{IN}	82S25	3101A	54/74S89	54/74S189
				DATA OUT			
Read	0	1	X	$\overline{\text{Stored data}}$	$\overline{\text{Stored data}}$	$\overline{\text{Stored data}}$	$\overline{\text{Stored data}}$
Write "0"	0	0	0	1	1	1	Hi-Z
Write "1"	0	0	1	1	1	0	Hi-Z
Disable	1	X	X	1	1	1	Hi-Z

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_{OH}	Output voltage High	+5.5	Vdc
T_A	Temperature range Operating		°C
	N grade	0 to +75	
	S grade	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N grade: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S grade: $55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER[7]		TEST CONDITIONS[6]	N GRADE			S GRADE			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low[1]	V_{CC} = Min			.85			.80	
V_{IH}	High[1]	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp[1,8]	I_{IN} = -12mA, V_{CC} = Min		-1.0	-1.5		-1.0	-1.5	
	Output voltage								V
V_{OL}	Low[3,4,1]	I_{OUT} = 16mA, V_{CC} = Min		0.35	0.45		0.35	0.5	
V_{OH}	High (54/74S189)[1]	I_{OUT} = 2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
I_{IH}	High	V_{IN} = 5.5V			10			25	
	Output current								
I_{OLK}	Leakage	CE = high, V_{OUT} = 5.5V, V_{CC} = Min		<1	100		<1	100	μA
I_{OS}	Short circuit (54/74S189)	V_{OUT} = 0V		-30	-100	-30		-100	mA
$I_{O(OFF)}$	Hi-Z (54/74S189)	$2.4 \ge V_{OUT} \ge 0.4V$			±50			±50	μA
I_{CC}	Supply current[4]								mA
	82S25, 54/74S89			80	105		80	120	
	3101A			80	105		80	120	
	54/74S189			80	110		80	110	
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IH} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V, CE = high		8			8		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, See ac test load
N grade: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S grade: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

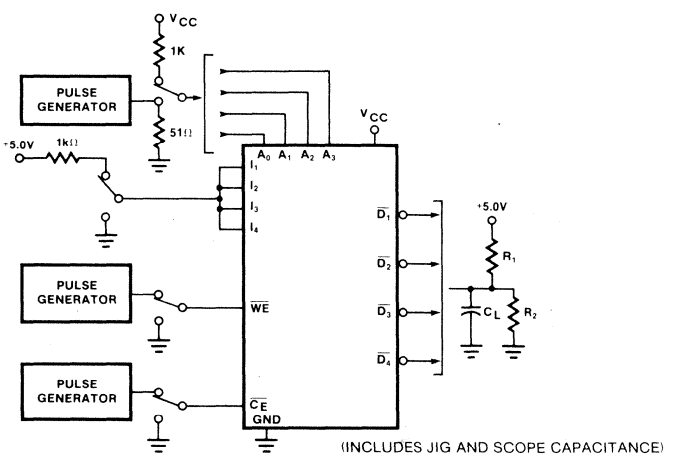
PARAMETER		TO	FROM	N82S25, N74S89			S82S25, S54S89			N3101A, N74S189			S3101A, S54S189			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time															ns
T_{AA}	Address				35	50		35	60		25	35		25	50	
T_{CE}	Chip enable				20	35		20	35		12	17		12	25	
T_{CD}	Disable time	Output	Chip enable		20	35		20	35		12	17		12	25	ns
T_{WD}	Response time	Output	Write enable		20	25		20	30		15	25		15	30	ns
T_{WR}	Write recovery time				35	50		35	60		22	35		22	40	ns
	Setup and hold time															ns
T_{WSA}	Setup time	Write	Address	5	-8		10	-8		0			0			
T_{WHA}	Hold time	enable		5	0		10	0		0			10			
T_{WSD}	Setup time	Write	Data in	30	15		30	15		25			30			
T_{WHD}	Hold time	enable		5	-3		10	-3		0			10			
T_{WSC}	Setup time	Write	$\overline{CE}$	0	-5		0	-5		0			0			
T_{WHC}	Hold time	enable		5	0		5	0		0			0			
	Pulse width															ns
T_{WP}	Write enable[5]			30	18		30	18		25			30			

NOTES

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Typical values are at $V_{CC} = +5.0V$ and $T_A = +25°C$.
3. Output sink current is supplied through a resistor to V_{CC}.
4. All sense outputs in low state.
5. To guarantee a Write into the slowest bit.
6. Positive current is defined as into the terminal referenced.
7. Positive logic definition: high ≈ +5.0V, low ≈ GND.
8. Test each input one at a time.

TEST LOAD CIRCUIT

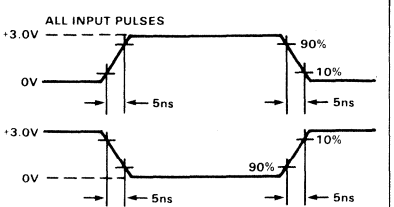
LOADING CONDITION



(INCLUDES JIG AND SCOPE CAPACITANCE)

VOLTAGE WAVEFORM

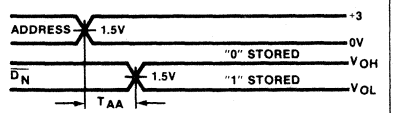
INPUT PULSES



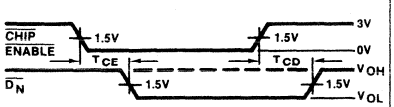
Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

TIMING DIAGRAMS

READ CYCLE

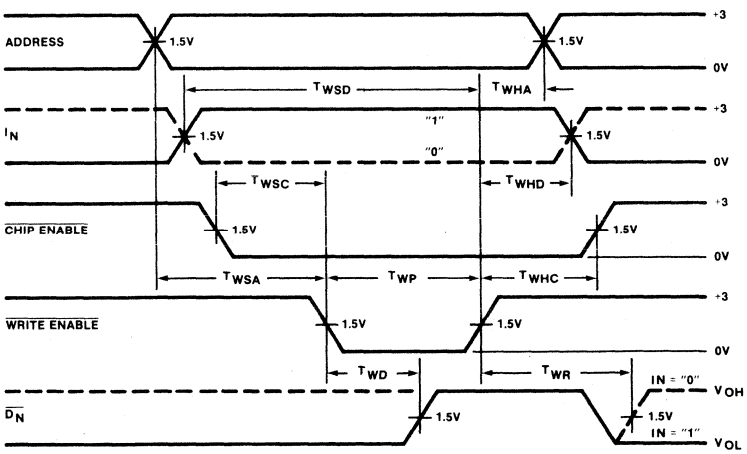


Address Access Time



Chip Enable/Disable Times

WRITE CYCLE



82S21-F,N

DESCRIPTION

The 82S21 is ideally suited for high speed buffers and as the memory element in high speed accumulators.

Words are selected through a 5-input decoder when the chip enable input, CE is at logic high. $\overline{WS_0}$ and $\overline{WS_1}$ are the write select inputs for the bit 0 and bit 1 of the word selected. $\overline{WE}$ is the write control input. When $\overline{WS_N}$ and $\overline{WE}$ are both at logic low data on the DI_0 and DI_1 data lines are written into the addressed word. The read function is enabled when either $\overline{WS_N}$ or $\overline{WE}$ is at logic high.

An internal latch provides the Write-While-Read capability. When the latch control line (strobe) is logic high and data is being read from the 82S21, the latch is effectively bypassed. The data at the output will be that of the addressed word. When strobe goes from a logic high to logic low, the outputs are latched and will remain latched regardless of the state of any other address or control line. When strobe goes from low to high, the outputs unlatch and will assume the contents of the present address word.

FEATURES

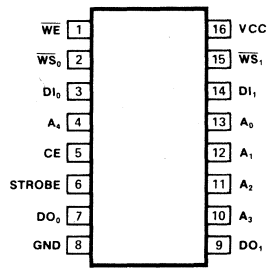
- **Address access time: 50ns max**
- **Write cycle time:**
  Transparent mode: 45ns max
  Latched mode: 60ns max
- **Power dissipation: 7.5mW/bit typ**
- **32mA output sink capability**
- **On-chip output latches**
- **Bit masking control lines**
- **Write-While-Read function**
- **Non-inverting open collector outputs**
- **TTL compatible**

APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Accumulator register**
- **Control store**

PIN CONFIGURATION

F,N PACKAGE



*F = Cerdip
N = Plastic

TRUTH TABLE

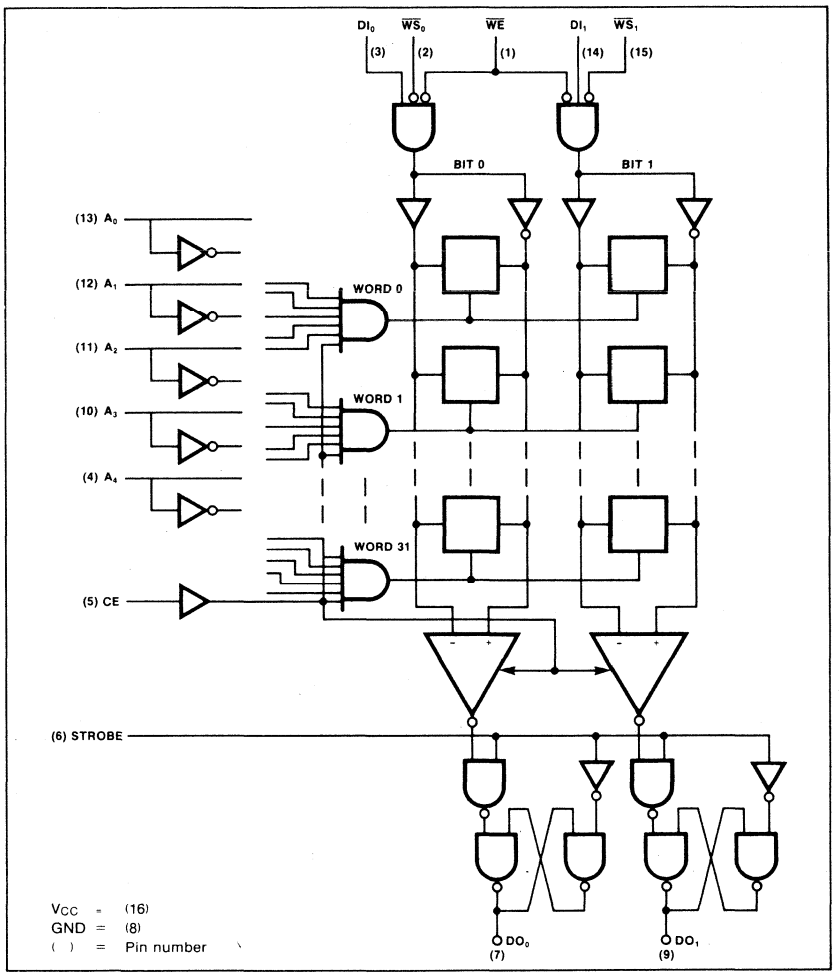
CE	$\overline{WE}$	$\overline{WS_0}$	$\overline{WS_1}$	STROBE	MODE	OUTPUTS
X	X	X	X	0	Output hold	$DO_N = (A_M)$ at last CE = high
0	X	X	X	0	Disabled	DO_N = high
1	1	X	X	1 or ↓	Read (transparent/latched)	$DO_N = (A_M)$
1	0	1	1	1 or ↓	Read (transparent/latched)	
1	0	0	0	0	Write data	$DO_N = (A_M)$ at last strobe = ↓
1	0	0	0	1	Write data	$DO_N = DI_N$
1	0	0	1	X	Write data into bit 0 only	If strobe = low:
						$DO_N = (A_M)$ at last strobe = ↓
1	0	1	0	X	Write data into bit 1 only	If strobe = high:
						$DO_N = DI_N$ or (A_M) as per $\overline{WS_N}$

( ) = Contents of
↓ = High → low transition

ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_{OH}	Output voltage	+5.5	Vdc
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	-65 to +150	

LOGIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 75°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER[1]		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low[1]	V_{CC} = 4.75V			0.85	
V_{IH}	High[1]	V_{CC} =5.25V	2			
V_{IC}	Clamp[1,3]	V_{CC} = 4.75V, I_{IN} = -18mA		-0.8	-1.2	
	Output voltage					V
V_{OL}	Low[1,4]	V_{CC} = 4.75V, I_{OL} = 32mA		0.35	0.45	
	Input current					
I_{IL}	Low	V_{IN} = 0.45V			-1.6	mA
I_{IH}	High	V_{IN} = 5.5V		<1	25	μA
	Output current	V_{CC} = 5.25V				μA
I_{OLK}	Leakage[5]	V_{OUT} = 5.25V		1	40	
I_{CC}	V_{CC} supply current[6]	V_{CC} = 5.25V		100	130	mA
	Capacitance	V_{CC} = 5.0V				pF
C_{IN}	Input	V_{IN} = 2.0V		5		
C_{OUT}	Output	V_{OUT} = 2.0V		8		

AC ELECTRICAL CHARACTERISTICS

$0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$, $R_1 = 150\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$

PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ[2]	Max	
Access time							ns
T_{AA} Address	Output	Address	Latched or transparent read		40	50	
T_{CE} Chip enable	Output	Chip enable	Latched or transparent read		40	50	
Disable time							ns
T_{CD} Chip enable	Output	Chip enable	Latched or transparent read		40	50	
Setup and hold time							ns
T_{WSA} Setup time	Write	Address	Latched or transparent write	15	10		
T_{WHA} Hold time				5	0		
T_{WSD} Setup time	Write	Data in	Latched or transparent write	25			
T_{WHD} Hold time				5	0		
T_{WSC} Setup time	Write	CE	Latched or transparent write	15	10		
T_{WHC} Hold time				5	0		
T_{CES} Setup time	Strobe	Chip enable	Latched read	50	40		
T_{CEH} Hold time				5	0		
T_{ADH} Hold time	Output	Address	Latched read	5	0		
Pulse width							ns
T_{SW} Strobe			Latched read	30			
T_{WP} Write inputs			Latched or transparent write	25			
Latch time							ns
T_{SLR} Read strobe	Strobe	Address	Latched read	50	40		
T_{SLW} Write strobe	Strobe	Write	Latched write	40	30		
T_{LRW} WWR strobe	Write	Strobe	Write while read	10	5		
Delatch time							ns
T_{DL} Strobe	Output	Strobe	Latched read		20	25	
T_{WD} Valid time	Output	Write	Latched or transparent write		30	40	ns

NOTES
1. All voltage values are with respect to network ground terminal.
2. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
3. Test each input one at a time.
4. Measured with a logic low stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IL} applied to CE, and V_{IH} to strobe.
6. I_{CC} is measured with all inputs at 4.5V, and the outputs open.

MEMORY TIMING DEFINITIONS

T_{CE} Delay between beginning of Chip Enable high (with Address valid) and when Data Output becomes valid.

T_{CD} Delay between when Chip Enable becomes low and Data Output is in high state.

T_{AA} Delay between beginning of valid Address (with Chip Enable high) and when Data Output becomes valid.

T_{WSC} Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.

T_{WHC} Required delay between end of Write Enable pulse and end of Chip Enable.

T_{WSA} Required delay between beginning of valid Address and beginning of Write Enable pulse.

T_{WHA} Required delay between end of Write Enable pulse and end of valid Address.

T_{WSD} Required delay between beginning of valid Data Input and end of Write Enable pulse.

T_{WHD} Required delay between end of Write Enable pulse and end of valid Input Data.

T_{WP} Width of Write Enable pulse.

T_{WD} Delay between beginning of Write Enable pulse and when Data Output reflects the contents of the Data Input.

T_{CES} Minimum delay between leading edge of Chip Enable and trailing edge of Strobe, for latching valid output data.

T_{CEH} Required delay between trailing edge of Strobe and end of Chip Enable, for latching valid output data.

T_{SLR} Minimum delay between Address valid time and trailing edge of Strobe, for latching valid output data.

T_{SW} Minimum width of Strobe pulse required to update contents of output data latches.

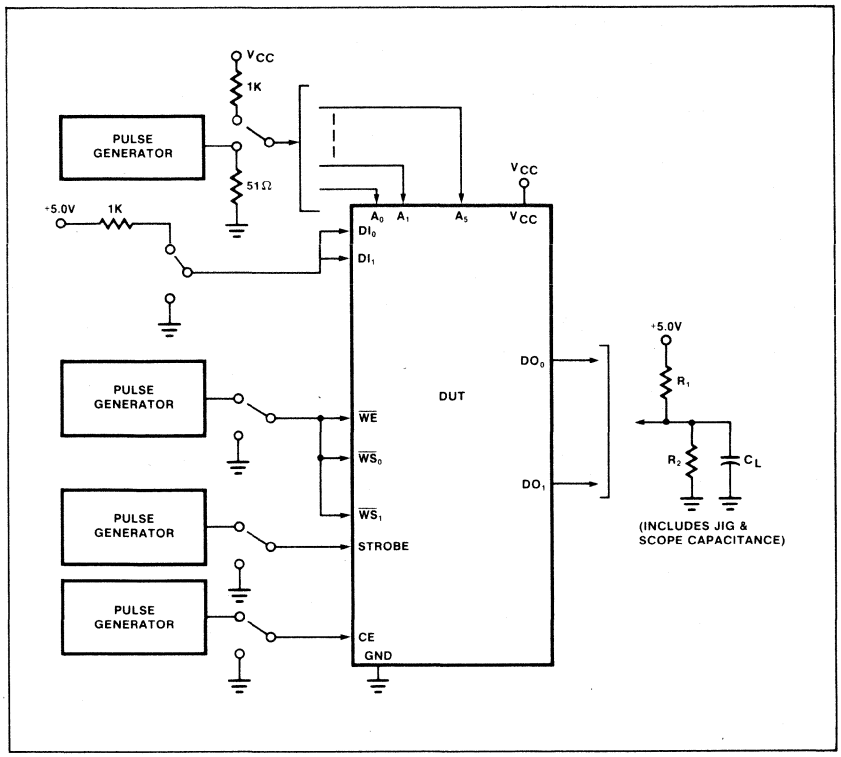
T_{ADH} Required delay between trailing edge of Strobe and end of valid Address.

T_{DL} Delay between leading edge of Strobe and when output data latches are released.

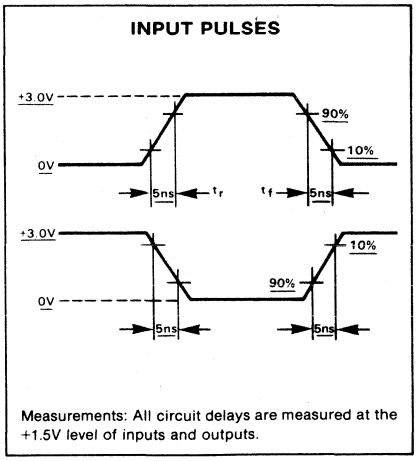
T_{LRW} Minimum delay required between trailing edge of Strobe and leading edges of Write Enable or Write Select for latching old output data (being read) while new data is being written (at the same address).

T_{SLW} Minimum delay between leading edge of Write Enable or Write Select and trailing edge of Strobe for latching data being written in output data latches.

TEST LOAD CIRCUIT

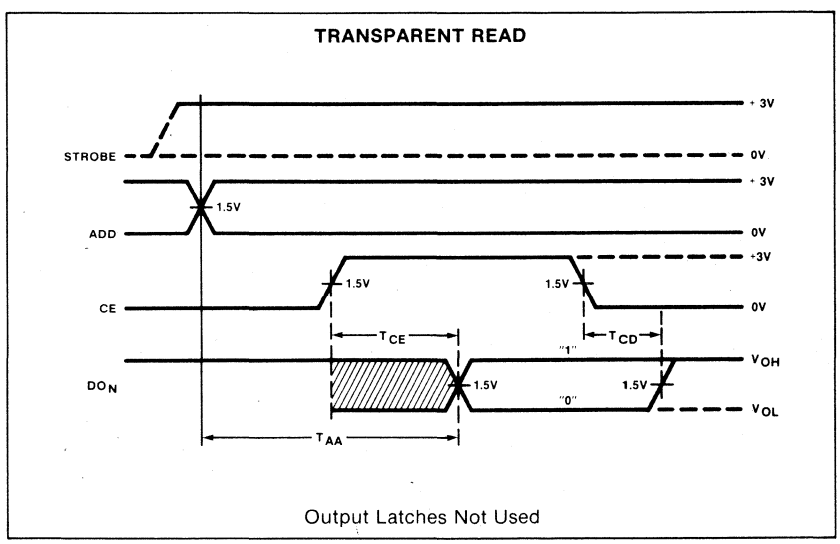


VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the +1.5V level of inputs and outputs.

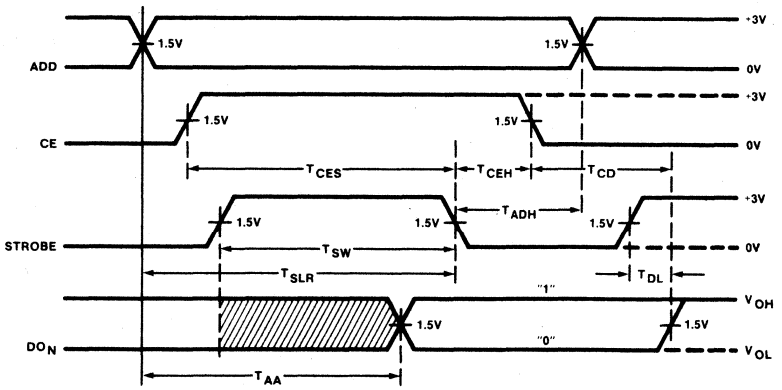
TIMING DIAGRAMS



Output Latches Not Used

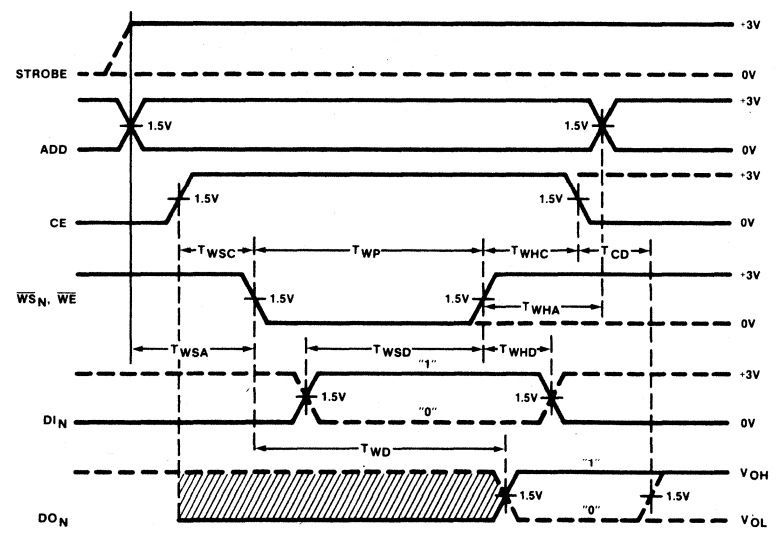
TIMING DIAGRAMS (Cont'd)

LATCHED READ



Output Latches Used

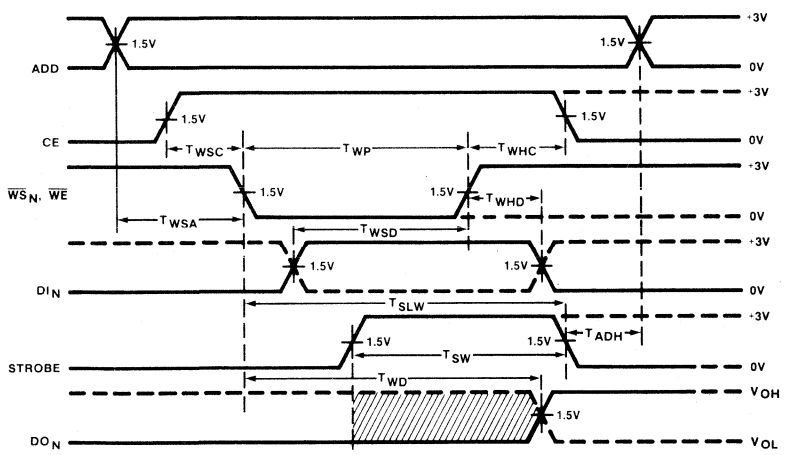
TRANSPARENT WRITE



Output Latches Not Used

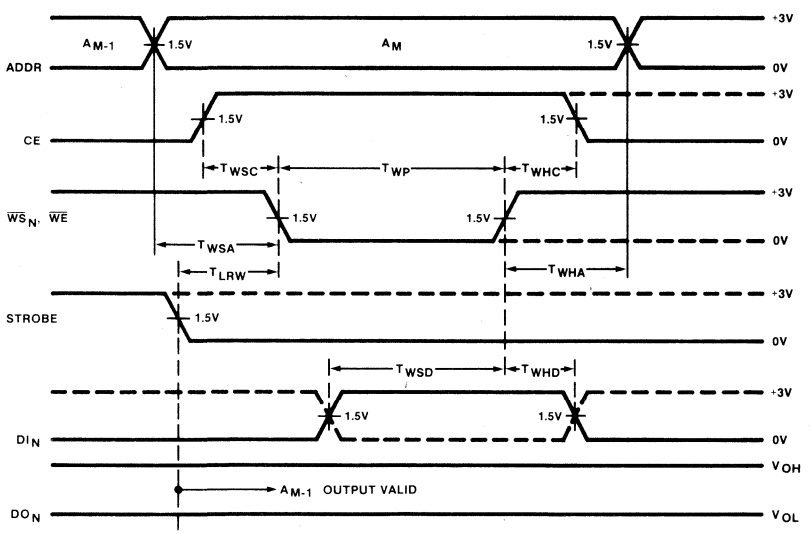
TIMING DIAGRAMS (Cont'd)

LATCHED WRITE



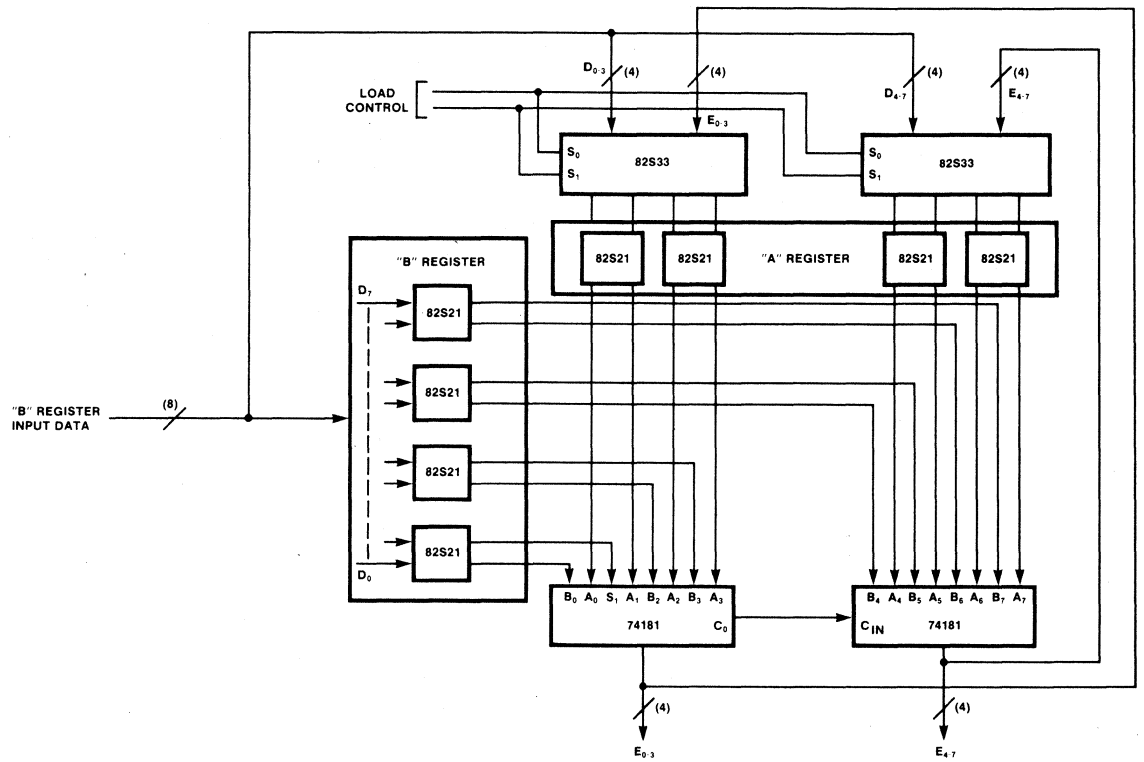
Output Latches Used

WRITE-WHILE-READ



TYPICAL APPLICATION

BASIC 8-BIT FULLY BUFFERED ACCUMULATOR



By use of the control lines S_0 and S_1 data is loaded into the "A" register through inputs D_X or from the outputs of the 74181's (E_X) to the 82S33's and stored in the 82S21's organized as a 32X8 RAM register. Data is loaded directly into the "B" register. With this arrangement, the function A+B → A (A plus B into A) can be performed in 70ns, typically, starting from data stored in the 82S21's.

DESCRIPTION

The 82S16/116 and 82S17/117 are read/write memory arrays which feature either open collector or tri-state output options for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and pnp input transistors which reduce input loading to 25μA for a high level, and −100μA for a low level.

During Write operation, the logical state of the output of both devices follows the complement of the data input being written. This feature allows faster execution of Write-Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a Write cycle.

Both devices have fast read access and write cycle times, and thus are ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

All devices are available in the commercial temperature range (0°C to +75°C) and are specified as N82S16/116/17/117, F or N. The 82S16 and 82S17 are also available in the military temperature range (−55°C to +125°C) and are specified as S82S16/17.

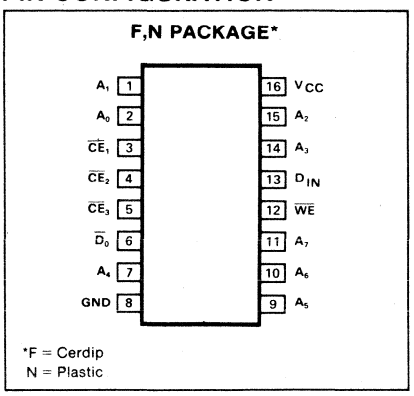
FEATURES

- **Address access time:**
  82S116/117: 40ns max
- **Write cycle time:**
  82S116/117: 25ns max
- **Power dissipation: 1.5mW/bit typ**
- **Input loading:**
  N82S116/117: −100μA
- **Output follows complement of data input during Write**
- **On-chip address decoding**
- **Output option:**
  82S16/116: Tri-state
  82S17/117: Open collector
- **Schottky clamped**
- **TTL compatible**

APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION



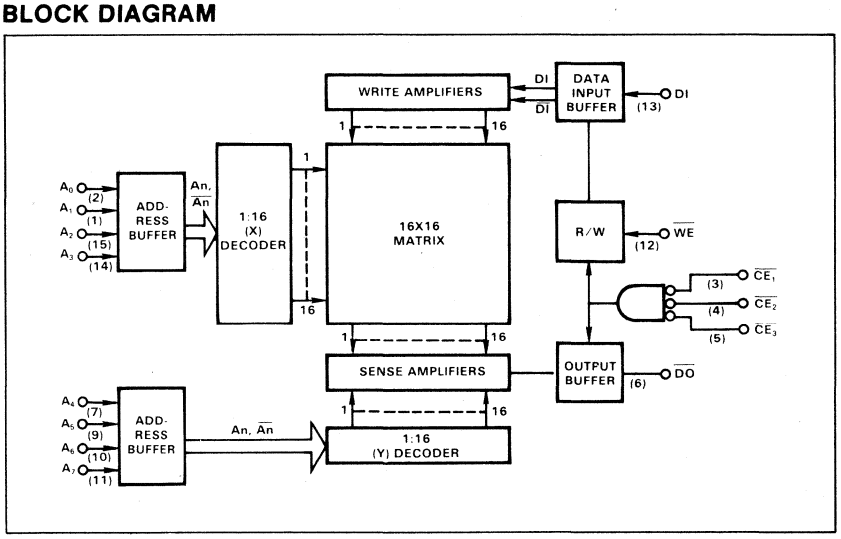
*F = Cerdip
N = Plastic

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	
				82S16/116	82S17/117
Read	0	1	X	Stored $\overline{data}$	Stored $\overline{data}$
Write "0"	0	0	0	1	1
Write "1"	0	0	1	0	0
Diasabled	1	X	X	High-Z	1

*"0" = All $\overline{CE}$ inputs low; "1" = one or more $\overline{CE}$ inputs high.
X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage	+5.5	Vdc
V_{OUT}	High (82S17)		
V_O	Off-state (82S16)		
	Temperature range		°C
T_A	Operating		
	S82S16/17	-55 to + 125	
	N82S16/17, N82S116/117	0 to +75	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S116/117, N82S16/17: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S16/17: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TEST CONDITIONS	N82S16/17/116/117			S82S16/17			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
	Input voltage[2]								V
V_{IH}	High	V_{CC} = Max	2.0			2.0			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = -12mA		-1.0	-1.5		-1.0	-1.5	
	Output voltage[2]	V_{CC}= Min							V
V_{OH}	High (82S16/116)[4]	I_{OH} = -3.2mA	2.6			2.4			
V_{OL}	Low[5]	I_{OL} = 16mA		0.35	0.45		0.35	0.5	
	Input current[3]	V_{CC} = Max							μA
I_{IH}	High	V_{IN} = 5.5V		1	25		1	25	
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-250	
	Output current								
I_{OLK}	Leakage (82S17/117)[6]	V_{OUT} = 5.5V		1	40		1	40	μA
$I_{O(OFF)}$	Hi-Z state (82S16/116)[6]	V_{OUT} = 5.5V		1	40		1	50	μA
		V_{OUT} = 0.45V		-1	-40		-1	-50	
I_{OS}	Short-circuit (82S16/116)[7]	V_{CC} = Max, V_O = 0V	-20		-70	-20		-70	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		80	115		80	120	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$
N82S116/117, N82S16/17: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S16/17: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

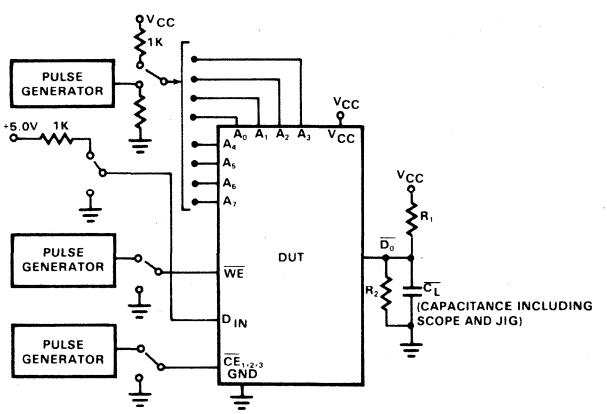
PARAMETER		TO	FROM	N82S16/17			N82S116/117			S82S16/17			UNIT
				Min	Typ[1]	Max	Min	Typ[1]	Max	Min	Typ[1]	Max	
	Access time												ns
T_{AA}	Address				40	50		30	40		40	70	
T_{CE}	Chip enable				30	40		15	25		30	40	
T_{CD}	Disable time	Output	Chip enable		30	40		15	25		30	40	ns
T_{WD}	Valid time	Output	Write enable		30	40		30	40		30	55	ns
	Setup and hold time												ns
T_{WSA}	Setup time	Write enable	Address	20	5		0	-5		20	5		
T_{WHA}	Hold time			5	0		0	-5		10	0		
T_{WSD}	Setup time	Write enable	Data in	40	30		25	15		50	40		
T_{WHD}	Hold time			5	0		0	-5		10	0		
T_{WSC}	Setup time	Write enable	$\overline{CE}$	10	0		0	-5		10	0		
T_{WHC}	Hold time			5	0		0	-5		10	0		
	Pulse width												ns
T_{WP}	Write enable[9]			30	15		25	15		40	20		

NOTES

1. All typical values are at V_{CC} = 5V, T_A +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at the time.
4. Measured with a logic low stored and V_{IL} applied to $\overline{CE_1}$, $\overline{CE_2}$ and $\overline{CE_3}$.
5. Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
7. Duration of the short-circuit should not exceed 1 second.
8. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.

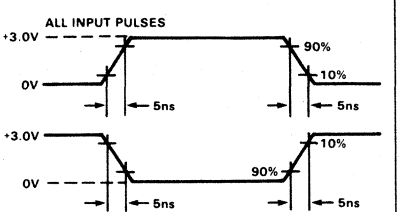
TEST LOAD CIRCUIT

LOADING CONDITION



VOLTAGE WAVEFORM

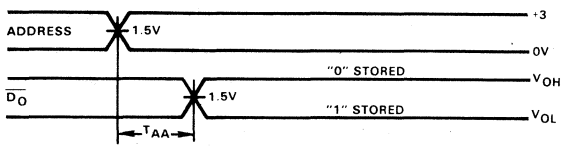
INPUT PULSES



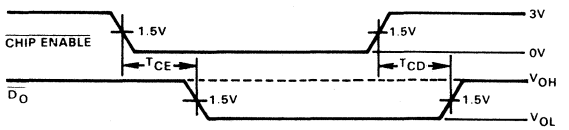
Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

TIMING DIAGRAMS

READ CYCLE

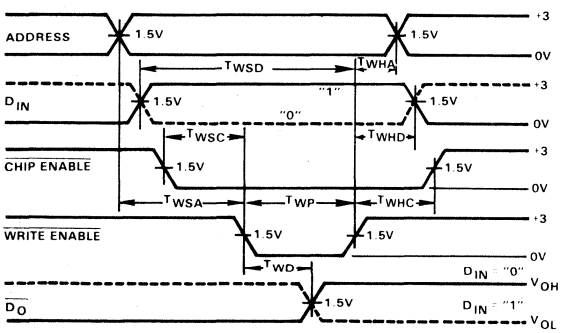


Address Access Time



Chip Enable/Disable Times

WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{CE}	Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
T_{CD}	Delay between when Chip Enable becomes high and Data Output is in off state.
T_{AA}	Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
T_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
T_{WHD}	Required delay between end of Write Enable pulse and end of valid Input Data.
T_{WP}	Width of Write Enable pulse.
T_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
T_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
T_{WD}	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.
T_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
T_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.

DESCRIPTION

The 82LS116 and 82LS117 are read/write memory arrays which feature either open collector or tri-state output options for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs, and pnp input transistors which reduce input loading to 25μA for a high level, and −100μA for a low level.

During Write operation, the logical state of the output of both devices follows the complement of the data input being written. This feature allows faster execution of Write-Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a Write cycle.

Both devices have fast read access and write cycle times, and thus are ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

Both devices are available in the commercial temperature range (0°C to +75°C) and are specified as N82LS116/117, F or N. The 82LS116 and 82LS117 are also available in the military temperature range (−55°C to +125°C) and are specified as S82LS116/117, F.

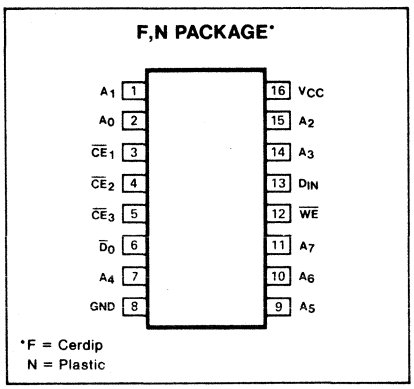
FEATURES

- **Address access time:**
  N82LS116/117: 40ns max
- **Write cycle time:**
  N82LS116/117: 25ns max
- **Power dissipation: 1.5mW/bit typ**
- **Input loading:**
  N82LS116/117: −100μA
- **Output follows complement of data input during Write**
- **On-chip address decoding**
- **Output option:**
  82LS116: Tri-state
  82LS117: Open collector
- **Schottky clamped**
- **TTL compatible**

APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION

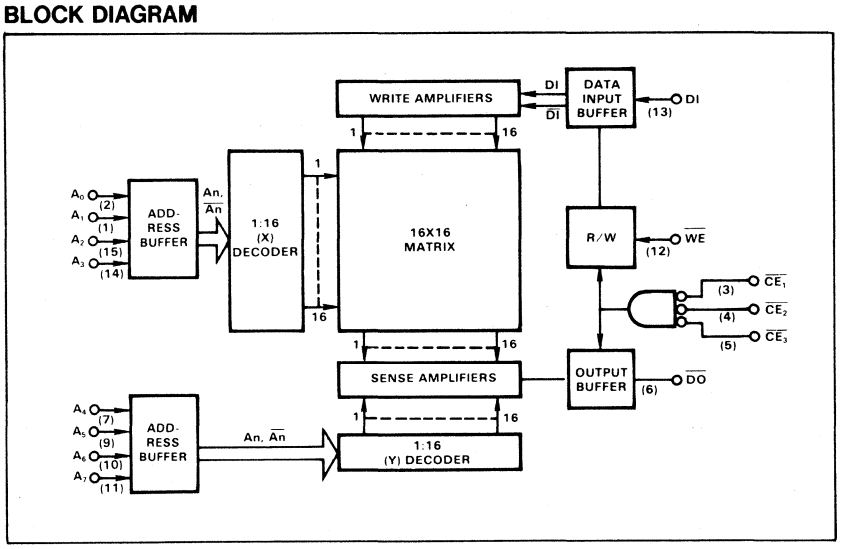


TRUTH TABLE

MODE	$\overline{CE}$ *	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	
				82LS116	82LS117
Read	0	1	X	Stored $\overline{data}$	Stored $\overline{data}$
Write "0"	0	0	0	1	1
Write "1"	0	0	1	0	0
Disabled	1	X	X	High-Z	1

*"0" = All $\overline{CE}$ inputs low; "1" = one or more $\overline{CE}$ inputs high.
X = Don't care.

BLOCK DIAGRAM



BIPOLAR MEMORY

OBJECTIVE SPECIFICATION

82LS116 F,N • 82LS117 F,N

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage	+5.5	Vdc
V_{OUT}	High (82LS117)		
V_O	Off-state (82LS116)		
	Temperature range		°C
T_A	Operating		
	S82LS116/117	−55 to + 125	
	N82LS116/117	0 to +75	
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82LS116/117: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82LS116/117: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TEST CONDITIONS	N82LS116/117			S82LS116/117			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
	Input voltage[2]								V
V_{IH}	High	V_{CC} = Max	2.0			2.0			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = −12mA		−1.0	−1.5		−1.0	−1.5	
	Output voltage[2]	V_{CC} = Min							V
V_{OH}	High (82LS116)[4]	I_{OH} = −1.0mA	2.6			2.4			
V_{OL}	Low[5]	I_{OL} = 16mA		0.35	0.45		0.35	0.5	
	Input current[3]	V_{CC} = Max							μA
I_{IH}	High	V_{IN} = 5.5V		1	25		1	25	
I_{IL}	Low	V_{IN} = 0.45V		−10	−100		−10	−250	
	Output current								
I_{OLK}	Leakage (82LS117)[6]	V_{OUT} = 5.5V		1	40		1	40	μA
$I_{O(OFF)}$	Hi-Z state (82LS116)[6]	V_{OUT} = 5.5V		1	40		1	50	μA
		V_{OUT} = 0.45V		−1	−40		−1	−50	
I_{OS}	Short-circuit (82LS116)[7]	V_{CC} = Max, V_O = 0V	−20		−70	−20		−70	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		50	70		50	70	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

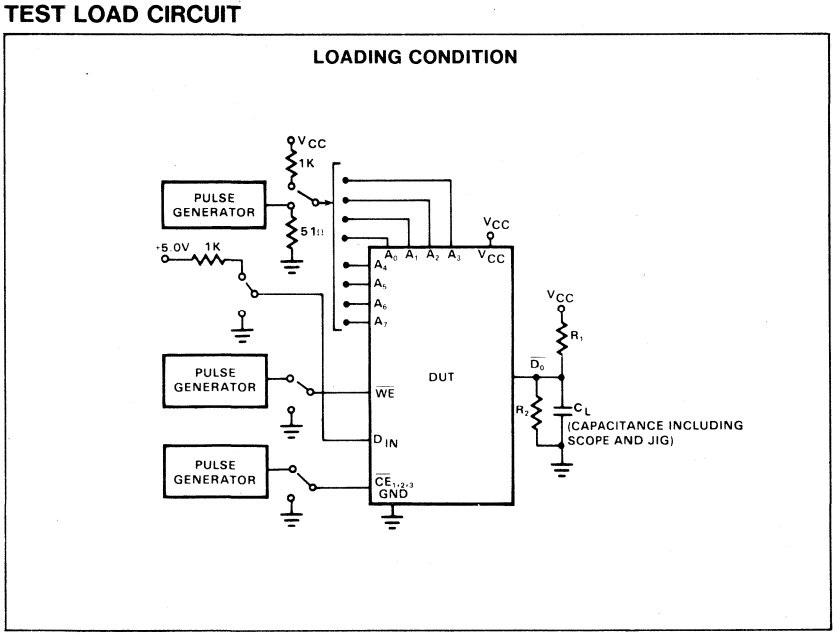
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$
N82LS116/117: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82LS116/117: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TO	FROM	N82LS116/117			S82LS116/117			UNIT
				Min	Typ[1]	Max	Min	Typ[1]	Max	
	Access time									ns
T_{AA}	Address				30	40		40	70	
T_{CE}	Chip enable				15	25		30	40	
T_{CD}	Disable time	Output	Chip enable		15	25		30	40	ns
T_{WD}	Valid time	Output	Write enable		30	40		30	55	ns
	Setup and hold time									ns
T_{WSA}	Setup time	Write enable	Address	0	−5		20	5		
T_{WHA}	Hold time			0	−5		10	0		
T_{WSD}	Setup time	Write enable	Data in	25	15		50	40		
T_{WHD}	Hold time			0	−5		10	0		
T_{WSC}	Setup time	Write enable	$\overline{CE}$	0	−5		10	0		
T_{WHC}	Hold time			0	−5		10	0		
	Pulse width									ns
T_{WP}	Write enable[9]			25	15		40	20		

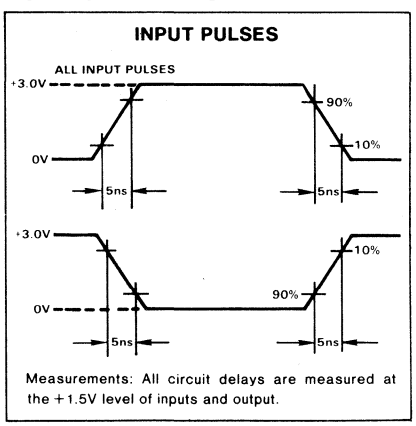
NOTES

1. All typical values are at V_{CC} = 5V, T_A +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at the time.
4. Measured with a logic low stored and V_{IL} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
5. Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{CE}_3$.
7. Duration of the short-circuit should not exceed 1 second.
8. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.

TEST LOAD CIRCUIT



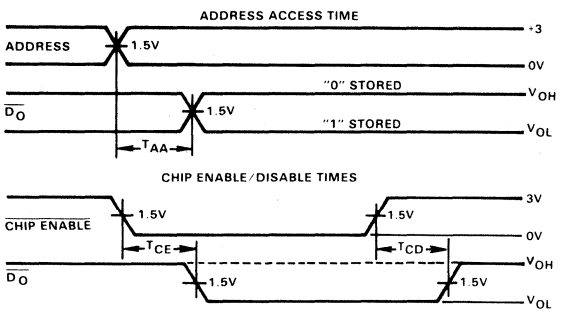
VOLTAGE WAVEFORM



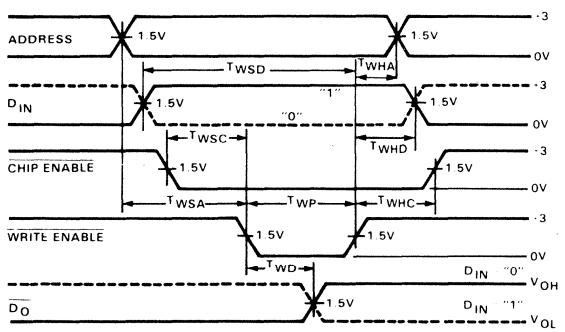
Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{CE}	Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
T_{CD}	Delay between when Chip Enable becomes high and Data Output is in off state.
T_{AA}	Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
T_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
T_{WHD}	Required delay between end of Write Enable pulse and end of valid Input Data.
T_{WP}	Width of Write Enable pulse.
T_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
T_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
T_{WD}	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.
T_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
T_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.

DESCRIPTION

The 54/74S200/201 and 54/74S301 are read/write memory arrays which feature either open collector or tri-state output options for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and pnp input transistors, which reduces input loading to 25μA for a high level and -250μA (S54S200/201/301) or -100μA (N74S200/201/301) for a low level.

The additional feature of output blanking during Write ($\overline{D}_O$ terminal "H" or "Hi-Z" state) permits $\overline{D}_O$ and D_{IN} terminals to share a common I/O line to reduce system interconnections. These devices have fast read access and write cycle times, and thus are ideally suited in high speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

They are available in both the commercial and military temperature ranges. The commercial temperature range (0°C to +75°C) is specified as N74S200/201/301, F or N, and the military temperature range (-55°C to +125°C) is specified as S54S200/201/301, F only.

FEATURES

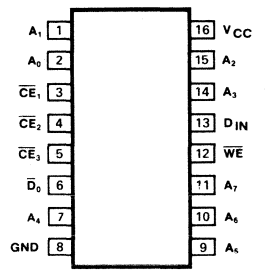
- **Address access time:**
  N74S200/201/301: 50ns max
  S54S200/201/301: 70ns max
- **Write cycle time:**
  N74S200/201/301: 50ns max
  S54S200/201/301: 60ns max
- **Power dissipation : 1.5mW/bit typ**
- **Input loading:**
  N74S200/201/301: -100μA max
  S54S200/201/301: -250μA max
- **Output blanking during Write**
- **On-chip address decoding**
- **Output option:**
  54/74S200/201: Tri-state
  54/74S301: Open collector
- **Schottky clamped**
- **TTL compatible**

APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION

F,N PACKAGE*



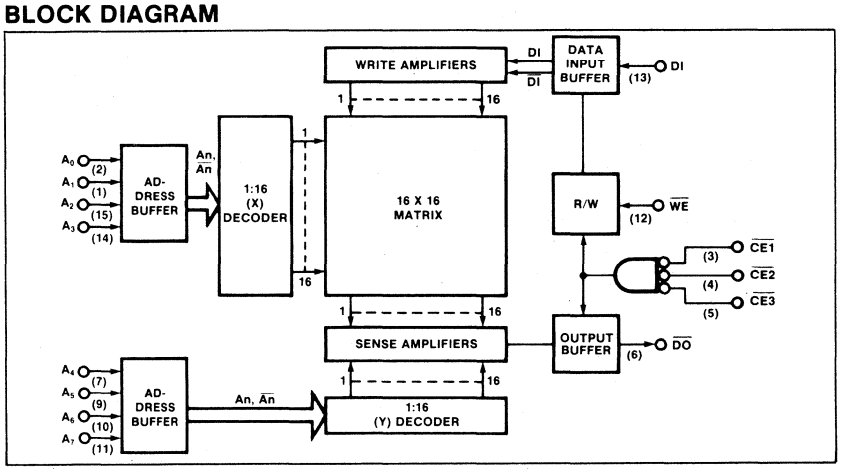
*F = Cerdip
N = Plastic

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D}_{OUT}$	
				54/74S301	54/74S200/201
Read	0	1	X	Stored $\overline{Data}$	Stored $\overline{Data}$
Write "0"	0	0	0	1	High-Z
Write "1"	0	0	1	1	High-Z
Disabled	1	X	X	1	High-Z

*"0" = All $\overline{CE}$ inputs low; "1" = One or more $\overline{CE}$ inputs high.
X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OUT}	High (54/74S301)	+5.5	
V_O	Off-state (54/74S200/201)	+5.5	
	Temperature range		°C
T_A	Operating		
	N74S200/201/301	0 to +70	
	S54S200/201/301	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N74S200/201/301: $0°C \le T_A \le +70°C$, $4.75V \le V_{CC} \le 5.25V$
S54S200/201/301: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N74S200/201/301			S54S200/201/301			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
	Input voltage								V
V_{IL}	Low[2]	V_{CC} = Min			0.85			0.8	
V_{IH}	High[2]	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp [2,3]	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[2,4]	I_{OL} = 16mA		0.35	0.45		0.30	0.50	
V_{OH}	High (N74S200/201)[2,5]	I_{OH} = 10.3mA	2.4						
V_{OH}	High (S54200/201)[2,5]	I_{OH} = -5.2mA				2.4			
	Input current[3]	V_{CC} = Max							
I_I	At V_{IN} Max	V_{IN} = 5.5V			1			1	mA
I_{IL}	Low	V_{IL} = 0.45V		-10	-100		-10	-250	μA
I_{IH}	High	V_{IH} = 2.7V		1	25		1	25	μA
	Output current								
I_{OLK}	Leakage (54/74S301)[6]	V_{IH} = 2V, V_O = 5.5V		1	40		1	50	μA
$I_{O(OFF)}$	Hi-Z state (54/74S200/201)[6]	V_{CC} = Max, V_O = 5.5V		1	40		1	100	μA
		V_{IH} = 2V, V_O = 0.4V		-1	-40		-1	-100	
I_{OS}	Short circuit (54/74S200/201)[7]	V_{CC} = Max, V_O = 0V	-30		-100	-30		-100	mA
I_{CC}	V_{CC} supply current[8]	V_{CC}= Max		80	130		80	130	mA
		V_{CC} = Max, T_A = +125°C						99	
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

R_L = 270Ω, C_L = 15pF, See ac test load
N74S200/201/301: 0°C ≤ T_A ≤ +70°C, 4.75V ≤ V_{CC} ≤ 5.25V
S54S200/201/301: −55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER[9]		TO	FROM	TEST CONDITIONS	N74S200/201			S54S200/201			UNIT
					Min	Typ[1]	Max	Min	Typ[1]	Max	
	Access time [B,D,E]										ns
t_{PLH}	Low to high		Address			40	50		40	70	
t_{PHL}	High to low										
t_{PLH}	Low to high		Address	R_{L1}=270Ω, R_{L2}=1kΩ							
	Enable time										ns
t_{ZL}	Low [C,D,F,G]	Output	Chip enable				35			45	
t_{ZH}	High [C,D,F,G]										
t_{PHL}	High to low [C,D,E]	Output	Chip enable	R_{L1}=270Ω, R_{L2}=1kΩ							
	Disable time										ns
t_{LZ}	Low [C,D,F,G]	Output	Chip enable	C_L=5pF			20			30	
t_{HZ}	High [C,D,F,G]										
t_{PLH}	Low to high [C,D,E]	Output	Chip enable Write enable	R_{L1}=270Ω, R_{L2}=1kΩ							
t_{PHL}	High to low [C,D,E]										
t_{LZ}	Low [D,G]	Output	Write enable	C_L=5pF			30			40	
t_{HZ}	High [D,G]										
	Sense recovery time										ns
t_{ZL}	Low [D,F]						40			50	
t_{ZH}	High [D,F]										
t_{SR}	Sense [D]										
	Pulse width [H]										ns
t_W	Write enable			R_{L1}=270Ω, R_{L2}=1kΩ	40			50			
	Setup and hold time [D]										ns
t_S	Setup time	Write enable	Address		0			0			
t_H	Hold time	Address	Write enable		10			10			
t_S	Setup time	Write enable	Address	R_{L1}=270Ω, R_{L2}=1kΩ							
t_H	Hold time	Address	Write enable								
t_S	Setup time	Write enable	Data		40			50			
t_H	Hold time	Data	Write enable		10			10			
t_S	Setup time	Write enable	Data	R_{L1}=270Ω, R_{L2}=1kΩ							
t_H	Hold time	Data	Write enable								
t_S	Setup time	Write enable	Chip enable		0			0			
t_H	Hold time	Chip enable	Write enable		0			0			
t_S	Setup time	Write enable	Chip enable	R_{L1}=270Ω, R_{L2}= 1kΩ							
t_H	Hold time	Chip enable	Write enable								

AC ELECTRICAL CHARACTERISTICS

(Cont'd) $R_L = 270\Omega$, $C_L = 15pF$, See ac test load
N74S200/201/301: $0°C \le T_A \le +70°C$, $4.75V \le V_{CC} \le 5.25V$
S54S200/201/301: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

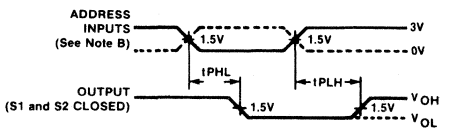
PARAMETER[9]		TO	FROM	TEST CONDITIONS	N74S301			S54S301			UNIT
					Min	Typ[1]	Max	Min	Typ	Max	
	Access time [B,D,E]										ns
t_{PLH}	Low to high		Address								
t_{PHL}	High to low										
t_{PLH}	Low to high		Address	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$		40	50		40	70	
	Enable time										ns
t_{ZL}	Low [C,D,F,G]	Output	Chip enable								
t_{ZH}	High [C,D,F,G]										
t_{PHL}	High to low [C,D,E]	Output	Chip enable	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$			35			45	
	Disable time										ns
t_{LZ}	Low [C,D,F,G]	Output	Chip enable	$C_L=5pF$							
t_{HZ}	High [C,D,F,G]										
t_{PLH}	Low to high [C,D,E]	Output	Chip enable	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$			20			30	
t_{PHL}	High to low [C,D,E]		Write enable				30			40	
t_{LZ}	Low [D,G]	Output	Write enable	$C_L=5pF$							
t_{HZ}	High [D,G]										
	Sense recovery time										ns
t_{ZL}	Low [D,F]										
t_{ZH}	High [D,F]										
t_{SR}	Sense [D]						40			50	
	Pulse width [H]										ns
t_W	Write enable			$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$	40			50			
	Setup and hold time [D]										ns
t_S	Setup time	Write enable	Address								
t_H	Hold time	Address	Write enable								
t_S	Setup time	Write enable	Address	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$	0			0			
t_H	Hold time	Address	Write enable		10			10			
t_S	Setup time	Write enable	Data								
t_H	Hold time	Data	Write enable								
t_S	Setup time	Write enable	Data	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$	40			50			
t_H	Hold time	Data	Write enable		10			10			
t_S	Setup time	Write enable	Chip enable								
t_H	Hold time	Chip enable	Write enable								
t_S	Setup time	Write enable	Chip enable	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$	0			0			
t_H	Hold time	Chip enable	Write enable		0			0			

NOTES

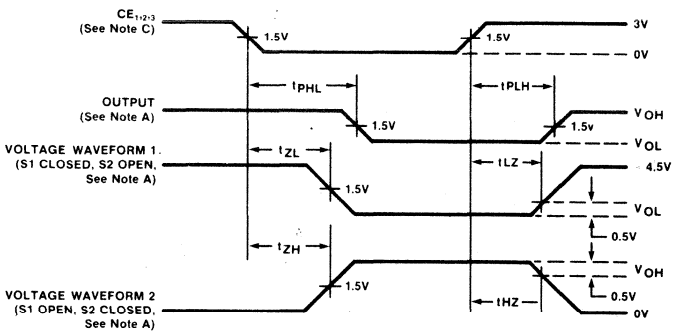
1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at a time.
4. Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with logic stored, and V_{IL} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
6. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
7. Duration of the short circuit should not exceed 1 second.
8. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. See timing diagram notes.

TIMING DIAGRAMS

READ CYCLE

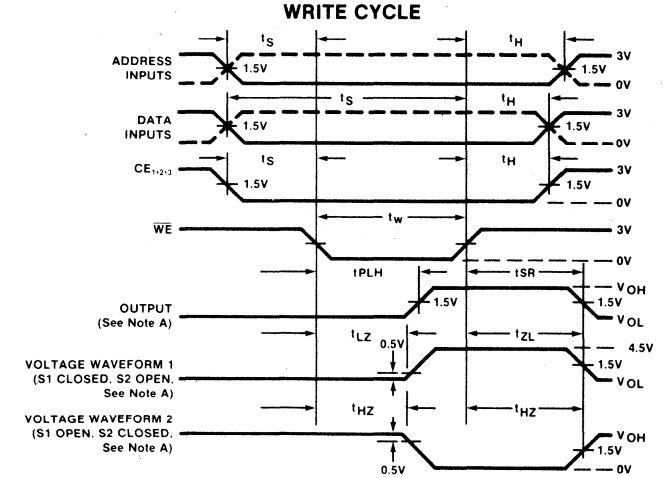


Access Time From Address



Chip Enable and Disable Time

WRITE CYCLE



NOTES

A. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.

B. When measuring delay times from address inputs, the chip enable inputs are low and the write enable input is high.

C. When measuring delay times from chip enable inputs, the address inputs are steady-state and the write enable input is high.

D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ns, $t_f \leq 2.5$ns, PRR ≤ 1MHz, and $Z_{OUT} \approx 50\Omega$.

E. t_{PLH} propagation delay time, low-to-high level output, t_{PHL} propagation delay time, high-to-low level output.

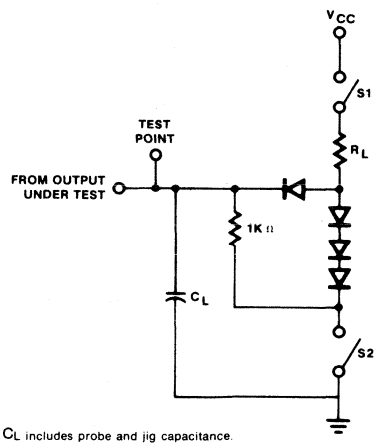
F. t_{ZH} propagation delay time, Hi-Z to high level output, t_{ZL} propagation delay time, Hi-Z to low level output.

G. T_{HZ} propagation delay time, high level to Hi-Z output, t_{LZ} propagation delay time, low level to Hi-Z output.

H. Minimum required to guarantee a Write into the slowest bit.

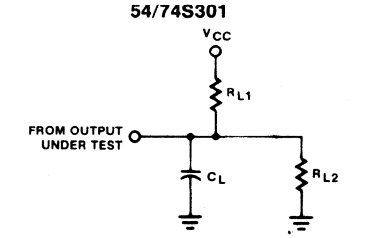
TEST LOAD CIRCUITS

54/74S200/201



C_L includes probe and jig capacitance.
All diodes are 1N3064.

54/74S301



C_L includes probe and jig capacitance.
All diodes are 1N3064.

82S09-I,N

DESCRIPTION

The organization of this device allows byte manipulation of data, including parity. Where parity is not monitored, the ninth bit can be used as a flag or status indicator for each word stored. With a typical access time of 30ns, it is ideal for scratch-pad, push-down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S09 features open collector outputs, chip enable input, and a very low current pnp input structure to enhance memory expansion.

During Write operation, the logic state of the device output follows the complement of the data input being written. This feature allows faster execution of Write-Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a Write cycle.

The 82S09 is available in the commercial and military temperature ranges. For the commercial temperature ranges. (0°C to +75°C) specify N82S09, and for the military temperature range (-55°C to +125°C) specify S82S09.

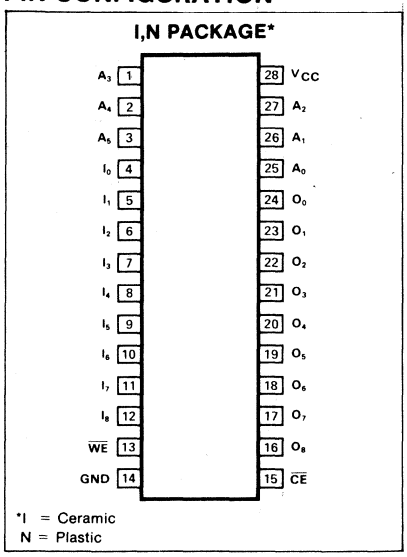
FEATURES

- **Address access time:**
  N82S09: 45ns max
  S82S09: 80ns max
- **Write cycle time:**
  N82S09: 45ns max
  S82S09: 75ns max
- **Power dissipation: 1.3mW/bit typ**
- **Input loading:**
  N82S09: -100μA max
  S82S09: -150μA max
- **Output follows complement of data input during Write**
- **On-chip address decoding**
- **Schottky clamped**
- **Fully TTL compatible**

APPLICATIONS

- **Buffer memory**
- **Control register**
- **FIFO memory**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION



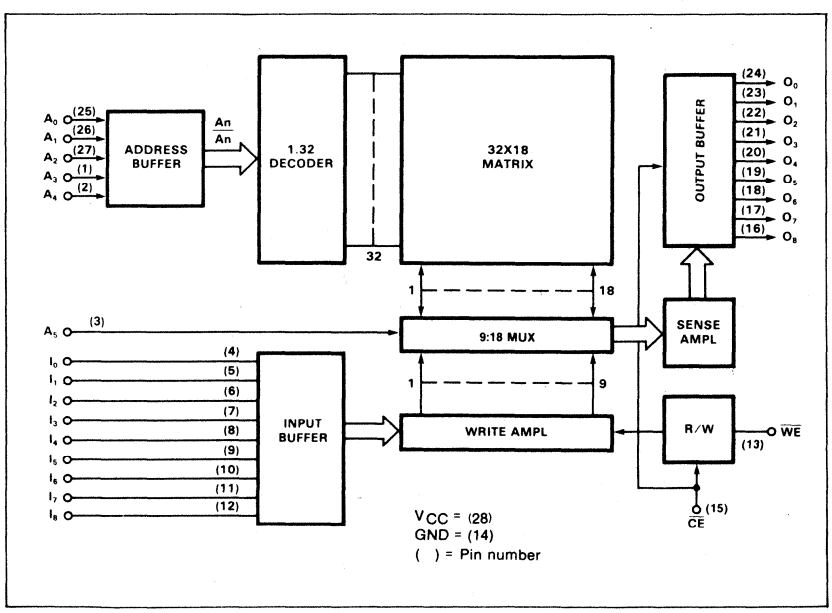
*I = Ceramic
N = Plastic

TRUTH TABLE

MODE	CE	WE	I_N	
Read	0	1	X	Complement of data stored
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disabled	1	X	X	1

X = Don't care

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S10)	+5.5	
T_A	Temperature range		°C
	Operating		
	N82S09	0 to +75	
	S82S09	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS[1,8]

N82S09: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

S82S09: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER[1]		TEST CONDITONS	N82S09			S82S09			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low	V_{CC} = Min			.85			.80	
V_{IH}	High	V_{CC} = Max	2.0			2.2			
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = -12mA		-1.0	-1.5		-1.0	-1.5	
	Output voltage								V
V_{OL}	Low[4]	V_{CC} = Min, I_{OL} = 6.4mA		0.35	0.5		0.35	0.5	
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
I_{IH}	High	V_{IN} = 5.5V		1	25		1	40	
	Output current								μA
I_{OLK}	Leakage[5]	V_{CC} = Max, V_{OUT} = 5.5V		1	40		1	60	
I_{CC}	V_{CC} supply current[6]	V_{CC} = Max		150	190		150	200	mA
	Capacitance	V_{CC} =5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS[8] $R_1 = 600\Omega$, $R_2 = 900\Omega$, $C_L = 30pF$, See ac test load

N82S09: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

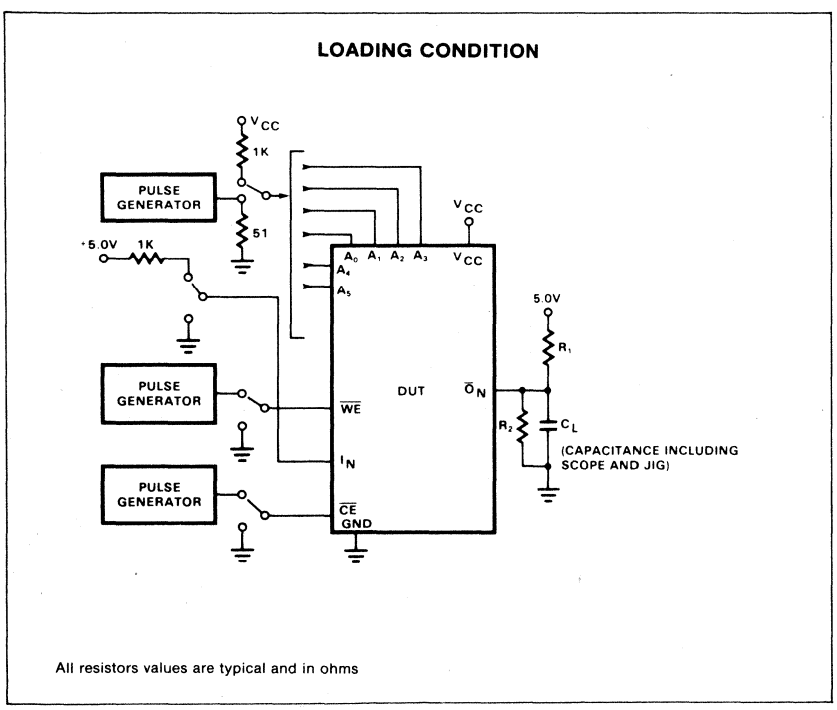
S82S09: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N82S09			S82S09			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time									ns
T_{AA}	Address				30	45		30	80	
T_{CE}	Chip enable				15	30		15	50	
T_{CD}	Disable time	Output	Chip enable		15	30		15	50	ns
T_{WD}	Valid time	Output	Write enable		25	50		25	80	ns
	Setup and hold time									ns
T_{WSA}	Setup time	Write enable	Address	5	0		10	0		
T_{WHA}	Hold time									
T_{WSD}	Setup time	Write enable	Data in	35	25		50	25		
T_{WHD}	Hold time			5	0		5	0		
T_{WSC}	Setup time	Write enable	CE	5	0		10	0		
T_{WHC}	Hold time									
	Pulse width									ns
T_{WP}	Write enable[7]			35	25		50	25		

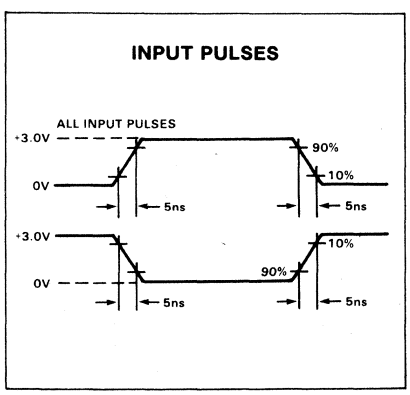
NOTES

1. All voltage values are with respect to network ground terminal.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Test each input one at a time.
4. Measured with the logic low stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IH} applied to $\overline{CE}$.
6. I_{CC} is measured with the write enable and memory enable input grounded, all other inputs at 4.5V, and the outputs open.
7. Minimum required to guarantee a Write into the slowest bit.
8. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.

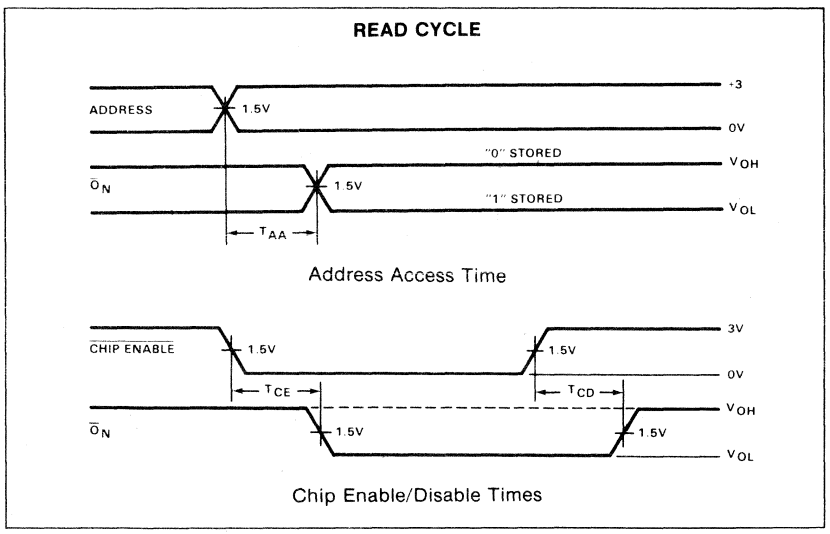
TEST LOAD CIRCUIT

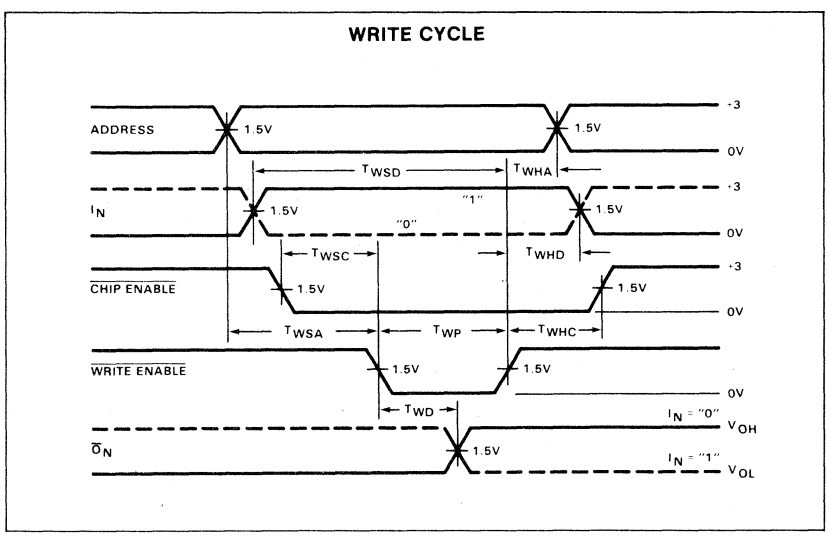


VOLTAGE WAVEFORM



TIMING DIAGRAMS





MEMORY TIMING DEFINITIONS

T_{CE}	Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
T_{CD}	Delay between when Chip Enable becomes high and Data Output is in off state.
T_{AA}	Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
T_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
T_{WHD}	Required delay between end of Write Enable pulse and end of valid Input Data.
T_{WP}	Width of Write Enable pulse.
T_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
T_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
T_{WD}	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.
T_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
T_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.

DESCRIPTION

The organization of this device allows byte manipulation of data, including parity. Where parity is not monitored, the ninth bit can be used as a flag or status indicator for each word stored. With a typical access time of 25ns, it is ideal for scratch-pad, push-down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S09A features open collector outputs, chip enable input, and a very low current pnp input structure to enhance memory expansion.

During Write operation, the output goes to a "1".

The 82S09A is available in the commercial and military temperature ranges. For the commercial temperature ranges. (0°C to +75°C) specify N82S09A, and for the military temperature range (−55°C to +125°C) specify S82S09A.

FEATURES

- **Address access time:**
  N82S09A: 35ns max
  S82S09A: 55ns max
- **Write cycle time:**
  N82S09A: 45ns max
  S82S09A: 55ns max
- **Power dissipation: 1.3mW/bit typ**
- **Input loading:**
  N82S09A: −100μA max
  S82S09A: −150μA max
- **Output is blanked during Write**
- **On-chip address decoding**
- **Schottky clamped**
- **Fully TTL compatible**

APPLICATIONS

- **Buffer memory**
- **Control register**
- **FIFO memory**
- **Push down stack**
- **Scratch pad**

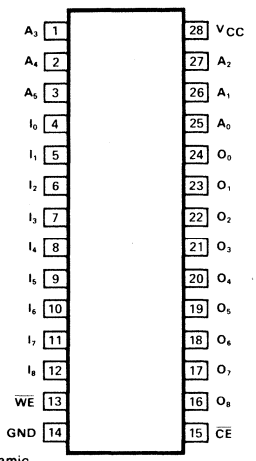
REPLACEMENT GUIDE

	T_{AA}	I_{OL}	OUTPUT LOGIC
82S09	45ns	6.4mA	T
82S09A	35ns	8mA	B

T-Transparent during WRITE
B-High impedance during WRITE

PIN CONFIGURATION

I,N PACKAGE*



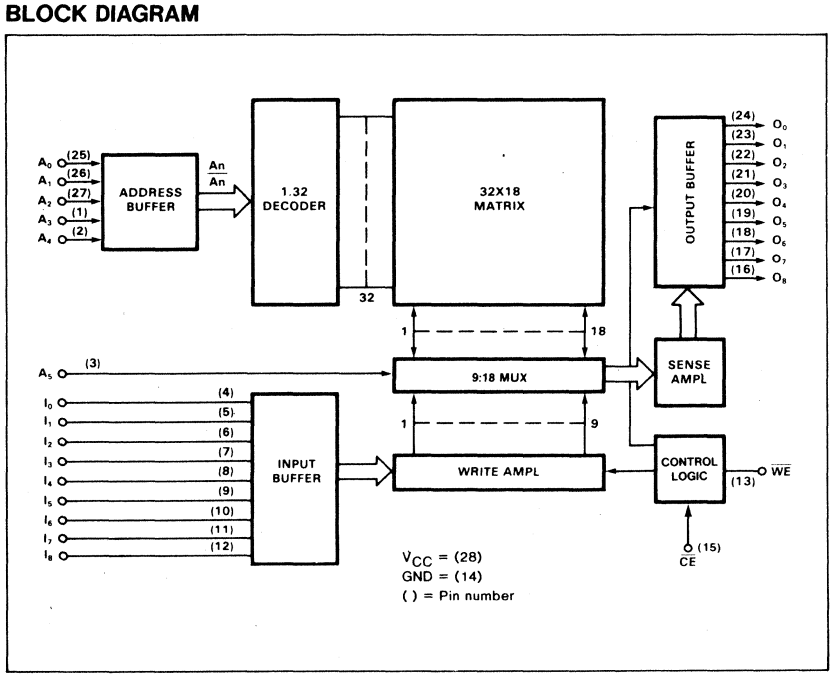
*I = Ceramic
N = Plastic

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	I_N	$\overline{O}_N$
Read	0	1	X	Complement of data stored
Write "0"	0	0	0	1
Write "1"	0	0	1	1
Disabled	1	X	X	1

X = Don't care

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High	+5.5	
T_A	Temperature range		°C
	Operating		
	N82S09A	0 to +75	
	S82S09A	−55 to +125	
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS[1,8]

N82S09A: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S09A: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER[1]		TEST CONDITIONS	N82S09A			S82S09A			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low	V_{CC} = Min			.85			.80	
V_{IH}	High	V_{CC} = Max	2.0			2.2			
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = −12mA		−1.0	−1.5		−1.0	−1.5	
	Output voltage								V
V_{OL}	Low[4]	V_{CC} = Min, I_{OL} = 8.0mA		0.35	0.5		0.35	0.5	
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100		−10	−150	
I_{IH}	High	V_{IN} = 5.5V		1	25		1	40	
	Output current								μA
I_{OLK}	Leakage[5]	V_{CC} = Max, V_{OUT} = 5.5V		1	40		1	60	
I_{CC}	V_{CC} supply current[6]	V_{CC} = Max		150	190		150	200	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS[8]

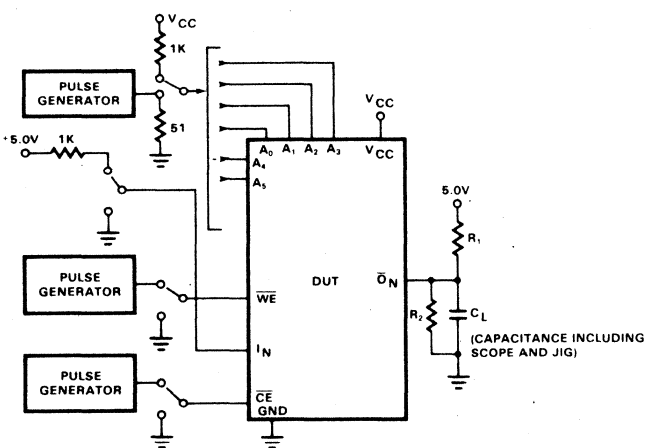
$R_1 = 600\Omega$, $R_2 = 900\Omega$, $C_L = 30pF$, See ac test load
N82S09A: $0° \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S09A: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TO	FROM	N82S09A			S82S09A			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time									ns
T_{AA}	Address				25	35		25	55	
T_{CE}	Chip enable				15	25		15	35	
T_{CD}	Disable time	Output	Chip enable		15	25		15	35	ns
T_{WD}	Valid time	Output	Write enable		20	25		20	50	ns
T_{WR}	Write recovery time	Output	Write enable		20	25		20	50	ns
	Setup and hold time									ns
T_{WSA}	Setup time	Write enable	Address	5	0		5	0		
T_{WHA}	Hold time			5	0		5	0		
T_{WSD}	Setup time	Write enable	Data in	30	20		45	20		
T_{WHD}	Hold time			5	0		5	0		
T_{WSC}	Setup time	Write enable	$\overline{CE}$	5	0		5	0		
T_{WHC}	Hold time									
	Pulse width									ns
T_{WP}	Write enable[7]			35	20		45	20		

NOTES
1. All voltage values are with respect to network ground terminal.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Test each input one at a time.
4. Measured with the logic low stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IH} applied to $\overline{CE}$.
6. I_{CC} is measured with the write enable and chip enable input grounded, all other inputs at 4.5V, and the outputs open.
7. Minimum required to guarantee a Write into the slowest bit.
8. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.

TEST LOAD CIRCUIT

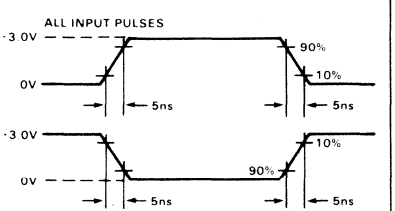
LOADING CONDITION



All resistors values are typical and in ohms

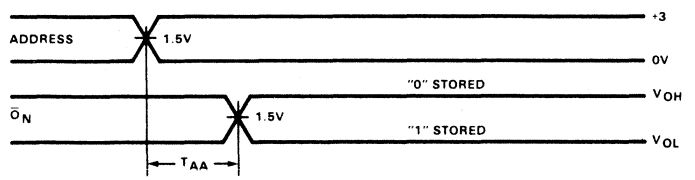
VOLTAGE WAVEFORM

INPUT PULSES

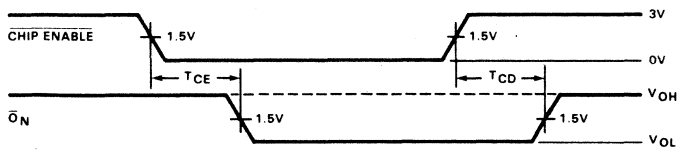


TIMING DIAGRAMS

READ CYCLE

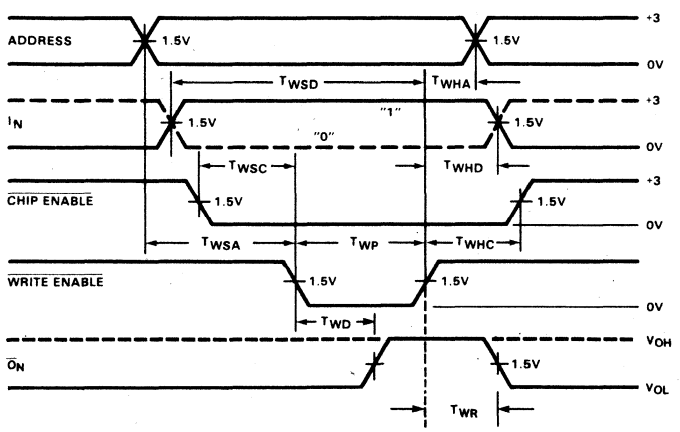


Address Access Time



Chip Enable/Disable Times

WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{CE}	Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
T_{CD}	Delay between when Chip Enable becomes high and Data Output is in off state.
T_{AA}	Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
T_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
T_{WHD}	Required delay between end of Write Enable pulse and end of valid Input Data.
T_{WP}	Width of Write Enable pulse.
T_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
T_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
T_{WD}	Delay between beginning of Write Enable pulse and when Data Output goes high.
T_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
T_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.
T_{WR}	Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming address still valid.)

DESCRIPTION

The 82S10/11, with a typical access time of 30ns, is ideal for cache buffer applications and for systems requiring very high speed main memory.

The 82S10/11 family requires single +5V power supply and features very low current pnp input structures. They include on-chip decoding and a chip enable input for ease of memory expansion, and feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

All devices are available in the commercial temperature range (0°C to +75°C) and are specified as N82S10/110/11/111. The 82S10 and 82S11 are also available in the military temperature range (-55°C to +125°C) and are specified as S82S10/11.

FEATURES

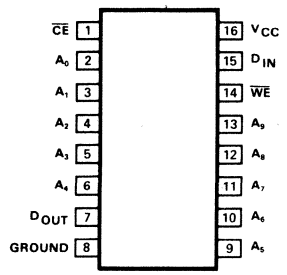
- **Address access time:**
  N82S10/11: 40ns max
  S82S10/11: 60ns max
  N82S110/111: 30ns max
- **Write cycle time:**
  N82S10/11: 40ns max
  S82S10/11: 60ns max
  N82S110/111: 30ns max
- **Power dissipation: 0.5W/bit typ**
- **Input loading:**
  N82S10/11: -250μA max
  S82S10/11: -250μA max
  N82S110/111: -250μA max
- **Output options:**
  82S10/110: Open collector
  82S11/111: Tri-state
- **On-chip address decoding**
- **Non-inverting output**
- **Blanked output during Write**
- **Fully TTL compatible**

APPLICATIONS

- **High speed main frame**
- **Cache memory**
- **Buffer storage**
- **Writable control store**

PIN CONFIGURATION

F,N PACKAGE *



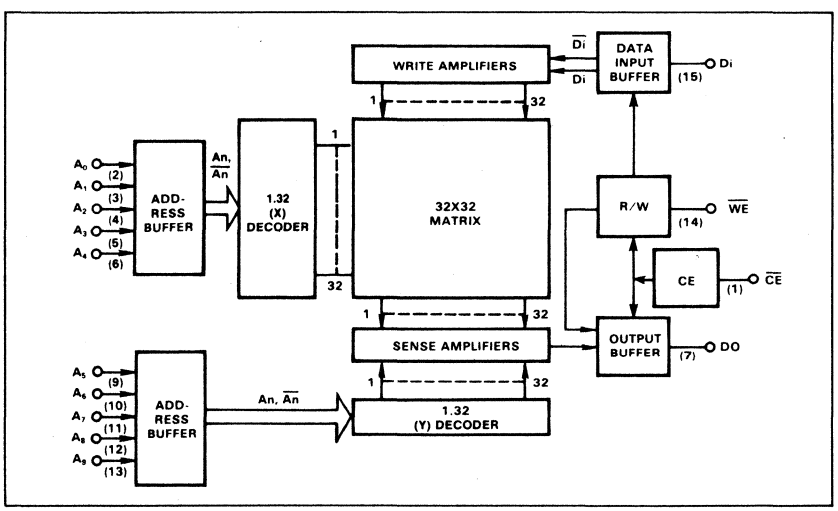
*F = Cerdip
N = Power plastic

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	D	D_{OUT}	
				82S10/110	82S11/111
Read	0	1	X	Stored data	Stored data
Write "0"	0	0	0	1	High-Z
Write "1"	0	0	1	1	High-Z
Disabled	1	X	X	1	High-Z

X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S10/110)	+5.5	
V_O	Off-state (82S11/111)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S10/11/110/111	0 to +75	
	S82S10/11	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS[2]

N82S10/110/11/111: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S10/11: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N82S10/11/110/111			S82S10/11			UNIT
			Min	Typ[3]	Max	Min	Typ[3]	Max	
	Input voltage								V
V_{IL}	Low[1]	V_{CC} = Min			.85			.80	
V_{IH}	High[1]	V_{CC} = Max	2.1			2.1			
V_{IC}	Clamp[1,4]	V_{CC} = Min, I_{IN} = -12mA		-1.0	-1.5		-1.0	-1.5	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[1,5]	I_{OL} = 16mA		0.35	0.45		0.35	0.50	
V_{OH}	High (82S11/111)[1,6]	I_{OH} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		-10	-250		-10	-250	
I_{IH}	High	V_{IN} = 5.5V		1	25		1	40	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage (82S10/110)[7]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S11/111)	V_{OUT} = 5.5V		1	60		1	100	μA
		V_{OUT} = 0.45V[7]		-1	-60		-1	-100	
I_{OS}	Short circuit (82S11/111)[8]	V_{OUT} = 0V	-20		-100	-20		-100	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} = Max							mA
		$0 < T_A < 25°C$		120	155		120	155	
		$T_A \ge 25°C$		95	130		95	130	
		$T_A \le 0°C$			170			170	
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		7			4		
C_{OUT}	Output	V_{OUT} = 2.0V							

AC ELECTRICAL CHARACTERISTICS[2]

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$

N82S10/110/11/111: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

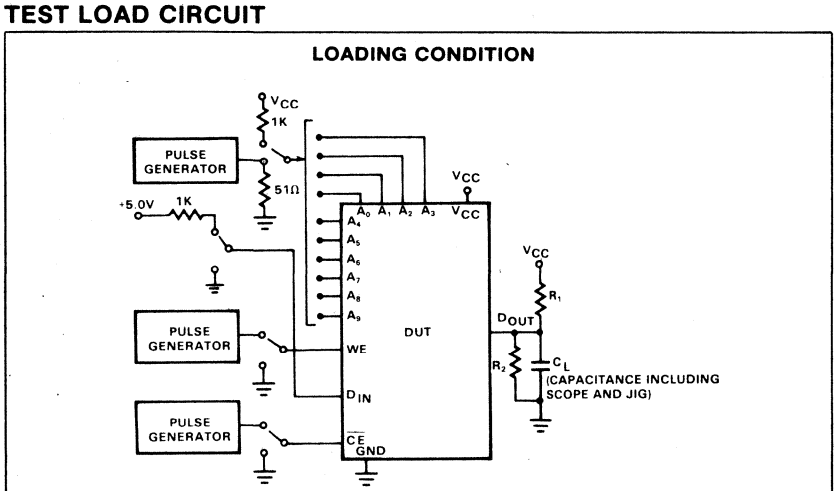
S82S10/11: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S10/11			N82S110/111			S82S10/11			UNIT
			Min	Typ[3]	Max	Min	Typ	Max	Min	Typ[3]	Max	
Access time												ns
T_{AA} Address				30	40			30		30	60	
T_{CE} Chip enable				15	30			25		15	45	
Disable time												ns
T_{CD}	Output	Chip enable		15	30			25		15	45	
T_{WD}	Output	Write enable		20	30			20		20	45	
T_{WR} Write recovery time				20	30			25		20	45	ns
Setup and hold time												ns
T_{WSA} Setup time	Write enable	Address	5	0		5			15	0		
T_{WHA} Hold time			5	0		5			10	0		
T_{WSD} Setup time	Write enable	Data in	30	25		25			55	35		
T_{WHD} Hold time			5	0		5			5	0		
T_{WSC} Setup time	Write enable	$\overline{CE}$	5	0		5			5	0		
T_{WHC} Hold time												
Pulse width												ns
T_{WP} Write enable[10]			30	25		20			50	25		

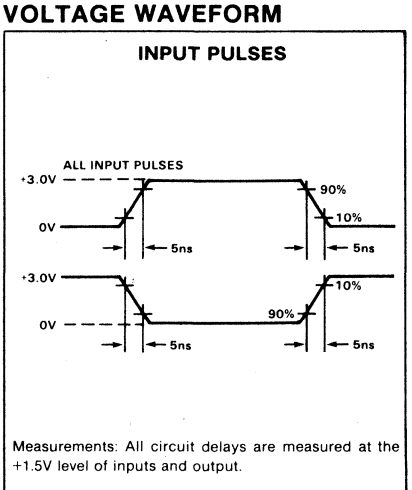
NOTES

1. All voltage values are with respect to network ground terminal.
2. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.
   Typical thermal resistance values of the package at maximum temperature are:
   Θ_{JA} junction to ambient at 400fpm air flow - 50°C/watt
   Θ_{JA} junction to ambient - still air - 90°C/watt
   Θ_{JA} junction to case - 20°C/watt
3. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
4. Test each input one at a time.
5. Measured with a logic low stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
7. Measured with V_{IH} applied to $\overline{CE}$.
8. Duration of the short circuit should not exceed 1 second.
9. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
10. Minimum required to guarantee a Write into the slowest bit.

TEST LOAD CIRCUIT

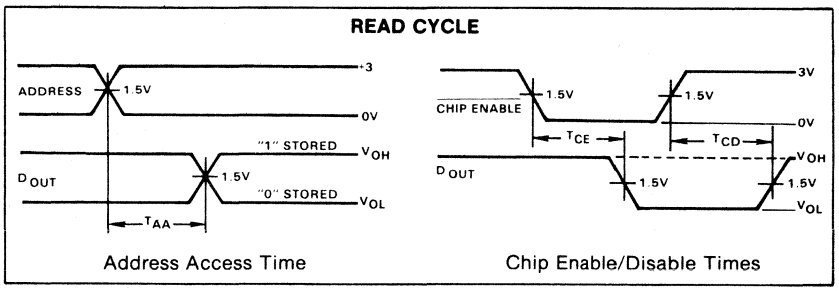


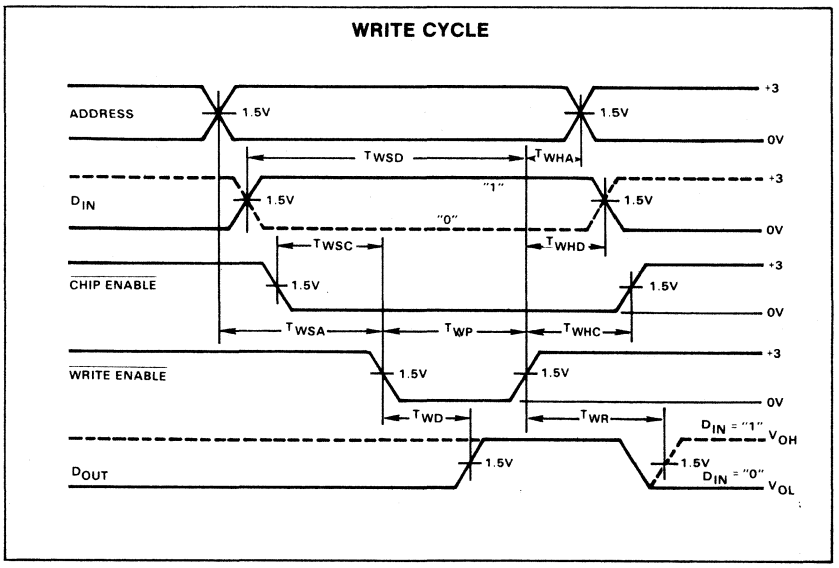
VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

TIMING DIAGRAMS





MEMORY TIMING DEFINITIONS

T_{WR}	Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming Address still valid—not as shown.)
T_{CE}	Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
T_{CD}	Delay between when Chip Enable becomes high and Data Output is in off state.
T_{AA}	Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
T_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
T_{WHD}	Required delay between end of Write Enable pulse and end of valid Input Data.
T_{WP}	Width of Write Enable pulse.
T_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
T_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
T_{WD}	Delay between beginning of Write Enable pulse and when Data Output is in off state.
T_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
T_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.

DESCRIPTION

This family of low power 1024x1 Rams with a typical access time of 30ns, are ideal for cache buffer applications and for systems requiring very high speed main memory.

These products require a single +5V power supply and feature very low current pnp input structures. They include on-chip decoding and a chip enable input for ease of memory expansion, and feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

All devices are available in the commercial temperature range (0°C to +75°C), and military temperature range (-55°C to +125°C).

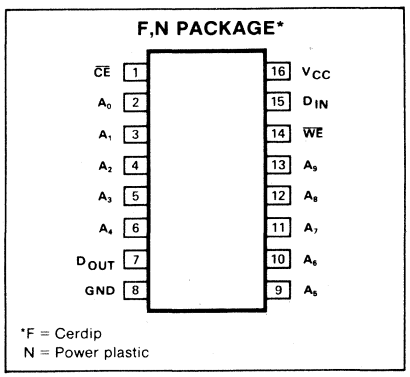
FEATURES

- **Address access time: 45ns max**
- **Write cycle time: 45ns max**
- **Power dissipation: 0.2mW/bit typ**
- **Input loading: -250μA max**
- **On-chip address decoding**
- **Output options:**
  - **82LS10, 93L415: Open collector**
  - **82LS11, 93L425: Tri-state**
- **Non-inverting output**
- **Blanked output during Write**
- **Fully TTL compatible**

APPLICATIONS

- **High speed main frame**
- **Cache memory**
- **Buffer storage**
- **Writable control store**

PIN CONFIGURATION



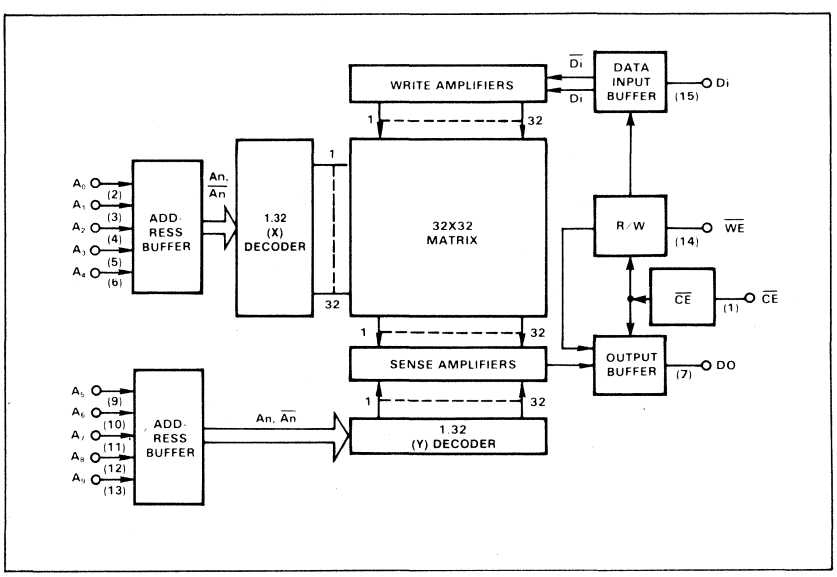
*F = Cerdip
N = Power plastic

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	D_{IN}	D_{OUT}	
				82LS10/93L415	82LS11/93L425
Read	0	1	X	Stored data	Stored data
Write low	0	0	0	1	High-Z
Write high	0	0	1	1	High-Z
Disabled	1	X	X	1	High-Z

X = Don't care

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High 82LS10/93L415	+5.5	
V_O	Off-state 82LS11/93L425	+5.5	
	Temperature range		°C
T_A	Operating		
	N Grade	0 to +75	
	S Grade	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS[9]

N Grade: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S Grade: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N82LS10/11 N93L415/425			S82LS10/11 S93L415/425			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low[1]	V_{CC} = Min			.85			.80	
V_{IH}	High[1]	V_{CC} = Max	2.1			2.1			
V_{IC}	Clamp[1,3]	V_{CC} = Min, I_{IN} = -12mA		-1.0	-1.5		-1.0	-1.5	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[1,4]	I_{OL} = 16mA		0.35	0.45		0.35	0.50	
V_{OH}	High (Tri-state)[1,5]	I_{OH} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		-10	-250		-10	-250	
I_{IH}	High	V_{IN}= 5.5V		1	25		1	40	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage (Open collector)[6]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (Tri-state)[6]	V_{OUT} = 5.5V		1	60		1	100	μA
		V_{OUT} = 0.45V		-1	-60		-1	-100	
I_{OS}	Short circuit (Tri-state)[7]	V_{OUT} = 0V	-20		-100	-20		-100	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max							mA
		$0 < T_A < 25°C$							
		$T_A \ge 25°C$							
		$T_A \le 0°C$			65			75	
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		7			4		
C_{OUT}	Output	V_{OUT} = 2.0V							

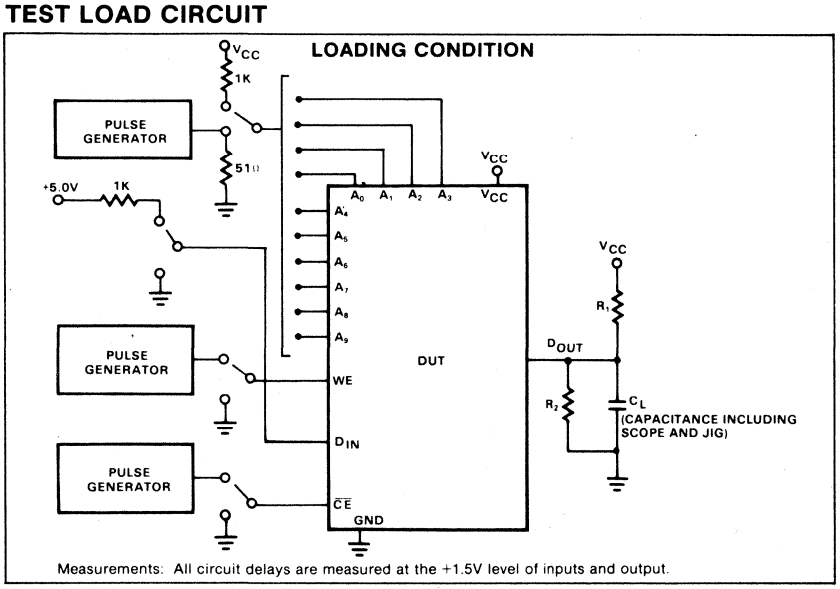
AC ELECTRICAL CHARACTERISTICS[9]

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, See ac test load
N Grade: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S Grade: $-55°C \leq T_A + 125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER	TO	FROM	N82LS10 N82LS11			S82LS10 S82LS11			N93L415 N93L425			S93L415 S93L425			
			Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time															ns
T_{AA} Address	Output	Address		30	45		30	70		30	60			70	
T_{CE} Chip enable	Output	Chip enable		15	30		15	45			40			45	
T_{CD} Disable time	Output	Chip enable		15	30		15	45			40			50	ns
T_{WD} Response time	Output	Write enable		20	30		20	45			45			45	ns
T_{WR} Write recovery time				20	30		20	45			45			55	ns
Setup and hold time															ns
T_{WSA} Setup time	Write	Address	5	0		10	0		5	0		10			
T_{WHA} Hold time	enable		5	0		10	0		5	0		10			
T_{WSD} Setup time	Write	Data in	40	30		55	35		50			60			
T_{WHD} Hold time	enable		5	0		5	0		5			10			
T_{WSC} Setup time	Write	CE	5			5			5			10			
T_{WHC} Hold time	enable		5	0		5	0		5			10			
Pulse width															ns
T_{WP} Write enable[10]			35	25		50	25		45			50			

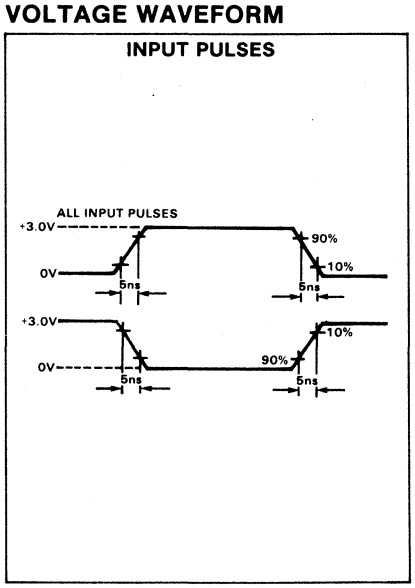
NOTES
1. All voltage values are with respect to network ground terminal.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Test each input one at a time.
4. Measured with a logic low stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Duration of the short circuit should not exceed 1 second.
8. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA} junction to ambient at 400fpm air flow-50°C/watt
   θ_{JA} junction to ambient-still air-90°C/watt
   θ_{JA} junction to case-20°C/watt
10. Minimum required to guarantee a Write into the slowest bit.

TEST LOAD CIRCUIT

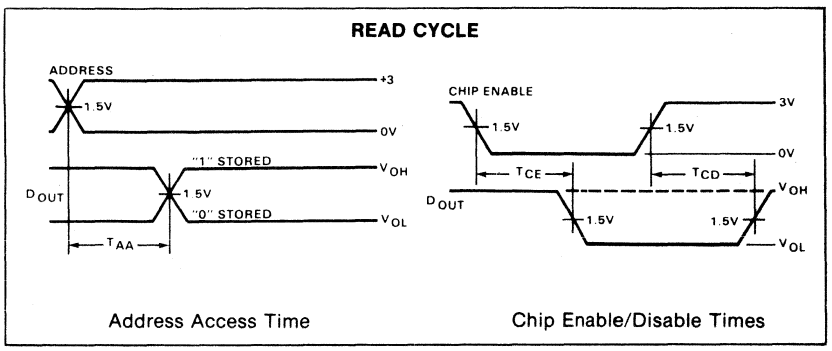


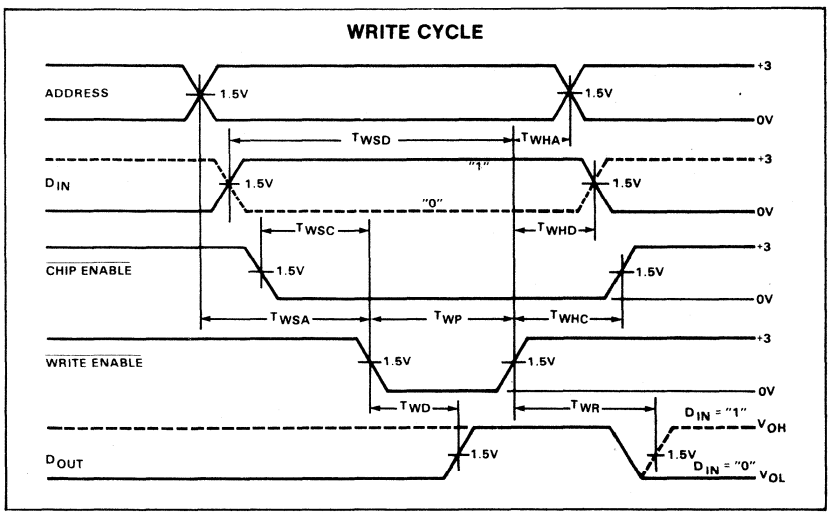
Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

VOLTAGE WAVEFORM



TIMING DIAGRAMS





MEMORY TIMING DEFINITIONS

T_{WR}	Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming Address still valid—not as shown.)
T_{CE}	Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
T_{CD}	Delay between when Chip Enable becomes high and Data Output is in off state.
T_{AA}	Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
T_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
T_{WHD}	Required delay between end of Write Enable pulse and end of valid Input Data.
T_{WP}	Width of Write Enable pulse.
T_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
T_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
T_{WD}	Delay between beginning of Write Enable pulse and when Data Output is in off state.
T_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
T_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.

DESCRIPTION

The 82S208 and 82S210 data inputs and outputs are common (common I/O) with separate output disable (OD) line that allows ease of read/write operations using a common bus.

The address inputs have a latch feature controlled by a latch control pin ($\overline{L}$). In the transparent mode, the $\overline{L}$ pin is held high and the read or write location is accessed directly from the address inputs. In the Latched mode, a negative transition on the $\overline{L}$ line causes the present address state to be held in the address latches, independent of any other control signals. A positive pulse on the $\overline{L}$ line will cause a new address state to be strobed into the latches.

FEATURES

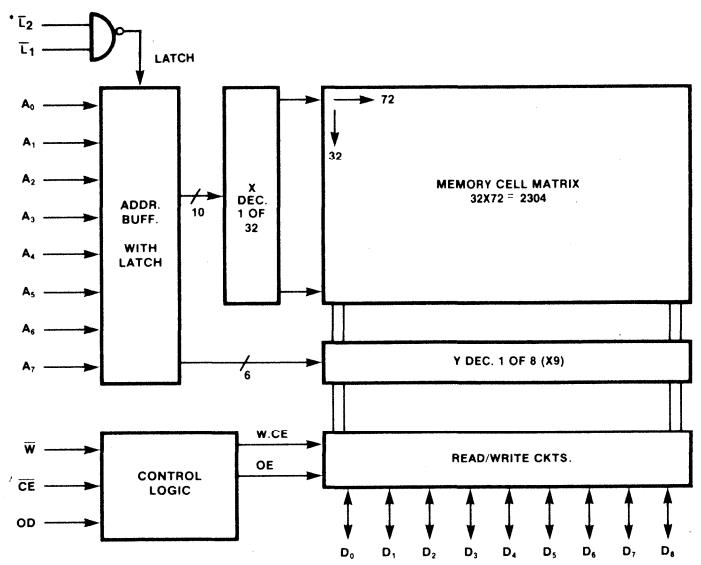
- **Access time:**
  Address: 60ns max
  Strobe: 70ns max
- **On-chip address latches**
- **Tri-state outputs**
- **Schottky clamped TTL**

TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CE}$	OD	$\overline{L}_1$	$\overline{L}_2$*	D_N IN/OUT
Disable output	X	X	1	X	X	High Z
Disable R/W	X	1	X	X	X	High Z
Write	0	0	1	X	X	Data in
Read	1	0	0	X	X	Data out
Transparent address	X	X	X	1	1	—
Hold address	X	X	X	0	X	—
	X	X	X	X	0	—

X = Don't care
*V_{IH} Applied internally on 82S208.

BLOCK DIAGRAM

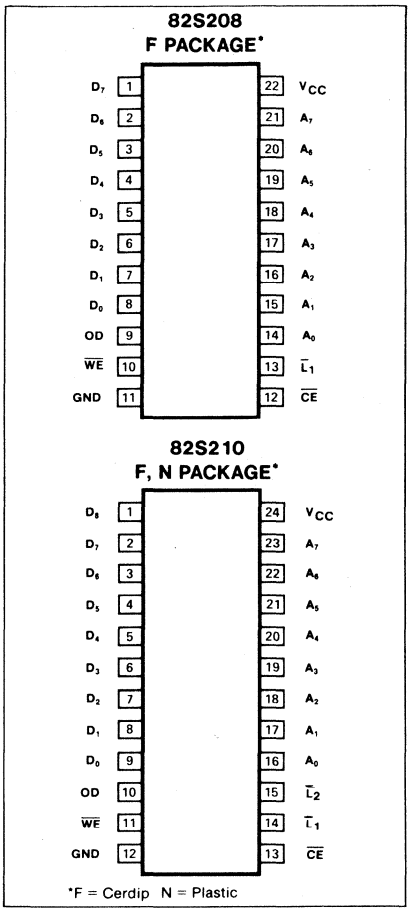


*V_{IH} Applied internally on 82S208.

ABSOLUTE MAXIMUM RATINGS

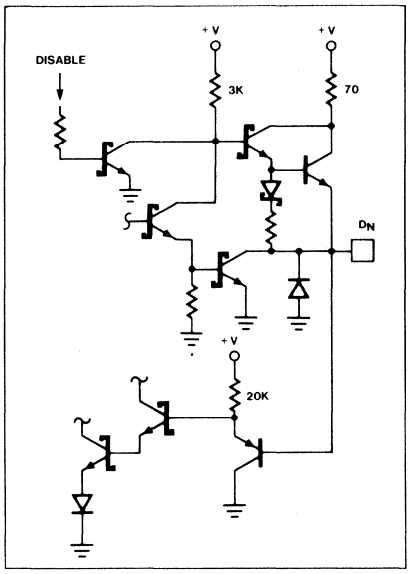
	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_O	Off-state output voltage	+5.5	Vdc
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	−65 to +150	

PIN CONFIGURATION



*F = Cerdip N = Plastic

TYPICAL I/O STRUCTURE



DC ELECTRICAL CHARACTERISTICS[1] $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
	Input voltage[2]					V
V_{IL}	Low				.85	
V_{IH}	High		2.0			
V_{IC}	Clamp[4]	$I_{IN} = -12mA$		−0.8	−1.2	
	Output voltage[2]					V
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.5	
V_{OH}	High	$I_{OUT} = -2mA$	2.4	3.3		
	Input current					μA
I_{IL}	Low	$V_{IN} = 0.45V$			−100	
I_{IH}	High	$V_{IN} +5.5V$			25	
	Output current					
$I_{O(OFF)}$	Hi-Z state	$V_{OUT} = 5.5V$			40	μA
		$V_{OUT} = 0.5V$			−100	
I_{OS}	Short circuit[4,5]	$V_{OUT} = 0V$	−20		−70	mA
I_{CC}	Supply current			135	185	mA
	Capacitance	$V_{CC} = 5.0V$				pF
C_{IN}	Input	$V_{IN} = 2.0V$		5		
C_{OUT}	Output	$V_{OUT} = 2.0V$, $\overline{CE}$ = High, OD = High		8		

AC ELECTRICAL CHARACTERISTICS[1] $0°C \leq T_A \leq 75°C$, $4.75V \leq V_{CC} \leq 5.25V$

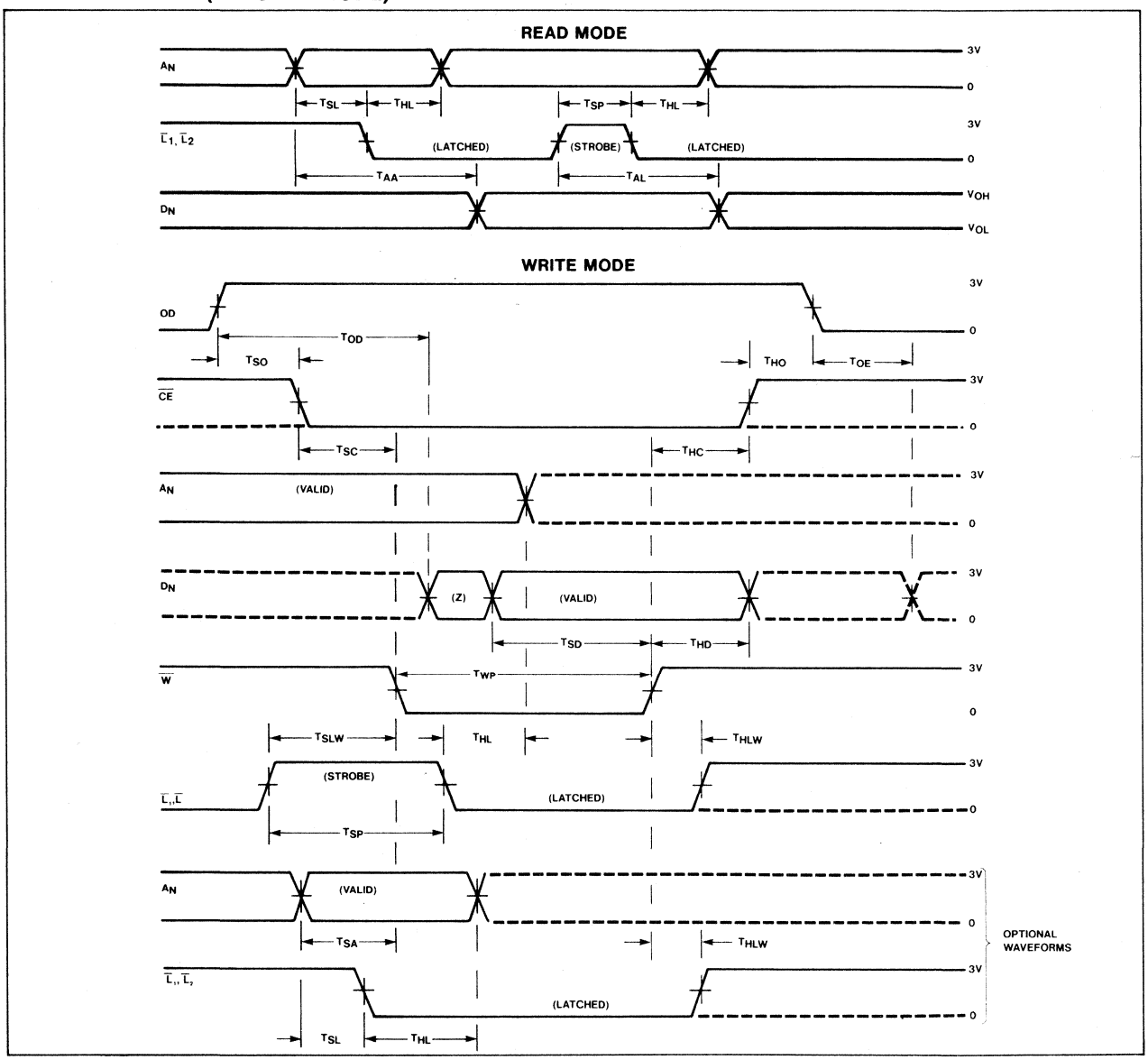
PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ[3]	Max	
T_{AA}	Address access time	D_N	A_N			60	ns
T_{OE}	Output enable time	D_N	OD	5		35	ns
T_{CE}	Output enable time	D_N	$\overline{CE}$			35	
T_{OD}	Output disable time	D_N	OD			35	ns
T_{CD}	Output disable time	D_N	$\overline{CE}$			35	
T_{WP}	Write pulse width		$\overline{W}$	40			ns
T_{SA}	Address setup time	$\overline{W}$	A_N	10			ns
T_{HA}	Address hold time	A_N	$\overline{W}$	10			
T_{SD}	Data setup time	$\overline{W}$	D_N	35			ns
T_{HD}	Data hold time	D_N	$\overline{W}$	10			
T_{SC}	Chip enable setup time	$\overline{W}$	$\overline{CE}$	5			ns
T_{HC}	Chip enable hold time	$\overline{CE}$	$\overline{W}$	5			
T_{SO}	OD setup time	$\overline{CE}$	OD	5			ns
T_{HO}	OD hold time	OD	$\overline{CE}$	5			
(To guarantee High Z state during entire write cycle)							

NOTES
1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warmup.
2. All voltages are with respect to network ground terminal.
3. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
4. Measured on one pin at a time.
5. Duration of test should not exceed one second.

AC CHARACTERISTICS $0°C \leq T_A \leq 75°C$, $4.75V \leq V_{CC} \leq 5.25V$

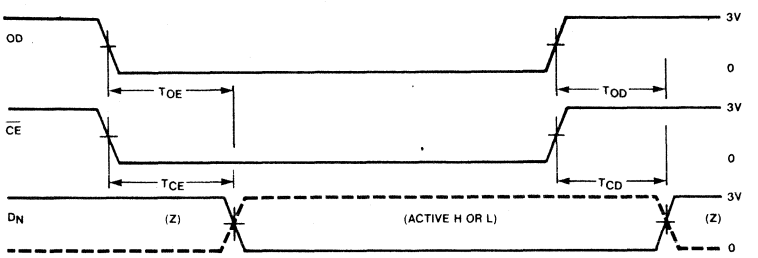
PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ[3]	Max	
T_{SP}	Strobe pulse width		$\overline{L}$	20			ns
T_{SL}	Latch setup time	$\overline{L}$	A_N	5			ns
T_{HL}	Latch hold time	A_N	$\overline{L}$	10			
T_{SLW}	Strobe setup time	$\overline{W}$	$\overline{L}$	15			ns
T_{HLW}	Latch hold after write	$\overline{L}$	$\overline{W}$	10			
T_{AL}	Strobe access time	D_N	$\overline{L}$			70	ns

TIMING DIAGRAMS (LATCHED MODE)

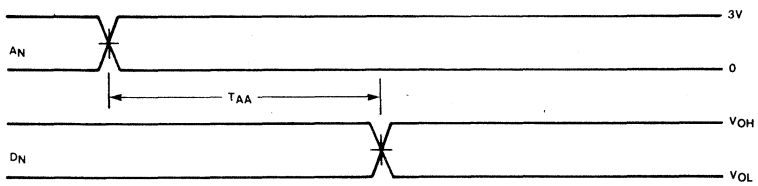


TIMING DIAGRAMS (TRANSPARENT MODE $\overline{L1} = \overline{L2} = 1$)

ENABLE / DISABLE

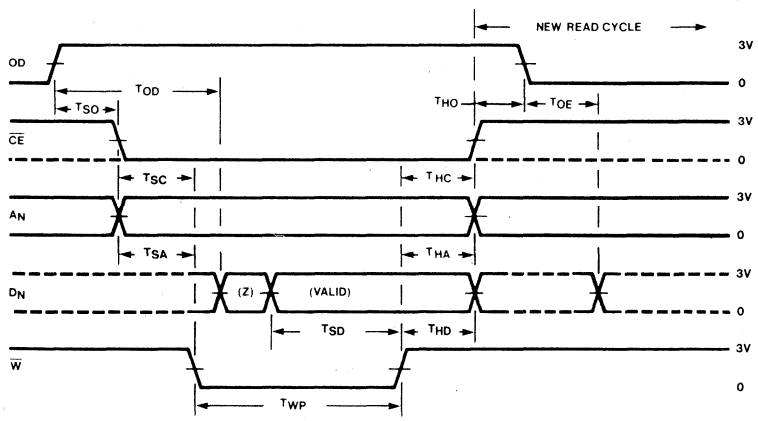


READ MODE



NOTE
(Z) Denotes High Z state

WRITE MODE



CAUTION = Data Bus conflict can occur with $\overline{CE} = 0$. Apply Data source after T_{OD} (max.) and remove Data Source before T_{OE} (min.).

OBJECTIVE SPECIFICATION 82S212-F

DESCRIPTION

The organization of this device allows byte manipulation of data, including parity. Where parity is not monitored, the ninth bit can be used as a flag or status indicator for each word stored. With a typical access time of 30ns, it is ideal for scratch-pad, pushdown stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S212 data inputs and outputs are common (common I/O) with separate output disable (OD) line that allows ease of read/write operations using a common bus.

FEATURES

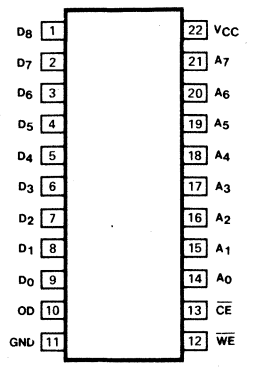
- **Address access time: 45ns max**
- **Power dissipation: 0.3 mW/bit**
- **Tri-state outputs**
- **Schottky clamped TTL**

APPLICATIONS

- **Cache memory**
- **Buffer storage**
- **Writable control store**

PIN CONFIGURATION

F PACKAGE*



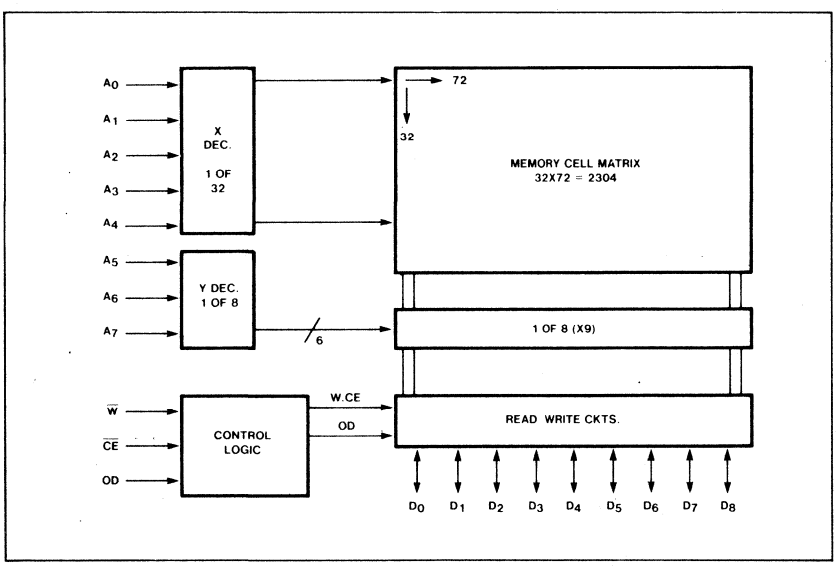
*F = Cerdip

TRUTH TABLE

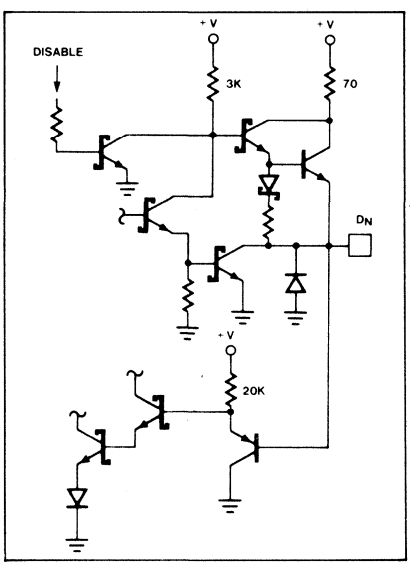
MODE	$\overline{WE}$	$\overline{CE}$	OD	D_N IN/OUT
Disable output	X	X	1	High Z
Disable R/W	X	1	X	High Z
Write	0	0	1	Data in
Read	1	0	0	Data out

X = Don't care

BLOCK DIAGRAM



TYPICAL I/O STRUCTURE



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_O	Off-state output voltage	+5.5	Vdc
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS[1] $0°C \leq T_A \leq 75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS[2]			UNIT
			Min	Typ[3]	Max	
	Input voltage[2]					V
V_{IL}	Low				.85	
V_{IH}	High		2.0			
V_{IC}	Clamp[4]	$I_{IN} = -12mA$		−0.8	−1.2	
	Output voltage[2]					V
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.5	
V_{OH}	High	$I_{OUT} = -2mA$	2.4	3.3		
	Input current					μA
I_{IL}	Low	$V_{IN} = 0.45V$			−100	
I_{IH}	High	$V_{IN} = 5.5V$			25	
	Output current					
$I_{O(OFF)}$	Hi-Z state	$V_{OUT} = 5.5V$			40	μA
		$V_{OUT} = 0.5V$			−100	
I_{OS}	Short circuit[4,5]	$V_{OUT} = 0V$	−20		−70	mA
I_{CC}	Supply current			135	185	mA
	Capacitance	$V_{CC} = 5.0V$				pF
C_{IN}	Input	$V_{IN} = 2.0V$		5		
C_{OUT}	Output	$V_{OUT} = 2.0V$, $\overline{CE}$ = High, OD = High		8		

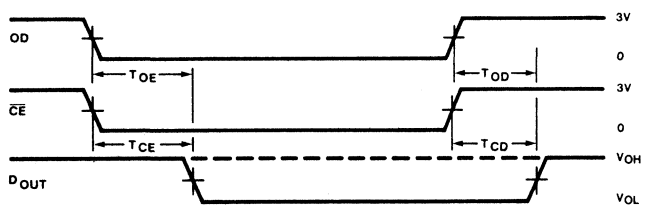
AC ELECTRICAL CHARACTERISTICS[1] $0°C \leq T_A \leq 75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ[3]	Max	
	Access time						ns
T_{AA}	Address	Output	Address			45	
	Enable time						ns
T_{OE}	Output	Output	OD	5		25	
T_{CE}	Output	Output	Chip enable			25	
	Disable time						ns
T_{OD}	Output	Output	OD			25	
T_{CD}	Output	Output	Chip enable			25	
	Pulse width						ns
T_{WP}	Write			25			
T_{WSC}	Setup time	Write	Chip enable	5			
T_{WHD}	Hold time	Chip enable	Write	5			
T_{WSD}	Setup time	Write	Data	25			
T_{WHD}	Hold time	Data	Write	5			
T_{WSA}	Setup time	Write	Address	5			
T_{WHA}	Hold time	Address	Write	5			
T_{SO}	Setup time (from disabled state)	Chip enable	OD	5			
T_{HO}	Hold time	OD	Chip enable	5			

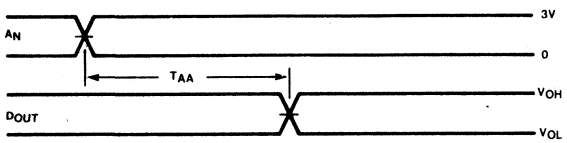
NOTES
1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warmup.
2. All voltages are with respect to network ground terminal.
3. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
4. Measured on one pin at a time.
5. Duration of I_{OS} test should not exceed one second.

TIMING DIAGRAMS

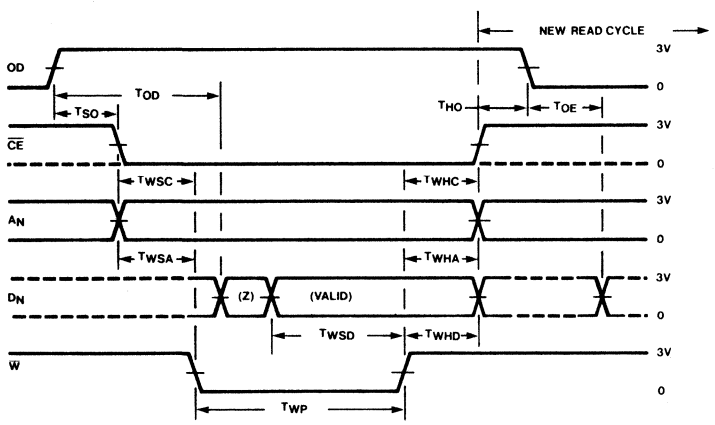
ENABLE/DISABLE



READ MODE



WRITE MODE



CAUTION = Data Bus conflict can occur with $\overline{CE}$ = 0, apply data source after T_{OD} (max.) and remove data source before T_{OE} (min.).

PRELIMINARY SPECIFICATION 8X350-F

DESCRIPTION

The 8X350 bipolar RAM is designed principally as a working storage element in an 8X300 based system. Internal circuitry is provided for direct use in 8X300 applications. When used with the 8X300, the RAM address and data buses are tied together and connected to the IV bus of the system.

The data inputs and outputs share a common I/O bus with 3-state outputs. The address inputs can be operated in a transparent or latched mode.

The 8X350 is available in commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N8X350-F, and for the military temperature range (−55°C to +125°C) specify S8X350-F.

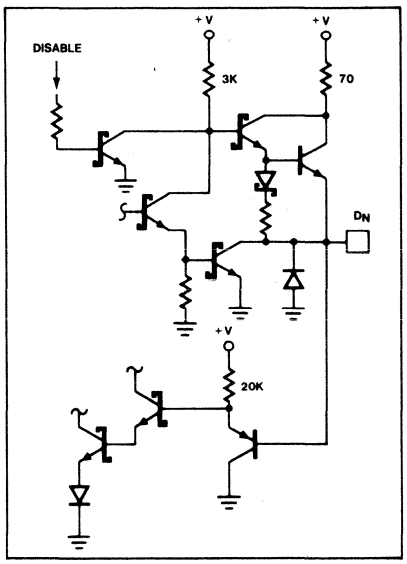
FEATURES

- **On-chip address latches**
- **3-state outputs**
- **Schottky clamped TTL**
- **Internal control logic for 8X300 system**
- **Directly interfaces with the 8X300 bipolar microprocessor with no external logic**

APPLICATIONS

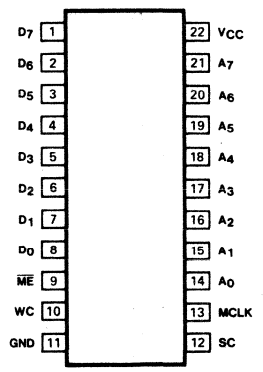
- **8X300 working storage**

TYPICAL I/O STRUCTURE



PIN CONFIGURATION

F PACKAGE



ABSOLUTE MAXIMUM RATINGS

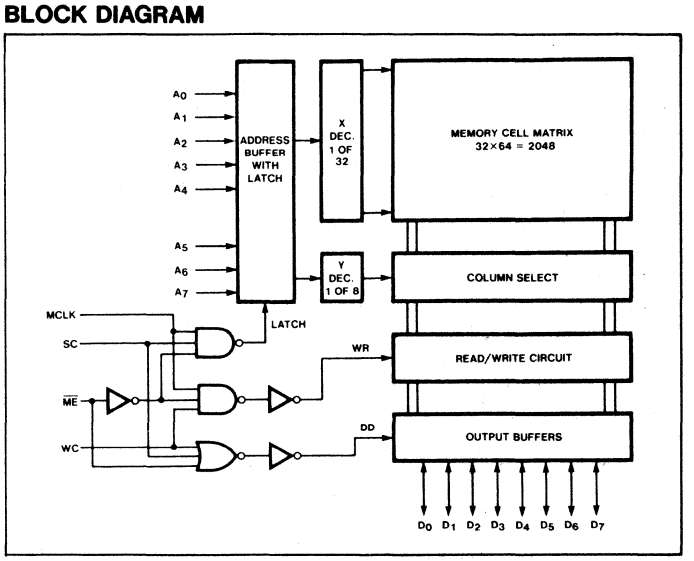
	PARAMETER[1]	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High	+5.5	
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	N8X350	0 to +75	
	S8X350	−55 to +125	
T_{STG}	Storage	−65 to +150	

TRUTH TABLE

Note X = Don't care

MODE	$\overline{ME}$	SC	WC	MCLK	BUSSED DATA/ADDRESS LINES
Hold address Disable data out	1	X	X	X	High Z data out
Input new address	0	1	0	1	Address
Hold address Disable data out	0	1	0	0	High Z data out
Hold address Write data	0	0	1	1	Data in
Hold address Disable data out	0	0	1	0	High Z data out
Hold address Read data	0	0	0	X	Data out
Undefined state[13]	0	1	1	1	—
Hold address[13] Disable data out	0	1	1	0	High Z data out

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS[2]

N8X350: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S8X350: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TEST CONDITIONS	N8X350			S8X350			UNIT
			Min	Typ[3]	Max	Min	Typ[3]	Max	
	Input voltage								V
V_{IL}	Low[1]	V_{CC} = Min			.85			.80	
V_{IH}	High[1]	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp[1,4]	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2		−.8	−1.2	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[1,5]	I_{OL} = 9.6mA		0.35	0.5			.5	
V_{OH}	High[1,6]	I_{OH} = −2mA	2.4	3.3		2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100			−150	
I_{IH}	High	V_{IN} = 5.5V			25			50	
	Output current								
$I_{O(OFF)}$	High Z state	V_{OUT} = 5.5V			40			60	μA
		V_{OUT} = 0.5 V[7]			−100			−100	μA
I_{OS}	Short circuit[4,7]	V_{OUT} = 0V	−20		−70	−15		−85	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		135	185			185	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		
		$\overline{ME}$ = V_{IH}							

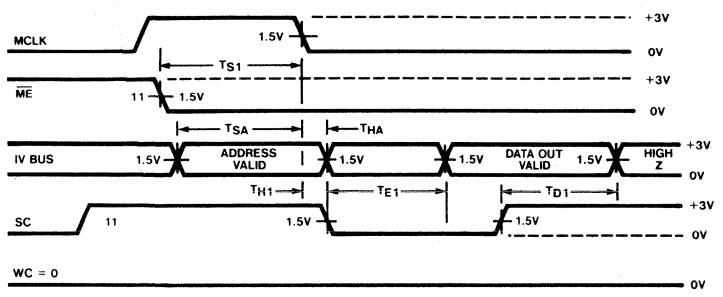
AC ELECTRICAL CHARACTERISTICS[2,10]

N8X350: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S8X350: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

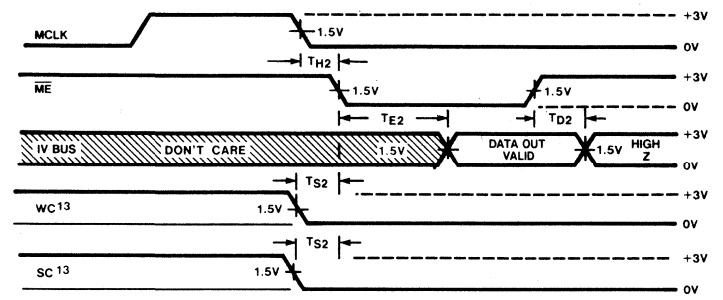
PARAMETER		TO	FROM	N8X350			S8X350			UNIT
				Min	Typ[3]	Max	Min	Typ[3]	Max	
	Enable time									ns
T_{E1}	Output	Data out	SC−			35			40	
T_{E2}	Output	Data out	$\overline{ME}$−			35			40	
	Disable time									ns
T_{D1}	Output	Data out	SC+			35			40	
T_{D2}	Output	Data out	$\overline{ME}$+			35			40	
	Pulse width									ns
T_W	Master clock[9]			40			50			
	Setup and hold time									ns
T_{SA}	Setup time	MCLK−	Address	30			40			
T_{HA}	Hold time	Address	MCLK−	5			10			
T_{SD}	Setup time	MCLK−	Data in	35			45			
T_{HD}	Hold time	Data in	MCLK−	5			10			
T_{S3}	Setup time	MCLK−	$\overline{ME}$−	40			50			
T_{H3}	Hold time	$\overline{ME}$+	MCLK−	5			5			
T_{S1}	Setup time	MCLK−	$\overline{ME}$−	30			40			
T_{H2}	Hold time	$\overline{ME}$−	MCLK−	5			5			
T_{S2}	Setup time	$\overline{ME}$−	SC−,WC−	0			5			
T_{H1}	Hold time	SC−	MCLK−	5			5			
T_{H4}	Hold time	WC−	MCLK−	5			5			

TIMING DIAGRAMS

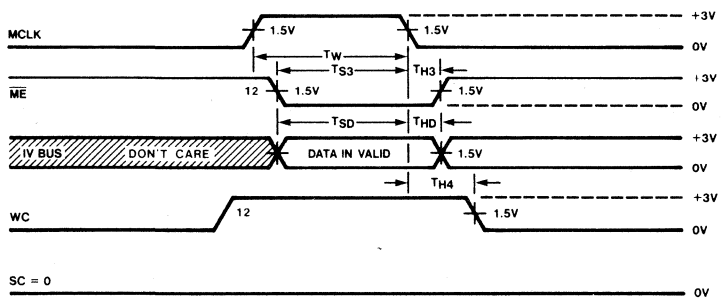
TRANSPARENT ADDRESS READ CYCLE



LATCHED ADDRESS READ CYCLE



LATCHED ADDRESS WRITE CYCLE



NOTES

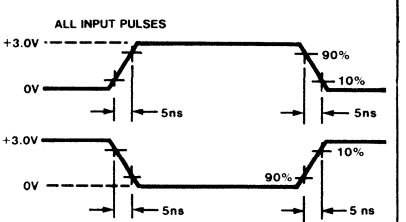
1. All voltage values are with respect to network ground terminal.
2. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.
   Typical thermal resistance values of the package at maximum temperature are:
   Θ_{JA} junction to ambient at 400fpm air flow - 50°C/watt
   Θ_{JA} junction to ambient - still air - 90°C/watt
   Θ_{JA} junction to case - 20°C/watt
3. All typical values are at V_{CC} = 5V, T_A = 25°C.
4. Test each pin one at a time.
5. Measured with a logic low stored Output sink current is supplied through a resistor to V_{CC}.
6. Measured with a logic high stored.
7. Duration of the short circuit should not exceed 1 second.
8. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V and the output open.
9. Minimum required to guarantee a Write into the slowest bit.
10. Applied to the 8X300 based system with the data and address pins tied to the IV Bus.
11. SC + $\overline{ME}$ = 1 to avoid bus conflict.
12. WC + $\overline{ME}$ = 1 to avoid bus conflict.
13. The SC and WC outputs from the 8X300 are never at 1 simultaneously.

TIMING DEFINITIONS

T_{S1}	Required delay between beginning of Master Enable low and falling edge of Master Clock.
T_{SA}	Required delay between beginning of valid address and falling edge of Master Clock.
T_{HA}	Required delay between falling edge of Master Clock and end of valid Address.
T_{H1}	Required delay between falling edge of Master Clock and when Select Command becomes low.
T_{E1}	Delay between beginning of Select Command low and beginning of valid data output on the IV Bus.
T_{D1}	Delay between when select Command becomes high and end of valid data output on the IV Bus.
T_{H2}	Required delay between falling edge of Master Clock and when Master Enable becomes low.
T_{E2}	Delay between when Master Enable becomes low and beginning of valid data output on the IV Bus.
T_{D2}	Delay between when Master Enable becomes high and end of valid data output on the IV Bus.
T_{S2}	Required delay between when Select Command or Write Command becomes low and when Master Enable becomes low.
T_W	Minimum width of the Master Clock pulse.
T_{S3}	Required delay between when Master Enable becomes low and falling edge of Master Clock.
T_{H3}	Required delay between falling edge of Master Clock and when Master Enable becomes high.
T_{SD}	Required delay between beginning of valid data input on the IV Bus and falling edge of Master Clock.
T_{HD}	Required delay between falling edge of Master Clock and end of valid data input on the IV Bus.
T_{H4}	Required delay between falling edge of Master Clock and when Write Command becomes low.

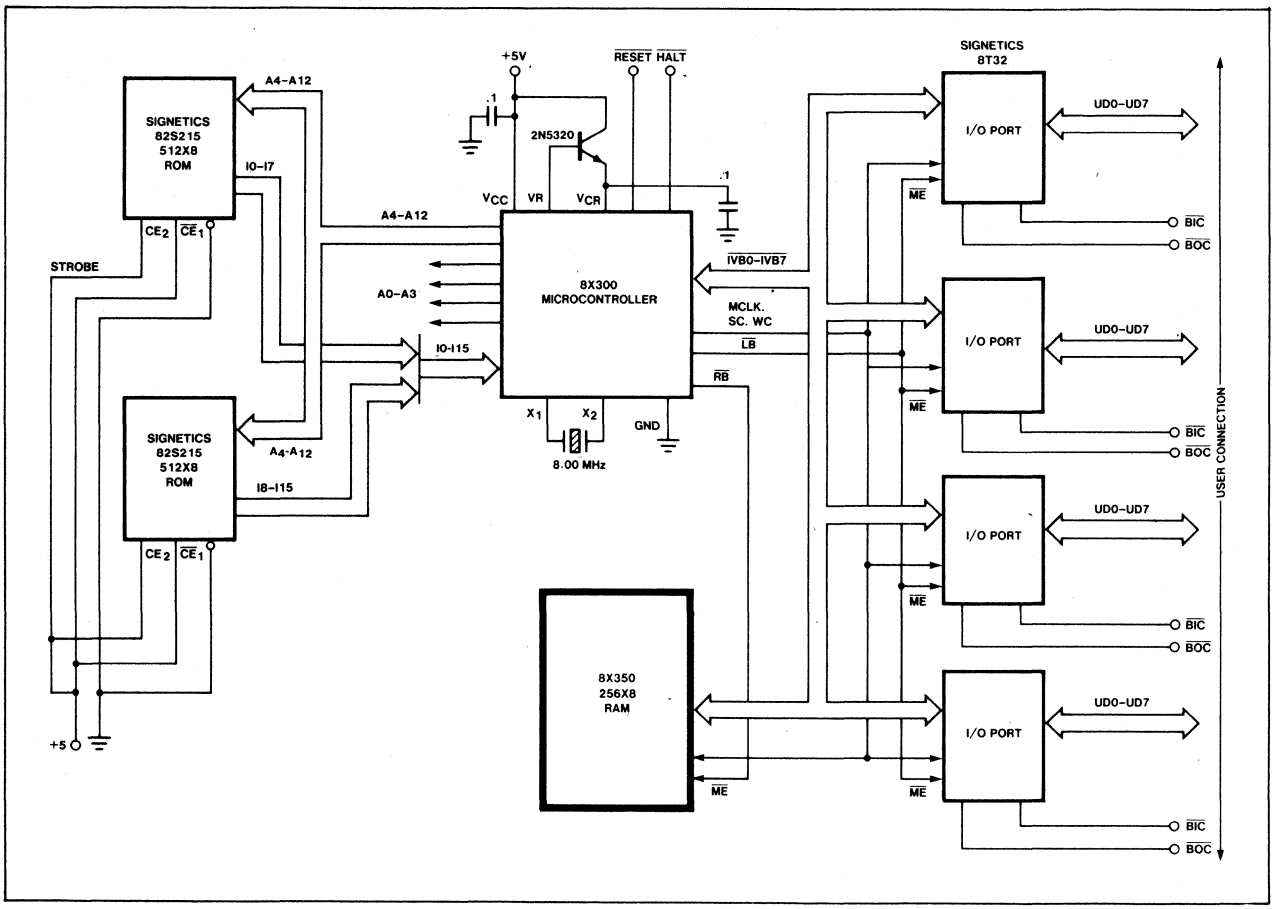
VOLTAGE WAVEFORM

INPUT PULSES



Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

TYPICAL 8X350 APPLICATION



DESCRIPTION

The 82S400 and 82S401, with maximum access time of 45ns, are ideal for cache buffer applications and for systems requiring very high speed main memory. The 82S400 and 82S401 are speed compatible with industry standard 1024 - bit RAMs having 45ns access time.

Both devices require a single +5V power supply, feature very low current pnp input structures, and include on-chip decoding and a chip enable input for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

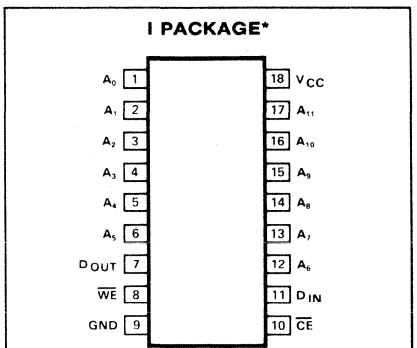
APPLICATIONS

- **High speed main frame**
- **Cache memory**
- **Buffer storage**
- **Writable control store**

FEATURES

- **Address access time:**
  82S400/401: 45ns max
- **Write cycle time: 45ns max**
- **Power dissipation: 0.12mW/bit typ**
- **Input loading: -150μA max**
- **On-chip address decoding**
- **Output options:**
  82S400: Open collector
  82S401: Tri-state
- **Non-inverting output**
- **Blanked output during Write**
- **Fully TTL compatible**

PIN CONFIGURATION



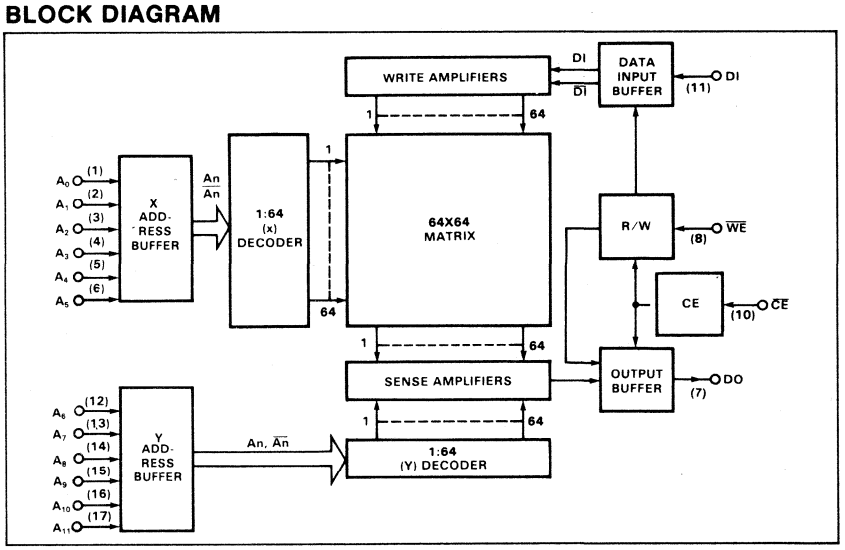
*I = Ceramic

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	D_{IN}	D_{OUT}	
				82S400	82S401
Read	0	1	X	Stored data	Stored data
Write "0"	0	0	0	1	High-Z
Write "1"	0	0	1	1	High-Z
Disabled	1	X	X	1	High-Z

X = Don't care

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S400)	+5.5	
V_O	Off-state (82S401)	+5.5	
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS[10] $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low[1]	V_{CC} = Min			.85	
V_{IH}	High[1]	V_{CC} = Max	2.0			
V_{IC}	Clamp[1,3]	V_{CC} = Min, I_{IN} = -12mA		-1.0	-1.5	
	Output voltage	V_{CC} = Min				V
V_{OL}	Low[1,4]	I_{OL} = 16mA		0.35	0.45	
V_{OH}	High (82S401)[1,5]	I_{OH} = -2mA	2.4			
	Input current					μA
I_{IL}	Low	V_{IN} = 0.45V		-25	-150	
I_{IH}	High	V_{IN} = 5.5V		1	25	
	Output current	V_{CC} = Max				
I_{OLK}	Leakage (82S400)[6]	V_{OUT} = 5.5V		1	40	μA
$I_{O(OFF)}$	Hi-Z state (82S401)[6]	V_{OUT} = 5.5V		1	60	μA
		V_{OUT} = 0.45V		-1	-60	
I_{OS}	Short circuit (82S401)[7]	V_{OUT} = 0V	-20		-100	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max				mA
		$0 < T_A < 25°C$		120	155	
		$T_A \ge 25°C$		105	130	
	Capacitance	V_{CC} = 5.0V				pF
C_{IN}	Input	V_{IN} = 2.0V		4		
C_{OUT}	Output	V_{OUT} = 2.0V		7		

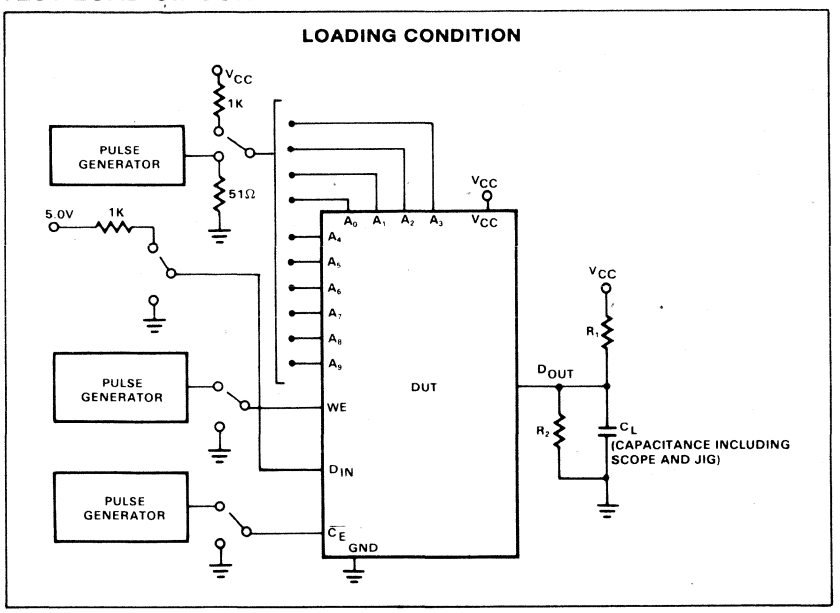
AC ELECTRICAL CHARACTERISTICS[10] $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$, $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$

PARAMETER		TO	FROM	N82S400/401			UNIT
				Min	Typ[2]	Max	
	Access time						ns
T_{AA}		Output	Address			45	
T_{CE}		Output	Chip enable			30	
	Disable time						ns
T_{CD}		Output	Chip enable			30	
T_{WD}		Output	Write enable			30	
T_{WR}	Recovery time	Output	Write enable			30	ns
	Setup and hold time						ns
T_{WSA}	Setup time	Write enable	Address	5			
T_{WHA}	Hold time						
T_{WSD}	Setup time	Write enable	Data in	35			
T_{WHD}	Hold time			5			
T_{WSC}	Setup time	Write enable	CE	5			
T_{WHC}	Hold time						
	Pulse width[9]						ns
T_{WP}	Write enable			35			

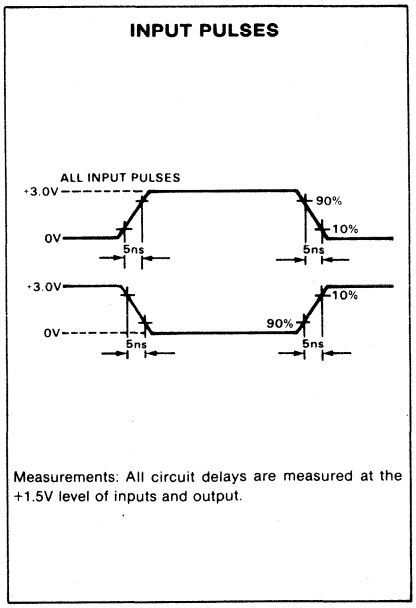
NOTES

1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A 25°C.
3. Test each input one at a time.
4. Measured with a logic low stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Duration of the short circuit should not exceed 1 second.
8. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.
10. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
    Θ_{JA} junction to ambient at 400fpm air flow - 50°C/watt
    Θ_{JA} junction to ambient - still air - 90°C/watt
    Θ_{JA} junction to case - 20°C/watt

TEST LOAD CIRCUIT

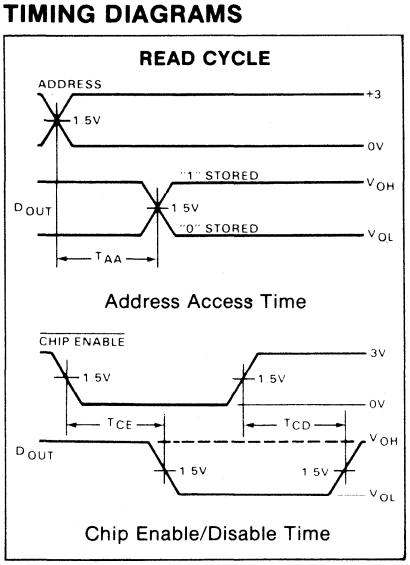


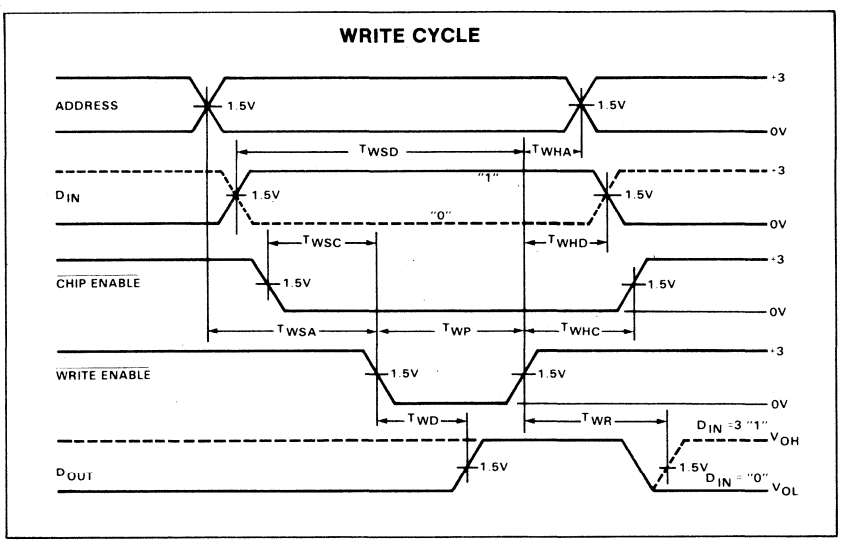
VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

TIMING DIAGRAMS





TIMING DEFINITIONS

T_{WR} Delay between end of Write Enable pulse and when Data Output becomes valid (assuming Address still valid—not as shown).

T_{CE} Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.

T_{CD} Delay between when Chip Enable becomes high and Data Output is in off state.

T_{AA} Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.

T_{WSC} Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.

T_{WHD} Required delay between end of Write Enable pulse and end of valid Input Data.

T_{WP} Width of Write Enable pulse.

T_{WSA} Required delay between beginning of valid Address and beginning of Write Enable pulse.

T_{WSD} Required delay between beginning of valid Data Input and end of Write Enable pulse.

T_{WD} Delay between beginning of Write Enable pulse and when Data Output is in off state.

T_{WHC} Required delay between end of Write Enable pulse and end of Chip Enable.

T_{WHA} Required delay between end of Write Enable pulse and end of valid Address.

DESCRIPTION

The 82S290 and 82S291 include on-chip decoding and 3 programmable chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S290 and 82S291 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S290/291, F or N, and for the military temperature range (-55°C to +125°C) specify S82S290/291, F.

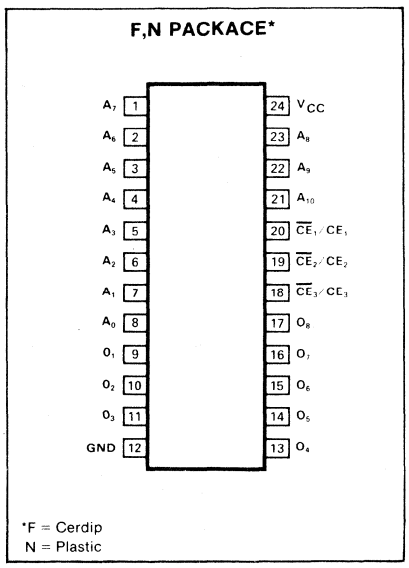
FEATURES

- **Address access time:**
  N82S290/291: 80ns max
  S82S290/291: 100ns max
- **Power dissipation: 40μW/bit typ**
- **Input loading:**
  N82S290/291: -100μA max
  S82S290/291: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S290: Open collector
  82S291: Tri-state
- **Fully compatible with Signetics 82S190/191 PROMs**
- **Fully TTL compatible**

APPLICATIONS

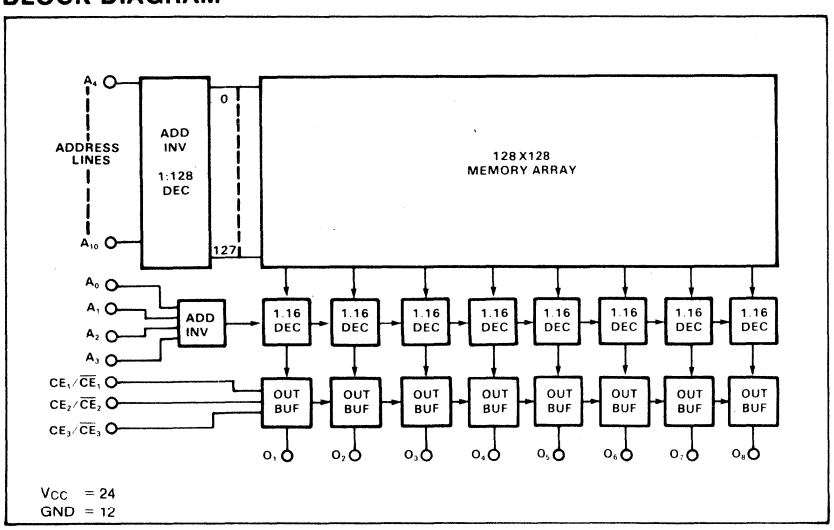
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



*F = Cerdip
N = Plastic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S290)	+5.5	
V_O	Off-state (82S291)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S290/291	0 to +75	
	S82S290/291	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S290/291: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S290/291: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	N82S290/291			S82S290/291			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 9.6mA			0.45			0.5	
V_{OH}	High (82S291)	$\overline{CE}$ = Low, I_{OUT} = -2.4mA, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}	Leakage (82S290)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S291)	$\overline{CE}$ = High, V_{OUT} = 0.5V			-40			-60	μA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			40			60	
I_{OS}	Short circuit (82S291)	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			130	170		130	180	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

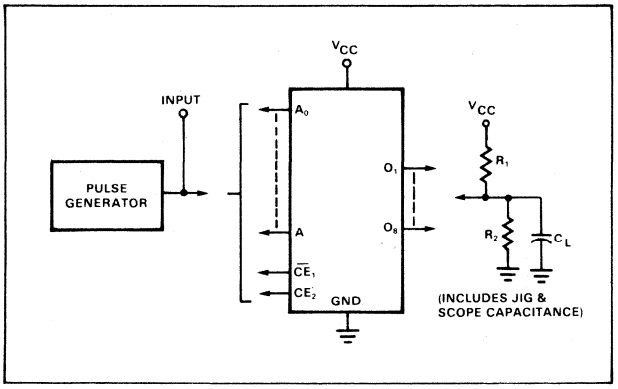
$R_1 = 270\Omega$, $R_2 = 600\Omega$, C_L = 30pF[1]
N82S290/291: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S290/291: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S290/291			S82S290/291			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time									ns
T_{AA}	Output	Address		70	110		70	100	
T_{CE}	Output	Chip enable		20	50		20	50	
Disable time									ns
T_{CD}	Output	Chip disable		20	50		20	50	

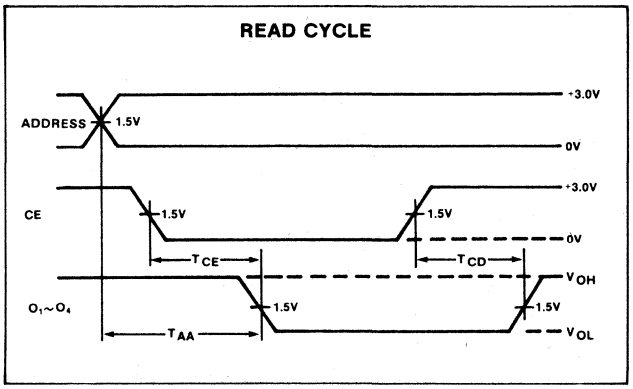
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



PROGRAMMING INFORMATION

Programming Equipment for Signetics PROMs

Programming equipment is available from several manufacturers, including Curtis Enterprises, Data I/O, and Pro-Log. Choice of equipment varies from manual duplicators to fully automatic programmers which read paper tape coded in a variety of formats.

For more information, contact Signetics Memory Marketing or any of the following programmer manufacturers:

Curtis Enterprises
P.O. Box 4090
Mountain View, Calif. 94040
(415) 964-3136

Data I/O Corporation
P.O. Box 308
Issaquah, Washington 98027

Pro-Log Corporation
2411A Garden Road
Monterey, Calif. 93940
(408) 372-4593

CURTIS ELECTRO DEVICES REFERENCE

PROM TYPE	ORGANIZATION	OUTPUTS	MANUAL PROGRAMMER	DUPLICATOR
8223	32X8	OC	PR-23B or PR-1369A	PR-2300
82S23	32X8	OC	PR-1369A	PR-2300S
82S123	32X8	TS	PR-1369A	PR-2300S
82S27	256X4	OC	PR-27	PR-2700S
82S126	256X4	OC	PR-1369A or PR-1269	PR
82S129	256X4	TS	PR-1369A or PR-1269	PR-2600SA
82S114	256X8	TS	PR-145	PR-1145
82S115	512X8	TS	PR-145	PR-1145
82S130	512X4	OC	PR-1369A	PR-2600SA
82S131	512X4	TS	PR-1369A	PR-2600SA
10139	32X8	(ECL)	PR-10139	—

PRO-LOG 90 SERIES REFERENCE

		GENERIC MODULE PM9059	
PROM TYPE	ORGANIZATION	CONFIGURATOR	PIN ADAPTER
82S23	32X8	L	PA16-2
82S123	32X8	L	PA16-2
82S126	256X4	L	PA16-1
82S129	256X4	L	PA16-1
82S130	512X4	L	PA16-1
82S131	512X4	L	PA16-1
82S114	256X8	SI	PA24-9
82S115	512X8	SI	PA24-9
82S140	512X8	L	PA24-8
82S141	512X8	L	PA24-8
82S136	1024X4	L	PA18-2
82S137	1024X4	L	PA18-2
82S184	2048X4	L	PA18-2
82S185	2048X4	L	PA18-2
82S180	1024X8	L	PA24-8
82S181	1024X8	L	PA24-8
82LS180	1024X8	L	PA24-8
82LS181	1024X8	L	PA24-8
82S182	1024X8	L	PA24-8
82S183	1024X8	L	PA24-8
82S190	2048X8	L	PA24-8
82S191	2048X8	L	PA24-8

DATA I/O
MODEL V UNIVERSAL PROGRAMMER
MODEL IX PORTABLE PROGRAMMER
MODEL X FPLA PROGRAMMER

CONFIGURATION	MANUFACTURERS' PART NO.	DATA I/O PROGRAM CARD SET	PROGRAM SOCKET ADAPTER	PRO-GRAMMED LOGIC LEVEL	READ-ONLY OPTIONS	
					READ-ONLY CARD	READ-ONLY SOCKET ADAPTER
32X8 (FL)	8223	1051-1	1034	VOH	1142	1037
32X8 (FL)	10139 ECL	1051-2	1034	VOH	1142	1037
32X8(FL)	82S23, 82S123	1226-2*	1037	VOH	1142	1037
256X8 (FL)	82S114	1226-2*	1096	VOH	1142	1096
512X8 (FL)	82S115	1226-2*	1097	VOH	1142	1097
256X4 (FL)	10149 ECL	1144-1	1003-4	VOH	1187-13	1003-4
256X4 (FL)	82S126, 82S129	1226-2*	1035-1	VOH	1142	1035
512X4 (FL)	82S130, 82S131	1226-2*	1035-2	VOH	1142	1035
512X8 (FL)	82S140, 82S141	1226-2*	1033-2	VOH	1142	1033
1024X4 (FL)	82S136, 82S137	1226-2*	1039-3	VOH	1142	1039
1024X8 (FL)	82S180, 82S181, 82S2708	1226-2*	1033-3	VOH	1142	1033
1024X8	82LS180, 82LS181, 82S182, 82S183	1226-2*	1033-3	VOH	1142	1033
2048X4 (FL)	82S184, 82S185	1226-2*	1039	VOH	1142	1039
2048X8 (FL)	82S190, 82S191	1226-2*	1033	VOH	1142	1033

*Contact Signetics or Pro-Log

DESCRIPTION

The 82S23 and 82S123 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S23 and 82S123 devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S23 and 82S123 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S23/123, N or F, and for the military temperature range (-55°C to +125°C) specify S82S23/123, F only.

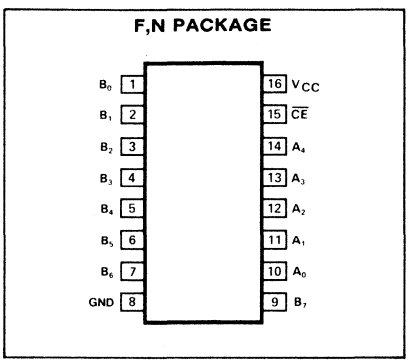
FEATURES

- **Address access time:**
  N82S23/123: 50ns max
  S82S23/123: 65ns max
- **Power dissipation: 1.3mW/bit typ**
- **Input loading:**
  N82S23/123: -100μA max
  S82S23/123: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S23: Open collector
  82S123: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

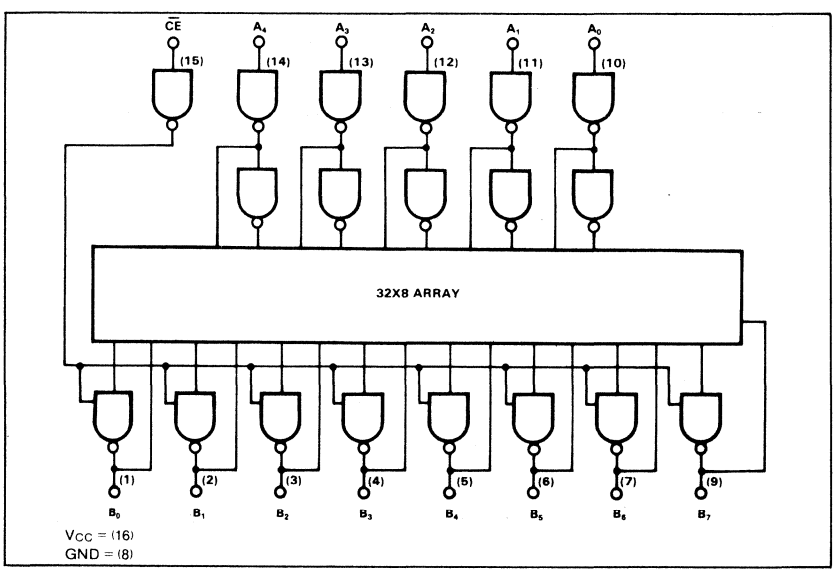
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Format conversion**
- **Hardwired algorithms**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S23)	+5.5	
V_O	Off-state (82S123)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S23/123	0 to +75	
	S82S23/123	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S23/123: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S23/123: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS[1]	N82S23/123			S82S23/123			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				0.85			0.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High	$\overline{CE}$ = Low, I_{OUT} = -2mA, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			50			50	
	Output current								
I_{OLK}	Leakage (82S23)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40			50	μA
$I_{O(OFF)}$	Hi-Z state (82S123)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40			50	μA
		$\overline{CE}$ = High, V_{OUT} = 0.5V			-40			-50	
I_{OS}	Short circuit (82S123)	V_{OUT} = 0V	-20		-90	-20		-100	mA
I_{CC}	V_{CC} supply current			65	77		65	85	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

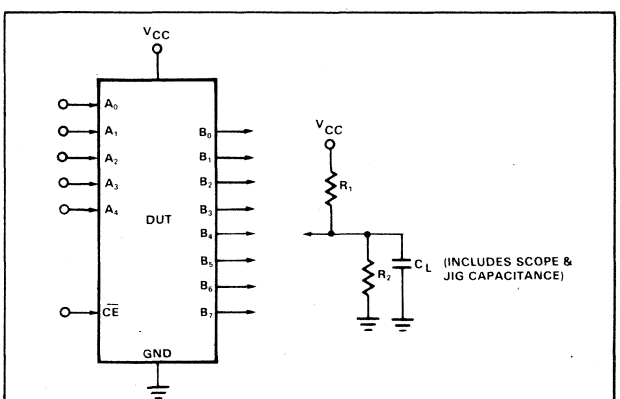
R_1 = 270Ω, R_2 = 600Ω, C_L = 30pF[1]
N82S23/123: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S23/123: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82S23/123			S82S23/123			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time									ns
T_{AA}[3]	Output	Address		35	50		35	65	
T_{CE}	Output	Chip enable		25	35		25	40	
Disable time									ns
T_{CD}	Output	Chip disable		25	35		25	40	

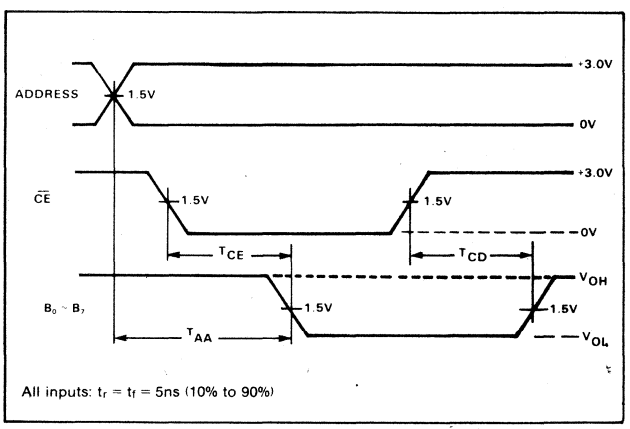
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.
3. Tested at an address cycle time of 1μsec.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



PROGRAMMING SYSTEM SPECIFICATIONS[4] $T_A = 25°C$. (Testing of these limits may cause programming of device.)

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Power supply voltage					V
V_{CCP}	To program[1]	I_{CCP} = 425 ± 75mA, Transient or steady state	8.5		9.0	
	Verify limit					V
V_{CCVH}	Upper		5.3		5.7	
V_{CCVL}	Lower		4.3		4.7	
V_S	Verify threshold[2]		1.4		1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	350		500	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0		0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			-500	
V_{OPF}	Forced output voltage (program)[3]	I_{OPF} = 200 ± 20mA, Transient or steady state	16.0		18.0	V
I_{OPF}	Forced output current (program)	V_{OPF} = +17 ± 1V	180		220	mA
T_R	Output pulse rise time		10			μs
t_P	$\overline{CE}$ programming pulse width		100		125	μs
t_D	Pulse sequence delay		5			μs
t_V	$\overline{CE}$ verify pulse width		1			μs
T_{PVA}	Address program-verify cycle				1	ms
T_{PVM}	Memory program-verify time (continuous)				20	sec
F_L	Fusing attempts per link				1	cycle

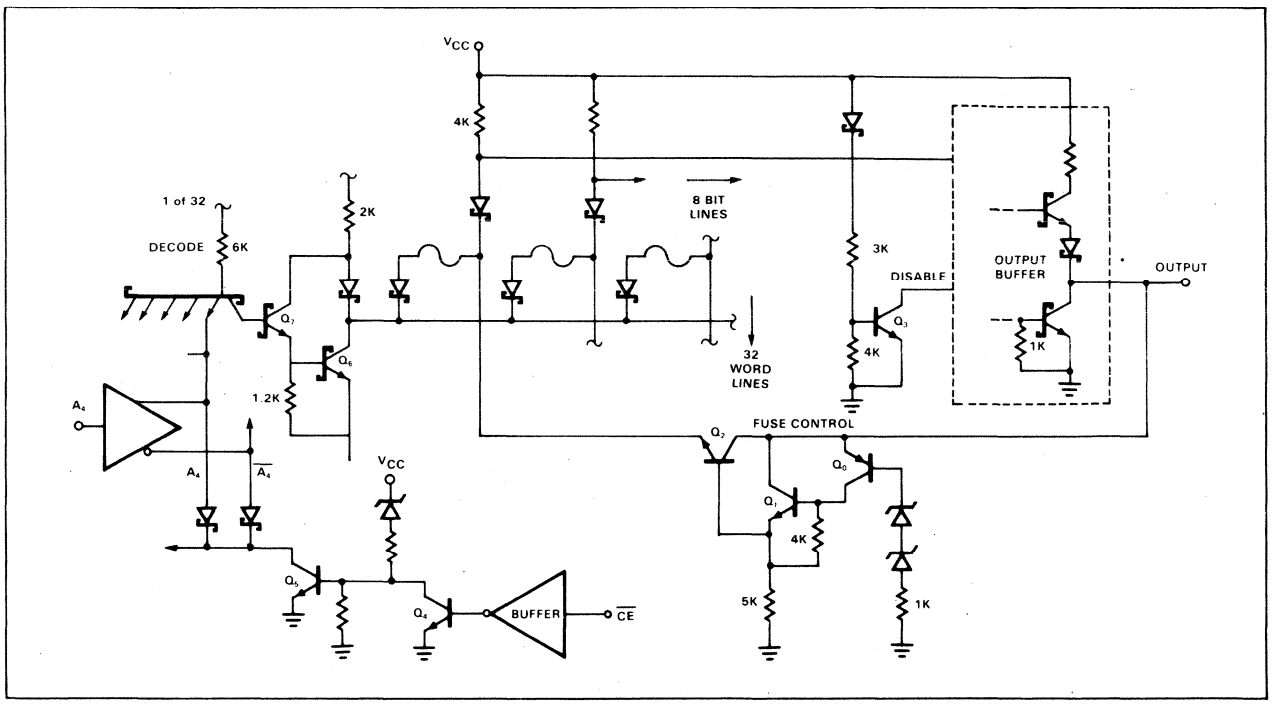
PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150mA, limit voltage spikes to a maximum slew rate of 2V/μs, and 10μs maximum recovery.
4. *These are specifications which a Programming System must satisfy in order to be qualified by* Signetics. They contain new limits for minimizing total device programming time, which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment.

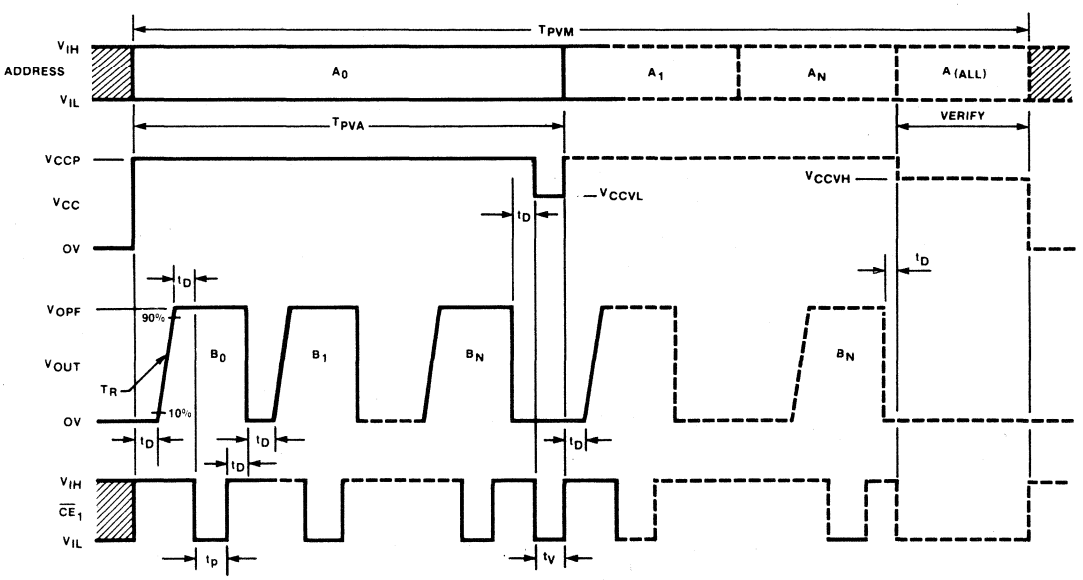
PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE}$ = High.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP}.
3. After t_D delay, apply V_{OPF} to the output to be programmed. Program one output at the time.
4. After t_D delay, pulse the $\overline{CE}$ input to logic low for a time t_P.
5. After t_D delay, remove V_{OPF} from the programmed output.
6. Repeat steps 3 through 5 to program other bits at the same address.
7. To verify programming of all bits at the same address after t_D delay lower V_{CC} to V_{CCVL} and apply a logic low level to the $\overline{CE}$ input. All programmed outputs should remain in the logic high state.
8. After t_D delay, repeat steps 2 through 7 to program and verify all other address locations.
9. After t_D delay raise V_{CC} to V_{CCVH} and verify all memory locations by applying a logic low level to $\overline{CE}$, and cycling through all device addresses.

TYPICAL FUSING PATH



TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

10139-F,N

DESCRIPTION

The 10139 is organized as an array of 32 words and 8 bits. The initial unprogrammed state is 0 (low). The user may program 1's to obtain any desired pattern. Outputs go to the 0 (low) state when the chip enable input is high, allowing wired-OR output connections. A 50Ω output drive capability makes the part suitable for use in high performance ECL systems.

FEATURES

- **Access time: 15ns typ**
- **Power dissipation: 580mW typ**
- **Field programmable (Ni-Cr link)**
- **Fully decoded**
- **High impedance inputs (50kΩ pulldown)**
- **Open emitter outputs (50Ω drive)**
- **Fully compatible with Signetics ECL 10K products**

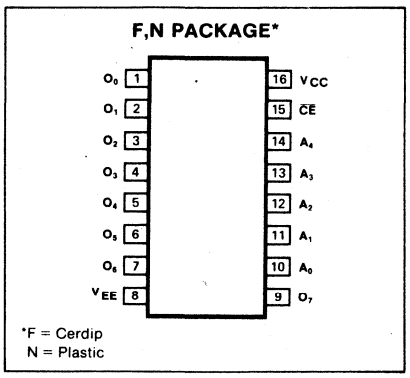
APPLICATIONS

- **Programmable logic**
- **Control stores**
- **Microprogramming**
- **Hardwired algorithms**

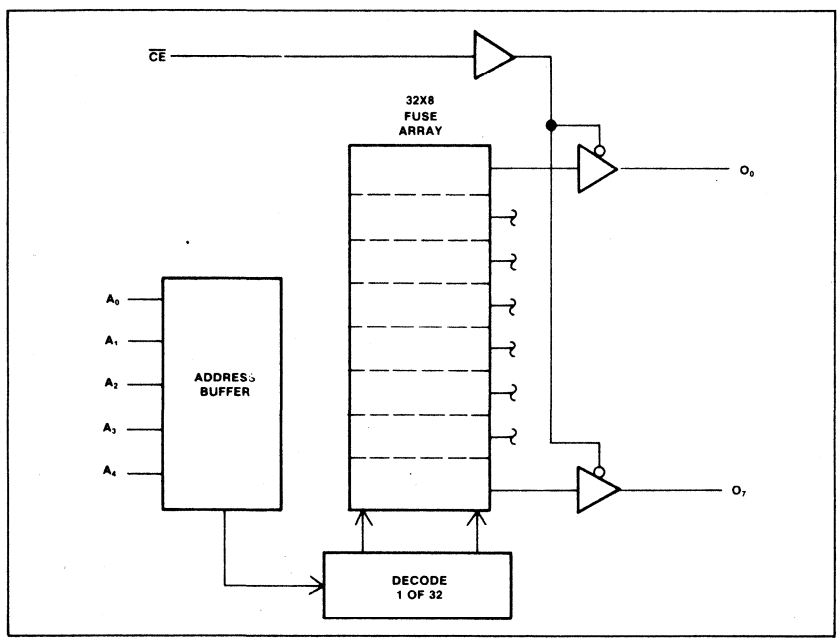
RECOMMENDED OPERATING VOLTAGE

- **V_{CC} = GND, V_{EE} = -5.2V ± 5%**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
T_A	Temperature range Operating	-30 to +85	°C

10139-F,N

DC ELECTRICAL CHARACTERISTICS[1] V_{CC} = 0V, V_{EE} = -5.2V, R_L = 50Ω to -2V

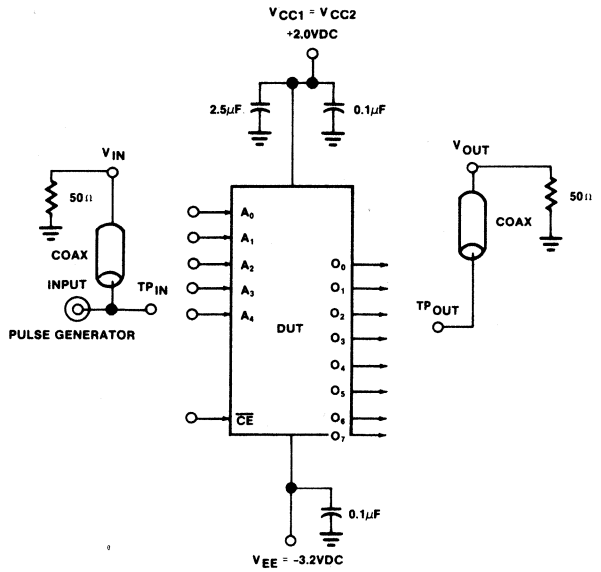
PARAMETER	TEST CONDITIONS	-30°C			+25°C			+85°C			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input voltage											V
V_{IL} Low		-1.890			-1.850			-1.825			
V_{IH} High				-0.890			-0.810			-0.700	
V_{ILA} Low threshold				-1.500			-1.475			-1.440	
V_{IHA} High threshold		-1.205			-1.105			-1.035			
Output voltage											V
V_{OL} Low	V_{IH} = Max, V_{IL} = Min	-1.89		-1.675	-1.85	-1.70	-1.65	-1.825		-1.615	
V_{OH} High		-1.06		-0.89	-0.96	-0.89	-0.81	-0.89		-0.70	
V_{OLA} Low threshold	V_{IHA} = Min, V_{ILA} = Max			-1.655			-1.63			-1.595	
V_{OHA} High threshold		-1.08			-0.98			-0.91			
Input current											μA
I_{IL} Low	V_{IL} = Min				0.5						
I_{IH} High	V_{IH} = Max						265				
I_{EE} Power supply drain current						110	145				mA

AC ELECTRICAL CHARACTERISTICS[1,2] V_{CC} = 2V, R_L = 50Ω to ground, -30°C ≤ T_A ≤ 85°C, V_{EE} = -3.2V

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ	Max	
Access time						ns
T_{AA}	Output	Address		15	22	
T_{CE}	Output	Chip enable		10	17	
Disable time						ns
T_{CD}	Output	Chip disable		10	17	
Rise and fall time						ns
t_+ Rise time (20-80%)				4.0		
t_- Fall time (20-80%)				4.0		

10139-F,N

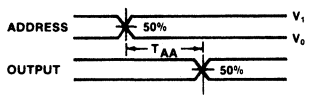
TEST LOAD CIRCUIT



Input pulse: $t_+ = t_- = 2.0 - 0.2$ns (20 to 80%)

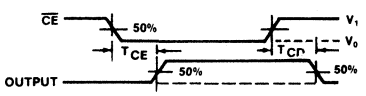
VOLTAGE WAVEFORMS

ADDRESS ACCESS TIME



Input pulse conditions: $V_0 = 0.31V$, $V_1 = 1.11V$, $t_r = 2$ns (20 to 80%), $t_f = 2$ns (20 to 80%)

CHIP ENABLE/DISABLE TIMES

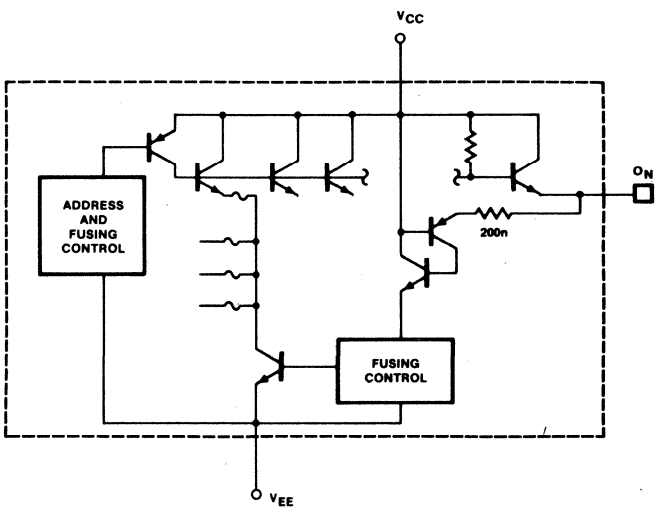


Input pulse conditions: $V_0 = 0.31V$, $V_1 = 1.11V$, $t_r = 2$ns (20 to 80%), $t_f = 2$ns (20 to 80%)

NOTES

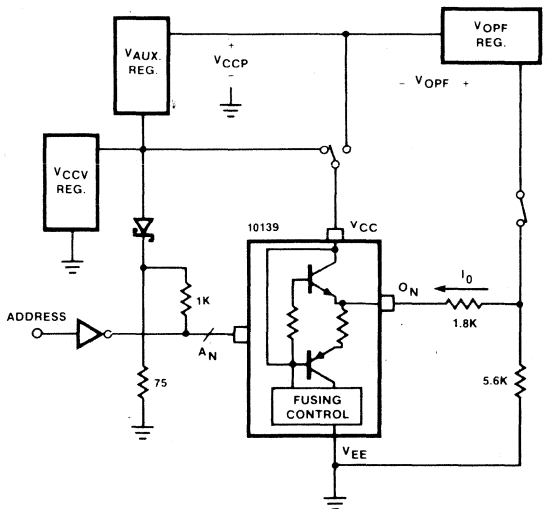
1. Dc and ac specifications apply after thermal equilibrium has been established, with transverse air flow greater than 500 linear ft/min.
2. For ac tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
3. Test procedures are shown for only 1 input or set of input conditions. Other inputs are tested in the same manner.

TYPICAL FUSING PATH

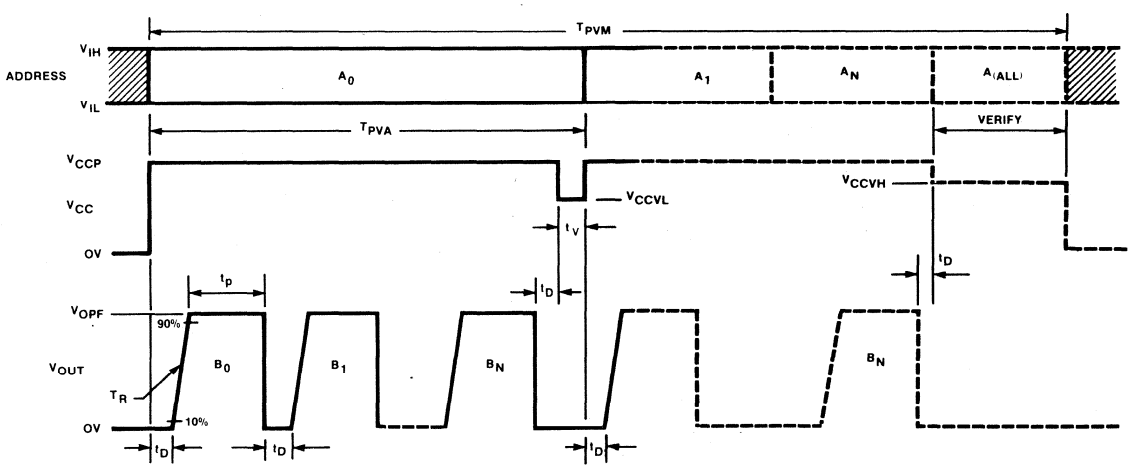


10139-F,N

TYPICAL PROGRAMMING CIRCUIT



PROGRAMMING SEQUENCE



10139-F,N

PROGRAMMING SYSTEM SPECIFICATIONS[4] (Testing of these limits may cause programming of device.) $T_A = +25°C$.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1,3]	I_{CCP} = 300±25mA (Transient or steady state)	11.5		12.5	V
	Verify limit					V
V_{CCVH}	Upper		5.5		5.7	
V_{CCVL}	Lower		4.7		4.9	
V_S	Verify threshold[2]			V_{CCV}		V
I_{CCP}	Programming supply current	V_{CCP} = 12±.5V	275	-1.3	325	mA
	Input voltage[5]		V_{CCV}		V_{CCV}	V
V_{IH}	High		-0.8		-0.2	
V_{IL}	Low		0		0.8	
	Input current					µA
I_{IH}	High	V_{IH} = Max.			300	
I_{IL}	Low	V_{IL} = Min.			-50	
V_{OPF}	Forced Output Voltage[3,6] (program)	I_{OPF} = 2.5±.5mA (Transient or steady state)	6.0		6.8	V
I_{OPF}	Forced Output Current (program)	V_{OPF} = 6.4±.4V	2		3	mA
T_R	Output pulse rise time		0.1		1	µs
t_p	Programming pulse width		100		125	µs
t_D	Pulse sequence delay		10			µs
t_V	Verify time		1			µs
T_{PVA}	Address program-verify cycle				2	ms
T_{PVM}	Memory program-verify time (continuous)				20	sec
F_L	Fusing attempts per link				1	cycle

PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01µF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150mA, limit voltage spikes to a maximum slew rate of 2V/µs, and 10µs maximum recovery.
4. These are specifications which a Programming System must satisfy in order to be qualified by Signetics.
5. Address buffers must be referenced to V_{CCV}.
6. V_{OPF} supply must be referenced to the V_{CCV} supply.

PROGRAMMING PROCEDURE

The 10139 is shipped with all bits at logical "0" (low). To write locical "1", proceed as follows:

SET-UP

a. Set V_{EE} and $\overline{CE}$ to GND.
b. Set V_{CC} to V_{CCVH}.
c. Terminate all device outputs with a 1.8K resistor in series with a 5.6K resistor to GND.

PROGRAM-VERIFY SEQUENCE

1. Select the Address to be programmed, and raise V_{CC} to V_{CCP}.
2. After t_D delay, apply a voltage V_{OPF} to the output to be programmed via the external divider (refer to typical programming circuit). Program one output at a time.
3. After t_p delay, remove V_{OPF} from the programmed output.
4. After t_D delay, repeat steps 2 and 3 to program other bits at the same address.
5. To verify programming of all bits at the same address, after t_D delay lower V_{CC} to V_{CCVH}. All programmed outputs should remain in the logic high state.
6. After t_D delay, repeat steps 1 through 5 to program and verify all other address locations.
7. After t_D delay lower V_{CC} to V_{CCVL}, and verify all memory locations by cycling through all device addresses.

DESCRIPTION

The 82S126 and 82S129 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S126 and 82S129 devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S126 and 82S129 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S126/129, F or N, and for the military temperature range (-55°C to +125°C) specify S82S126/129, F only.

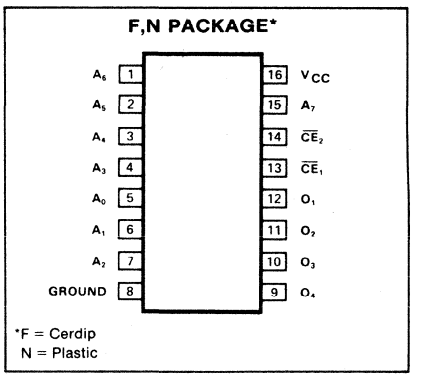
FEATURES

- **Address access time:**
  - **N82S126/129: 50ns max**
  - **S82S126/129: 70ns max**
- **Power dissipation: 0.5mW/bit typ**
- **Input loading:**
  - **N82S126/129: -100μA max**
  - **S82S126/129: -150μA max**
- **On-chip address decoding**
- **Output options:**
  - **82S126: Open collector**
  - **82S129: Tri-state**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

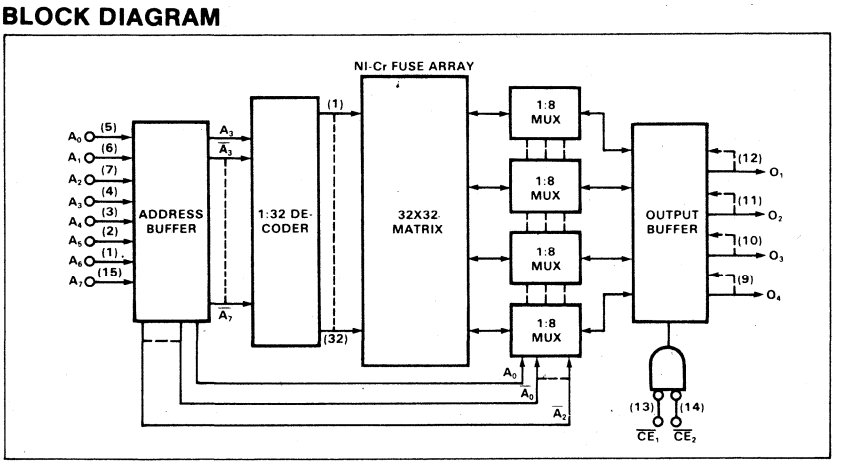
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S126)	+5.5	
V_O	Off-state (82S129)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S126/129	0 to +75	
	S82S126/129	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S126/129: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S126/129: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	N82S126/129			S82S126/129			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High (82S129)	$\overline{CE}_1 = \overline{CE}_2$ = Low, I_{OUT} = -2.0mA, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}	Leakage (82S126)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 5.5V			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S129)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 5.5V			40			60	μA
		$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 0.5V			-40			-60	
I_{OS}	Short circuit (82S129)	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			105	120		105	125	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

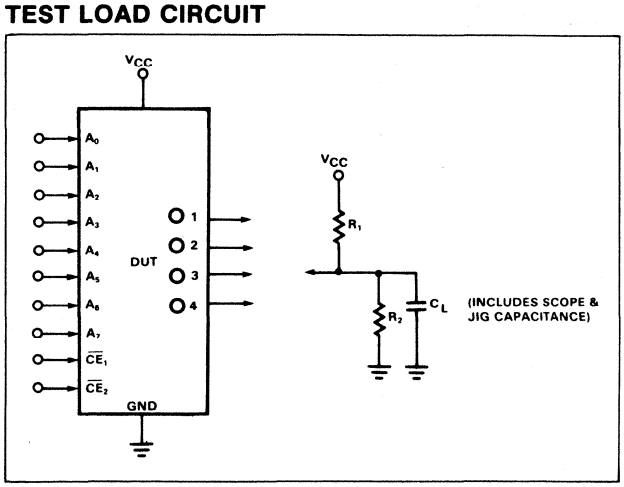
AC ELECTRICAL CHARACTERISTICS

$R_1 = 270\Omega$, $R_2 = 600\Omega$, C_L = 30pF
N82S126/129: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S126/129: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

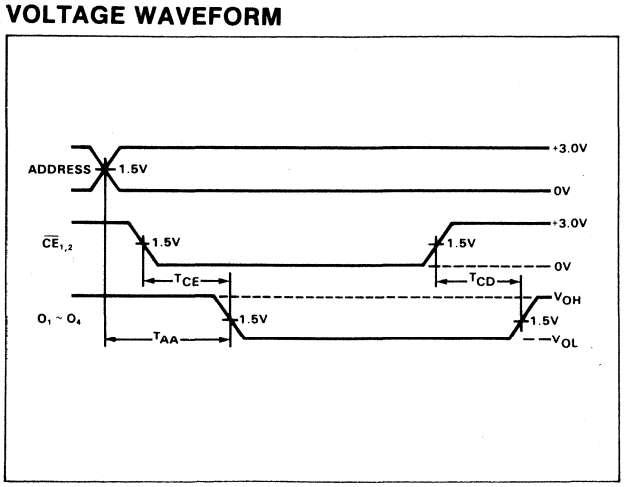
PARAMETER	TO	FROM	N82S126/129			S82S126/129			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time									ns
T_{AA}[3]	Output	Address		35	50		35	70	
T_{CE}	Output	Chip enable		15	25		15	35	
Disable time									ns
T_{CD}	Output	Chip disable		15	25		15	35	

NOTES
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.
3. Tested at an address cycle time of 1μsec.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



PROGRAMMING SYSTEM SPECIFICATIONS[4] (Testing of these limits may cause programming of device.) T_A = +25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1]	I_{CCP} = 425 ± 75mA, Transient or steady state	8.5		9.0	V
	Verify limit					V
V_{CCVH}	Upper		5.3		5.7	
V_{CCVL}	Lower		4.3		4.7	
V_S	Verify threshold[2]		1.4		1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	350		500	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0		0.8	
	Input current					µA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			-500	
V_{OPF}	Forced output voltage (program)[3]	I_{OPF} = 200 ± 20mA, Transient or steady state	16.0		18.0	V
I_{OPF}	Forced output current (program)	V_{OPF} = +17 ± 1V	180		220	mA
T_R	Output pulse rise time		10			µs
t_p	$\overline{CE}$ programming pulse width		100		125	µs
t_D	Pulse sequence delay		5			µs
T_V	$\overline{CE}$ verify pulse width		1			µs
T_{PVA}	Address program-verify cycle				1	ms
T_{PVM}	Memory program-verify time (continuous)				20	sec
F_L	Fusing attempts per link				1	cycle

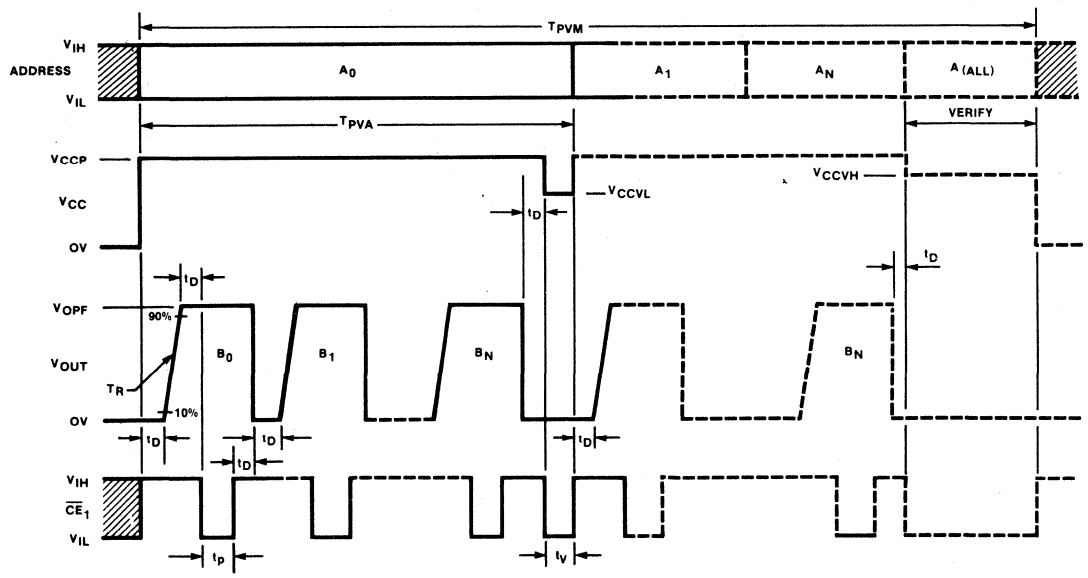
PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01µF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150mA, limit voltage spikes to a maximum slew rate of 2V/µs, and 10µs maximum recovery.
4. These are specifications which a Programming System must satisfy in order to be qualified by Signetics. They contain new limits for minimizing total device programming time, which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE}_1$ = High, $\overline{CE}_2$ = Low.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP}.
3. After t_D delay, apply V_{OPF} to the output to be programmed. Program one output at the time.
4. After t_D delay, pulse the $\overline{CE}_1$ input to logic low for a time t_p.
5. After t_D delay, remove V_{OPF} from the programmed output.
6. Repeat steps 3 through 5 to program other bits at the same address.
7. To verify programming of all bits at the same address, after t_D delay lower V_{CC} to V_{CCVL} and apply a logic low level to the $\overline{CE}_1$ input. All programmed outputs should remain in the logic high state.
8. After t_D delay, repeat steps 2 through 7 to program and verify all other address locations.
9. After t_D delay raise V_{CC} to V_{CCVH} and verify all memory locations by applying a logic low level to $\overline{CE}_1$, and cycling through all device addresses.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

10149-F

DESCRIPTION

The 10149 is field programmable, meaning that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard device is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

The 10149 is suitable for use in high performance ECL systems. The outputs are capable of driving 50Ω loads.

A chip enable input is provided for ease of memory expansion.

FEATURES

- **Address access time: 20ns max**
- **Power dissipation: 0.66mW/bit typ**
- **High impedance inputs (50kΩ pulldown)**
- **Open emitter outputs (50kΩ drive)**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 10K series**

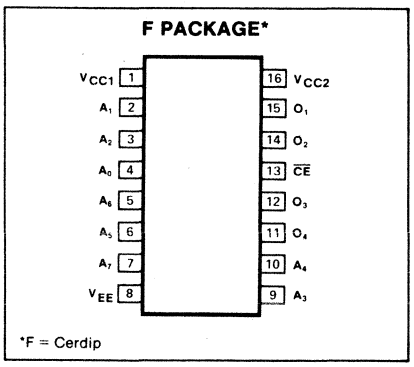
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

RECOMMENDED OPERATING RANGES

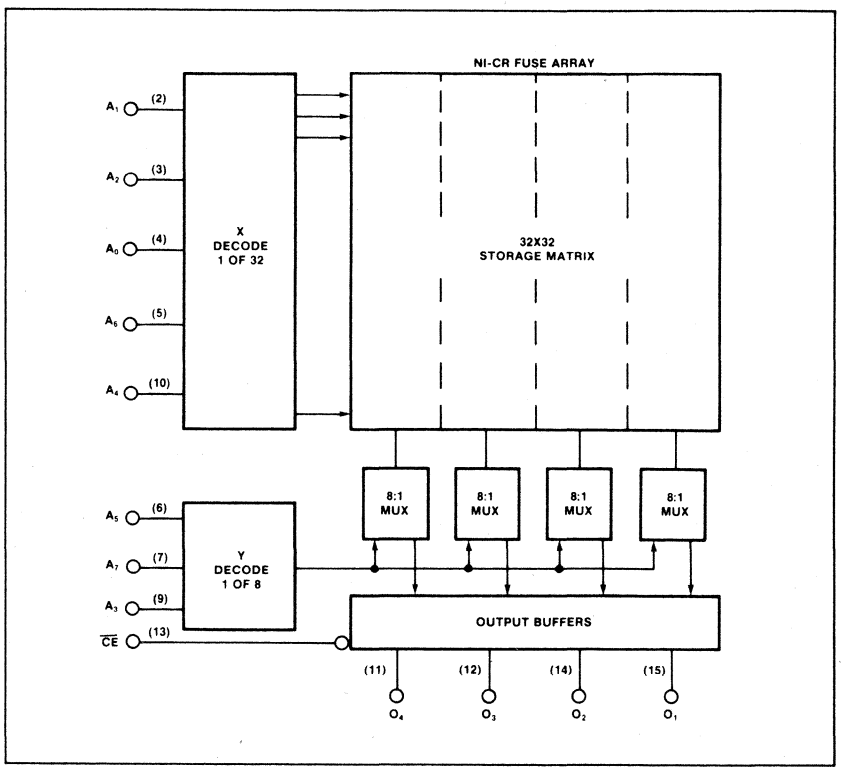
- **$V_{CC1} = V_{CC2} = GND$**
- **$V_{EE} = -5.2V \pm 5\%$**
- **$T_A = -30°C$ to $+85°C$ ambient**

PIN CONFIGURATION



*F = Cerdip

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER[1]	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	8	Vdc
V_{IN}	Input voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_O	Output source current	40	mAdc
	Temperature range		°C
T_A	Operating	-30 to +85	
T_J	Operating junction	125	
T_{STG}	Storage	-55 to +125	

10149-F

DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = 0V$, $V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2V$

PARAMETER[1]	TEST CONDITIONS	-30°C			+25°C			+85°C			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input voltage[2,3]											V
V_{IL} Low		-1.890			-1.850			-1.825			
V_{IH} High				-0.890			-0.810			-0.700	
V_{ILA} Low threshold				-1.500			-1.475			-1.440	
V_{IHA} High threshold		-1.205			-1.105			-1.035			
Output voltage											V
V_{OL} Low	V_{IH} = max	-1.89		-1.675	-1.85	-1.70	-1.65	-1.825		-1.615	
V_{OH} High	V_{IL} = min	-1.06		-0.89	-0.96	-0.89	-0.81	-0.89		-0.70	
V_{OLA} Low threshold	V_{IHA} = min, V_{ILA} = max			-1.655			-1.63			-1.595	
V_{OHA} High threshold		-1.08			-0.98			-0.91			
Input current											μA
I_{IL} Low	V_{IH} = max				0.5						
I_{IH} High	V_{IL} = min						265				
I_{EE} Supply drain current						130	150				mA

AC ELECTRICAL CHARACTERISTICS $T_A = +25°C$, $V_{EE} = -3.2V$, $V_{CC1} = V_{CC2} = 2V$, $R_L = 50\Omega$ to ground

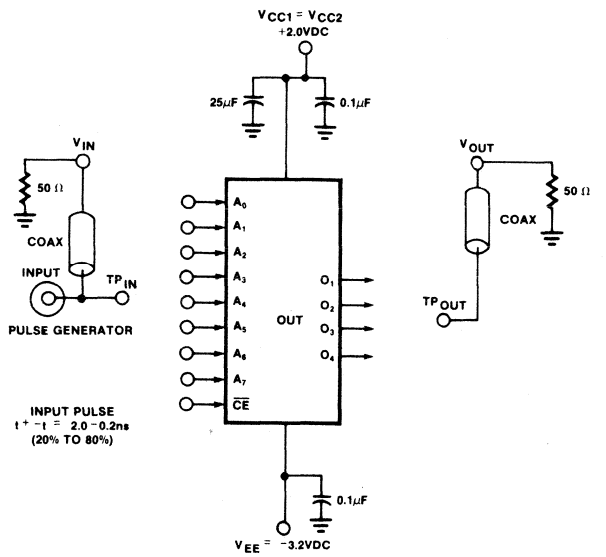
PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ	Max	
Access time						ns
T_{AA}	Output	Address		12	20	
T_{CE}	Output	Chip enable		5.5	8	
T_{CD} Disable time	Output	Chip disable		5.5	8	ns
Rise and fall time						ns
t+ Rise time (20-80%)				4.0		
t- Fall time (20-80%)				4.0		

NOTES

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Vdc ± 1%.
3. Each ECL 10K series device has been designed to meet the dc specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to -2V.

10149-F

TEST LOAD CIRCUIT



NOTES

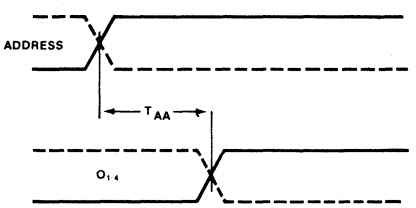
A. For ac tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.

B. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.

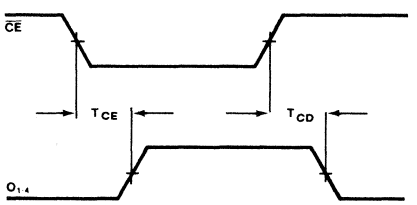
C. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A 10μF capacitor between V_{CC1} and V_{CC} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORMS

ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE PROPAGATION DELAYS



10149-F

PROGRAMMING SYSTEM SPECIFICATIONS[4] (Testing of these limits may cause programming of device.) $T_A = +25°C$.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1,3]	I_{CCP} = 150 ±25mA (Transient or steady state)	11.5		12.5	V
V_{CCVH}	Verify limit Upper	I_{CCV} = 400 ±50mA (Transient or steady state)	5.5		5.7	V
V_{CCVL}	Lower		4.7		4.9	
V_S	Verify threshold[2]			V_{CC}-1.3		V
I_{CCP}	Programming supply current	V_{CCP} = 12 ±.5V	125		175	mA
	Input voltage[5]		V_{CCV}		V_{CCV}	V
V_{IH}	High		-0.8		-0.2	
V_{IL}	Low		0		0.8	
	Input current					μA
I_{IH}	High	V_{IH} = Max.			300	
I_{IL}	Low	V_{IL} = Min.			-50	
V_{OPF}	Forced Output Voltage[3,6] (program)	I_{OPF} = 2.5±.5 mA (Transient or steady state)	6.0		6.8	V
I_{OPF}	Forced Output Current (program)	V_{OPF} = 6.4 ±.4V	2		3	mA
T_R	Output pulse rise time		0.1		1	μs
t_p	Programming pulse width		100		125	μs
t_D	Pulse sequence delay		10			μs
t_V	Verify time		1			μs
T_{PVA}	Address program-verify cycle				1	ms
T_{PVM}	Memory program-verify time (continuous)				20	sec
F_L	Fusing attempts per link				1	cycle

PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150mA, limit voltage spikes to a maximum slew rate of 2V/μs, and 10μs maximum recovery.
4. These are specifications which a Programming System must satisfy in order to be qualified by Signetics.
5. Address buffers must be referenced to the V_{CCV} supply.
6. V_{OPF} supply must be referenced to the V_{CCV} supply.

PROGRAMMING PROCEDURE

The 10149 is shipped with all bits at logical "0" (low). To write locical "1", proceed as follows:

SET-UP

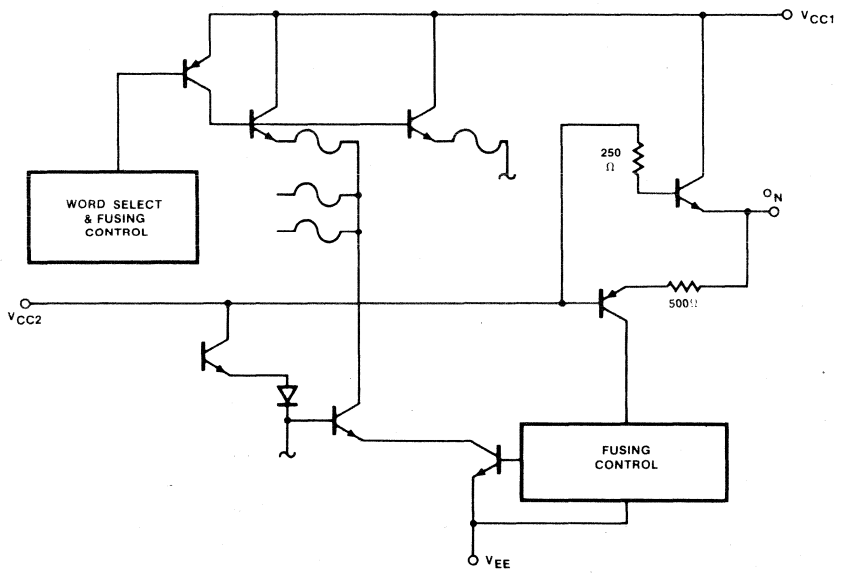
a. Set V_{EE} and $\overline{CE}$ to GND.
b. Set V_{CC1} and V_{CC2} to V_{CCVH}.
c. Terminate all device outputs with a 1.8K resistor in series with a 5.6K resistor to GND.

PROGRAM-VERIFY SEQUENCE

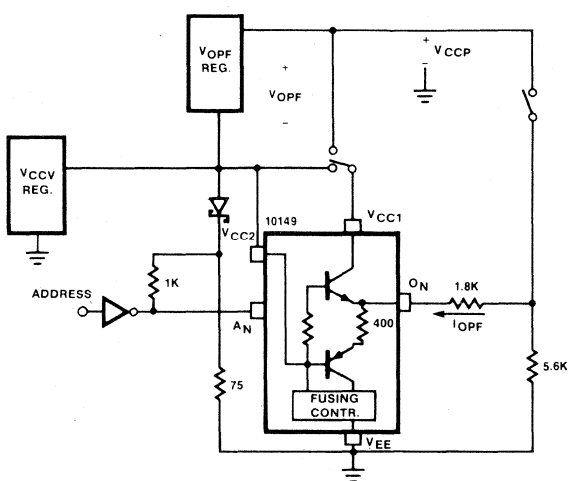
1. Select the Address to be programmed, and raise V_{CC1} to V_{CCP}.
2. After t_D delay, apply a voltage V_{OPF} to the output to be programmed via the external divider (refer to typical programming circuit). Program one output at a time.
3. After t_p delay, remove V_{OPF} from the programmed output.
4. After t_D delay, repeat steps 2 and 3 to program other bits at the same address.
5. To verify programming of all bits at the same address, after t_D delay lower V_{CC1} and V_{CC2} to V_{CCVH}. All programmed outputs should remain in the logic high state.
6. After t_D delay, repeat steps 1 through 5 to program and verify all other address locations.
7. After t_D delay lower V_{CC1} and V_{CC2} to V_{CCVL} and verify all memory locations by cycling through all device addresses.

10149-F

TYPICAL FUSING PATH

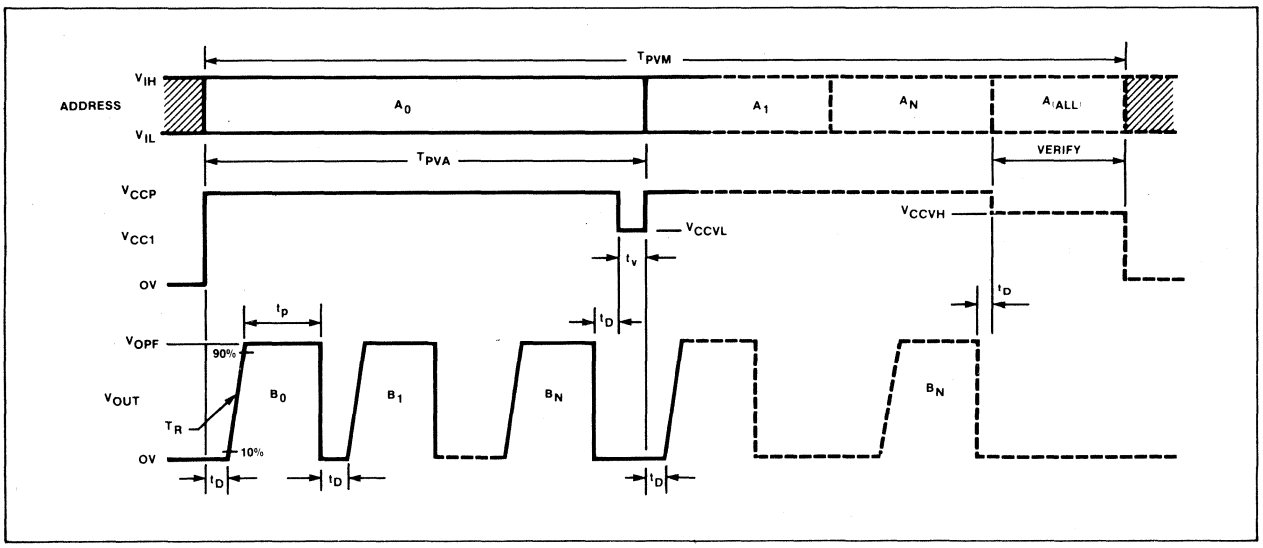


TYPICAL PROGRAMMING CIRCUIT



10149-F

PROGRAMMING SEQUENCE



DESCRIPTION

The 82S114 and 82S115 are field programmable and include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature tri-state outputs for optimization of word expansion in bused organizations. A D-type latch is used to enable the tri-state output drivers. In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe high. In this mode the bit drivers will be controlled solely by $\overline{CE}_1$ and CE_2 lines.

In the Latched Read mode, outputs are held in their previous state (high, low, or high Z) as long as Strobe is low, regardless of the state of address or chip enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the high Z state if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the high Z condition if the chip was disabled.

Both 82S114 and 82S115 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S114/115, F or N, and for the military temperature range (-55°C to +125°C) specify S82S114/115, F.

FEATURES

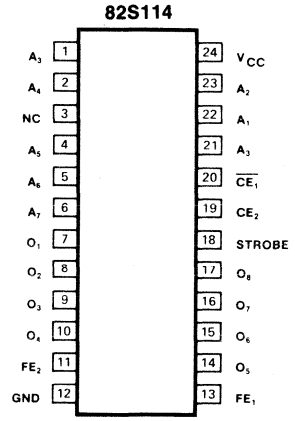
- **Address access time:**
  N82S114/115: 60ns max
  S82S114/115: 90ns max
- **Power dissipation: 165μW/bit typ**
- **Input loading:**
  N82S114/115: -100μA max
  S82S114/115: -150μA max
- **On-chip storage latches**
- **Schottky clamped**
- **Fully TTL compatible**

APPLICATIONS

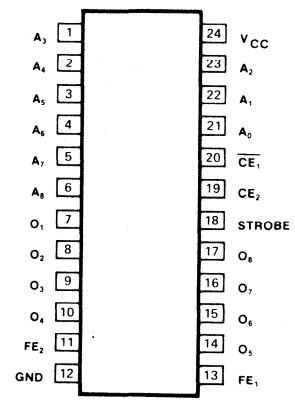
- **Microprogramming**
- **Hardwire algorithms**
- **Character generation**
- **Control store**
- **Sequential controllers**

PIN CONFIGURATIONS

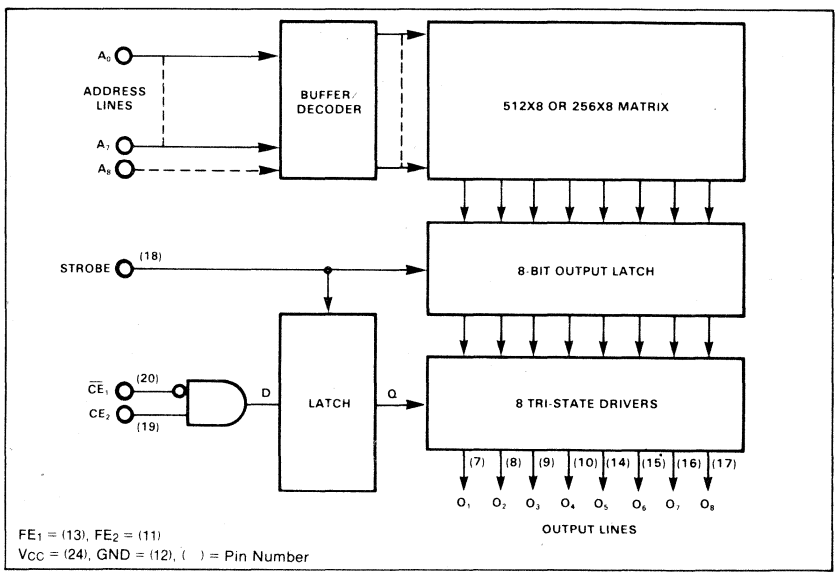
F,N PACKAGE
82S114



F,N PACKAGE
82S115



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Temperature range		°C
T_A	Operating		
	N82S114/115	0 to +75	
	S82S114/115	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S114/115: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S114/115: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[6]	N82S114/115			S82S114/115			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
	Input voltage								V
V_{IL}	Low				.85			.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 9.6mA		0.4	0.45		0.4	0.5	
V_{OH}	High	$\overline{CE_1}$ = Low, CE_2 = High, I_{OUT} = -2mA, High stored	2.7	3.3		2.4	3.3		
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			25			50	
	Output current								
$I_{O(OFF)}$	Hi-Z state	$\overline{CE_1}$ = High or CE_2 = O, V_{OUT} = 5.5V			40			100	μA
		$\overline{CE_1}$ = High or CE_2 = O, V_{OUT} = 0.5V			-40			-100	
I_{OS}	Short circuit[2]	V_{OUT} = OV	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			130	175		130	185	mA
	Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V							pF
C_{IN}	Input	V_{CC} = 5.0V, V_{OUT} = 2.0V		5			5		
C_{OUT}	Output	$\overline{CE_1}$ = High or CE_2 = 0		8			8		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, C_L = 30pF
N82S114/115: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S114/115: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

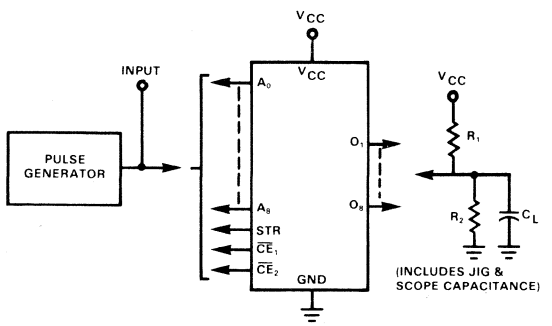
PARAMETER		TO	FROM	TEST CONDITIONS	N82S114/115			S82S114/115			UNIT
					Min	Typ[1]	Max	Min	Typ[1]	Max	
	Access time			Latched or transparent read[3,5]							ns
T_{AA}[7]		Output	Address			35	60		35	90	
T_{CE}		Output	Chip enable			20	40		20	50	
	Disable time										ns
T_{CD}		Output	Chip disable			20	40		20	55	
	Setup and hold time			Latched read only[4,5]							ns
T_{CDS}	Setup time	Output	Chip enable		40			50			
T_{CDH}	Hold time				10	0		15	0		
T_{ADH}	Hold time	Output	Address		0	-10		5	-10		
	Pulse width										ns
T_{SW}	Strobe				30	20		40	20		
	Latch time										ns
T_{SL}	Strobe				60	35		90	35		
	Delatch time										ns
T_{DL}	Strobe						30			45	

NOTES on following page.

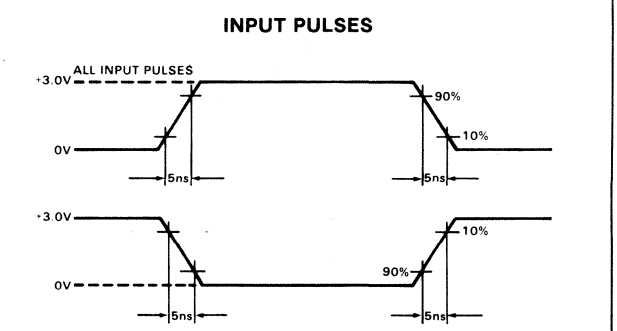
NOTES

1. Typical values are at V_{CC} = +5.0V and T_A = +25°C.
2. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in high state.
3. If the strobe is high, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_{AA} nanoseconds after the address has changed to T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an off or high impedance state after it has been enabled.
4. In latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.
5. During operation the fusing pins FE1 and FE2 may be grounded or left floating.
6. Positive current is defined as into the terminal referenced.
7. Tested at an address cycle time of 1μsec.

TEST LOAD CIRCUIT

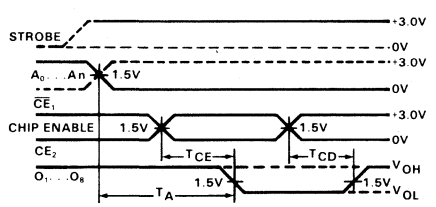


VOLTAGE WAVEFORM



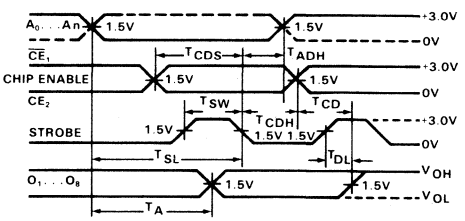
TIMING DIAGRAMS

TRANSPARENT READ[4]



Output Latches Not Used

LATCHED READ[5]



Output Latches Used

PROGRAMMING SYSTEM SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Power supply voltage					V
V_{CCP}	To program[1]	I_{CCP} = 200 ± 25mA, Transient or steady state	4.75	5.0	5.25	
	Verify limit					V
V_{CCVH}	Upper		5.3	5.5	5.7	
V_{CCVL}	Lower		4.3	4.5	4.7	
V_S	Verify threshold[2]		0.9	1.0	1.1	V
I_{CCP}	Programming supply current	V_{CCP} = +5.0 ± .25V	175	200	225	mA
	Input voltage					V
V_{IL}	Low		0	0.4	0.8	
V_{IH}	High		2.4		5.5	
	Input current (FE_1 & FE_2 only)					
I_{IL}	Low	V_{IL} = +0.45V			-100	μA
I_{IH}	High	V_{IH} = +5.5V			10	mA
	Input current (except FE_1 & FE_2)					μA
I_{IL}	Low	V_{IL} = +0.45V			-100	
I_{IH}	High	V_{IH} = +5.5V			25	
V_{OPF}	Forced output voltage (program)[3]	I_{OPF} = 200 ± 20mA, Transient or steady state	16.0	17.0	18.0	V
I_{OPF}	Forced output current (program)	V_{OPF} = +17 ± 1V	180	200	220	mA
T_R	Output pulse rise time		10		50	μs
t_P	FE_2 programming pulse width		0.3	0.4	0.5	ms
T_D	Pulse sequence delay		10			μs
T_{PR}	Programming time	$V_{CC} = V_{CCP}$			12	sec
T_{PS}	Programming pause	V_{CC} = 0V	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle[4]				50	%

PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle.
4. Continuous fusing for an unlimited time is also allowed, provided that a 60% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period (V_{CC} = 0V) of 3ms.

RECOMMENDED PROGRAMMING PROCEDURE

The 82S114/115 are shipped with all bits at logical low. To write logical high, proceed as follows:

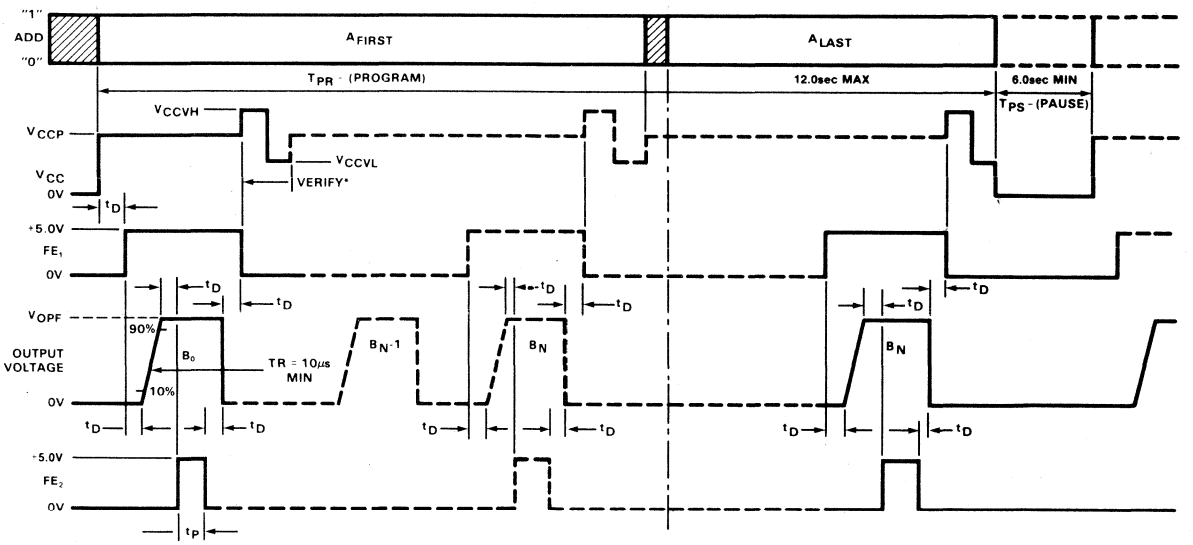
SET-UP

1. Apply GND to pin 12.
2. Terminate all device outputs with a 10kΩ resistor to V_{CC}.
3. Set $\overline{CE}_1$ to logic low, and CE_2 to logic high (TTL levels).
4. Set Strobe to logic high level.

Program-Verify Sequence

1. Raise V_{CC} to V_{CCP}, and address the word to be programmed by applying TTL high and low logic levels to the device address inputs.
2. After 10μs delay, apply to FE_1 (pin 13) a voltage source of +5.0 ± 0.5V, with 10mA sourcing current capability.
3. After 10μs delay, apply a voltage source of +17.0 ± 1.0V to the output to be programmed. The source must have a current limit 200mA. Program on output at the time.
4. After 10μs delay, raise FE_2 (pin 11) from 0V to +5.0 ± 0.5V for a period of 1ms, and then return to 0V. Pulse source must have a 10mA sourcing current capability.
5. After 10μs delay, remove +17.0V supply from programmed output.
6. To verify programming, after 10μs delay, return FE_1 to 0V. Raise V_{CC} to V_{CCH} = +5.5 ± .2V. The programmed output should remain in the high state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the high state.
7. Raise V_{CC} to V_{CCP} and repeat steps 2 through 6 to program other bits at the same address.
8. Repeat steps 1 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

82S130-F,N • 82S131-F,N

DESCRIPTION

The 82S130 and 82S131 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S130 and 82S131 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S130 and 82S131 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0° to +75°C) specify N82S130/131, F or N, and for the military temperature range (-55°C to +125°C) specify S82S130/131, F.

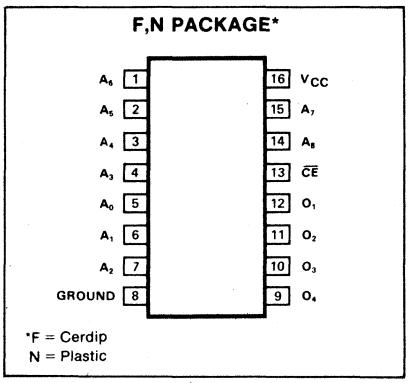
FEATURES

- **Address access time:**
  N82S130/131: 50ns max
  S82S130/131: 70ns max
- **Power dissipation: 0.3mW/bit typ**
- **Input loading:**
  N82S130/131: -100μA max
  S82S130/131: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S130: Open collector
  82S131: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

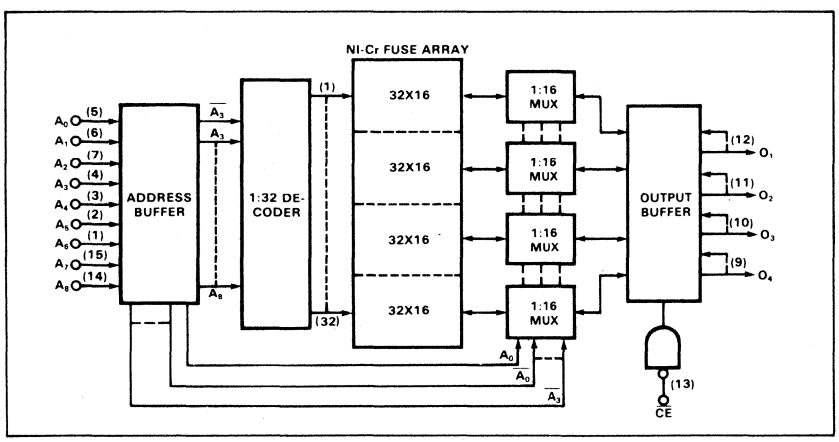
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S130)	+5.5	
V_O	Off-state (82S131)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S130/131	0 to +75	
	S82S130/131	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S130/131: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

S82S130/131: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[2]	N82S130/131			S82S130/131			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High (82S131)	$\overline{CE}$ = low, I_{OUT} = -2mA high stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}	Leakage (82S130)	$\overline{CE}$ = high, V_{OUT} = 5.5V			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S131)	$\overline{CE}$ = high, V_{OUT} = 5.5V			40			60	μA
		$\overline{CE}$ = high, V_{OUT} = 0.5V			-40			-60	
I_{OS}	Short circuit (82S131)	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			120	140		120	140	mA
	Capacitance	V_{IN} = 2.0V, V_{CC} = 5.0V							pF
C_{IN}	Input			5			5		
C_{OUT}	Output			8			8		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$[2]

N82S130/131: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

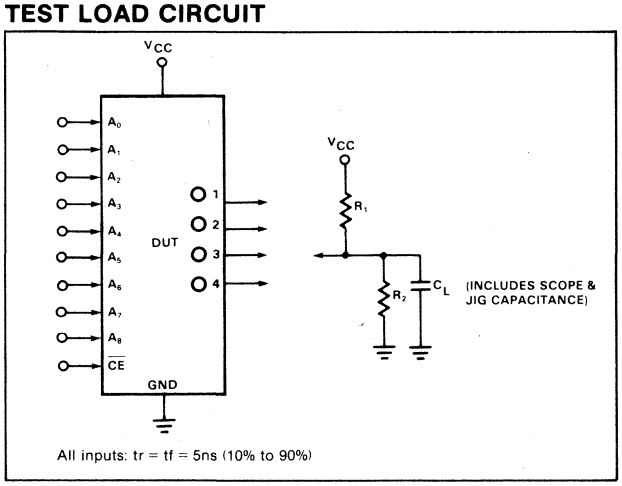
S82S130/131: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S130/131			S82S130/131			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
Access time									ns
T_{AA}[3]	Output	Address		40	50		40	70	
T_{CE}	Output	Chip enable		20	30		20	40	
Disable time									ns
T_{CD}	Output	Chip disable		20	30		20	40	

NOTES

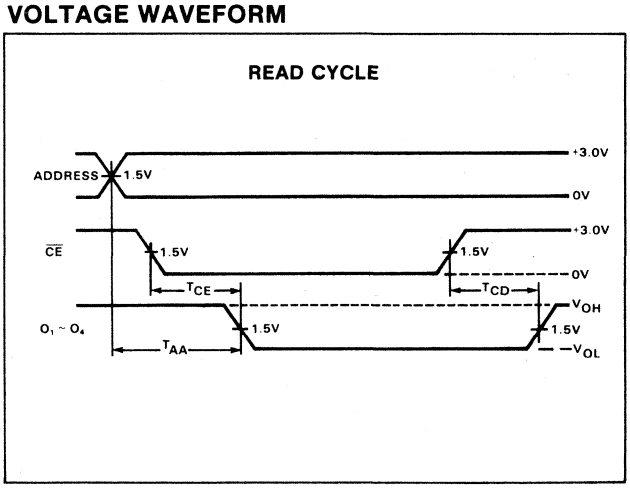
1. Typical values are at V_{CC} = 5.0V, T_A = +25°C.
2. Positive current is defined as into the terminal referenced.
3. Tested at an address cycle time of 1μsec.

TEST LOAD CIRCUIT



All inputs: tr = tf = 5ns (10% to 90%)

VOLTAGE WAVEFORM



PROGRAMMING SYSTEM SPECIFICATIONS[4] (Testing of these limits may cause programming of device.) $T_A = +25°C$

	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1]	I_{CCP} = 425 ± 75mA, Transient or steady state	8.5		9.0	V
	Verify limit					V
V_{CCVH}	Upper		5.3		5.7	
V_{CCVL}	Lower		4.3		4.7	
V_S	Verify threshold[2]		1.4		1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	350		500	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0		0.8	
	Input current					µA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			-500	
V_{OPF}	Forced Output Voltage[3] (program)	I_{OPF} = 200 ± 20mA, Transient or steady state	16.0		18.0	V
I_{OPF}	Forced Output Current (program)	V_{OPF} = +17 ± 1V	180		220	mA
T_R	Output pulse rise time		10			µs
t_P	$\overline{CE}$ programming pulse width		100		125	µs
t_D	Pulse sequence delay		5			µs
t_V	$\overline{CE}$ verify pulse width		1			µs
T_{PVA}	Address program-verify cycle				1	ms
T_{PVM}	Memory program-verify time (continuous)				20	sec
F_L	Fusing attempts per link				1	cycle

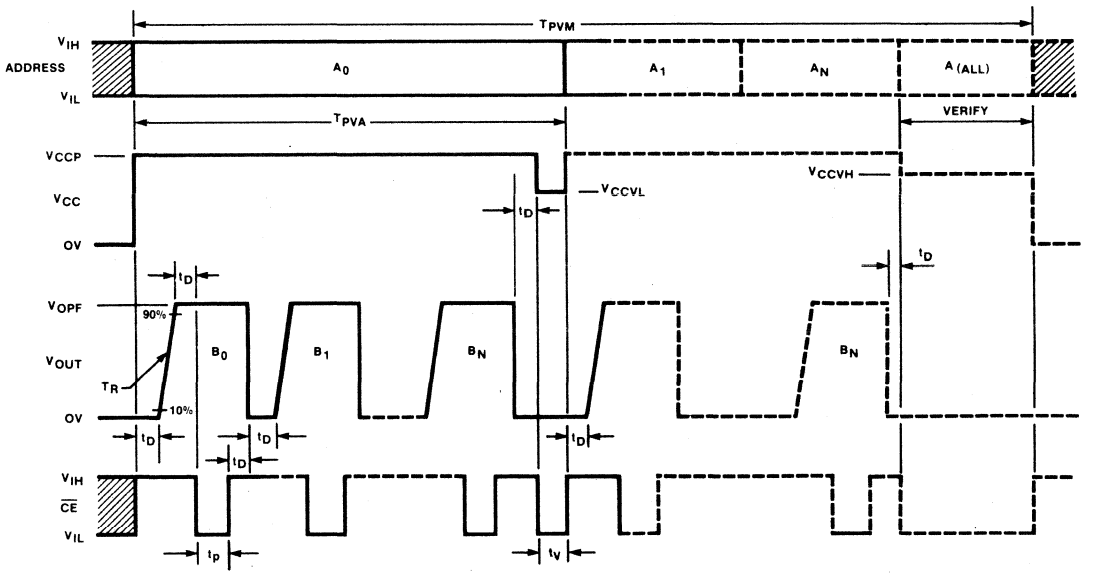
PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01µF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150mA, limit voltage spikes to a maximum slew rate of 2V/µs, and 10µs maximum recovery.
4. These are specifications which a Programming System must satisfy in order to be qualified by Signetics. They contain new limits for minimizing total device programming time, which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE}$ = High.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP}.
3. After t_D delay, apply V_{OPF} to the output to be programmed. Program one output at the time.
4. After t_D delay, pulse the $\overline{CE}$ input to logic low for a time t_P.
5. After t_D delay, remove V_{OPF} from the programmed output.
6. Repeat steps 3 through 5 to program other bits at the same address.
7. To verify programming of all bits at the same address, after t_D delay lower V_{CC} to V_{CCVL} and apply a logic low level to the $\overline{CE}$ input. All programmed outputs should remain in the logic high state.
8. After t_D delay, repeat steps 2 through 7 to program, and verify all other address locations.
9. After t_D delay raise V_{CC} to V_{CCVH} and verfiy all memory locations by applying a logic low level to $\overline{CE}$, and cycling through all device addresses.

TYPICAL PROGRAMMING SEQUENCE



* Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

82S140-F,N • 82S141-F,N

DESCRIPTION

The 82S140 and 82S141 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S140 and 82S141 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 4 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S140 and 82S141 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S140/141, F or N, and for the military temperature range (-55°C to +125°C) specify S82S140/141,F.

FEATURES

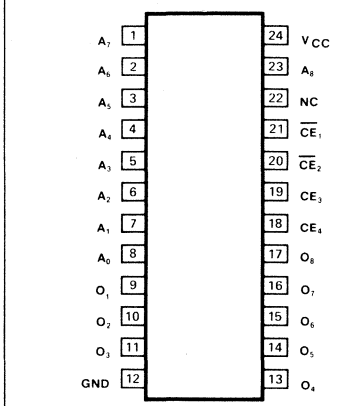
- **Address access time:**
  N82S140/141: 60ns max
  S82S140/141: 90ns max
- **Power dissipation: .17mW/bit typ**
- **Input loading:**
  N82S140/141: -100μA max
  S82S140/141: -150μA max
- **On-chip address decoding**
- **Output options:**
  S82S140: Open collector
  S82S141: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

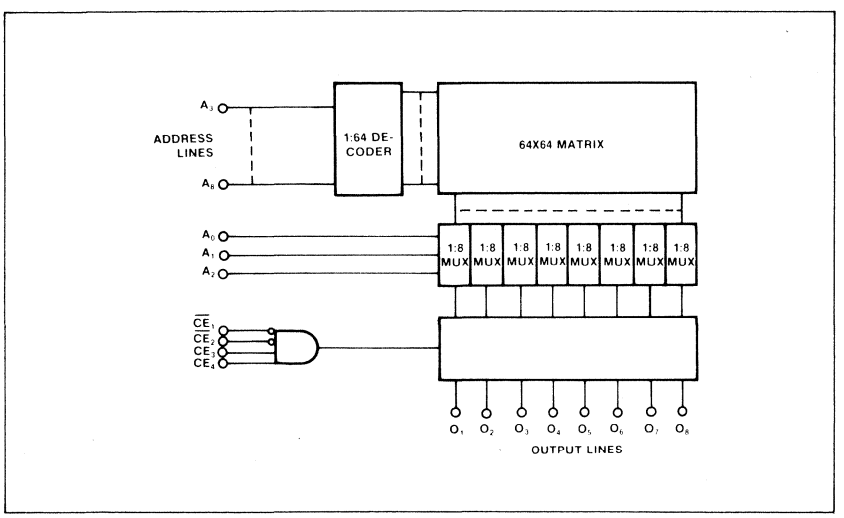
PIN CONFIGURATION

F,N PACKAGE *



*F = Cerdip
N = Plastic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S140)	+5.5	
V_O	Off-state (82S141)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S140/141	0 to +75	
	S82S140/141	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S140/141: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S140/141: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS[1]	N82S140/141			S82S140/141			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 9.6mA			0.45			0.5	
V_{OH}	High (82S141)	$\overline{CE_1}$ = Low, I_{OUT} = -2mA, $\overline{CE_2}$ = Low, CE_3 = High, CE_4 = High, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} =0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}	Leakage (82S140)	$\overline{CE_1}$ = High, V_{OUT} = 5.5V, $\overline{CE_2}$ = High, CE_3 = Low, CE_4 = Low			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S141)	$\overline{CE_1}$ = High, V_{OUT} = 0.5V, $\overline{CE_2}$ = High, CE_3 = Low, CE_4 = Low			-40			-60	μA
		$\overline{CE_1}$ = High, V_{OUT} = 5.5V, $\overline{CE_2}$ = High, CE_3 = Low, CE_4 = Low			40			60	
I_{OS}	Short circuit (82S141)	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			140	175		140	185	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

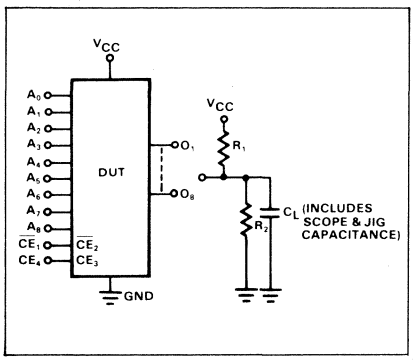
R_1 = 470Ω, R_2 = 1kΩ, C_L = 30pF
N82S140/141: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S140/141: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82S140/141			S82S140/141			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time									ns
T_{AA}[3]	Output	Address		40	60		40	90	
T_{CE}	Output	Chip enable		20	40		20	50	
Disable time									ns
T_{CD}	Output	Chip disable		20	40		20	50	

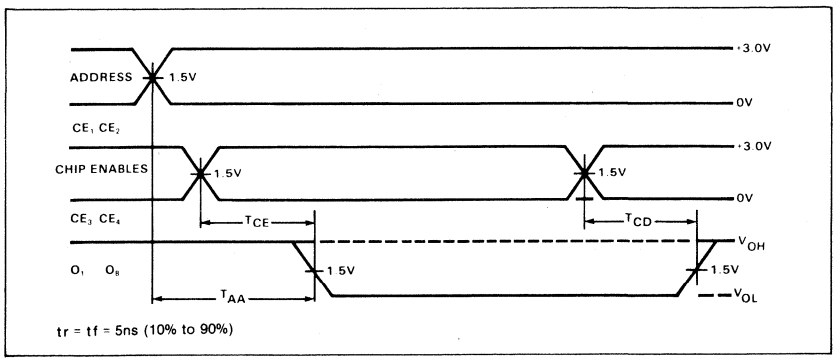
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.
3. Tested at an address cycle time of 1μsec.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



PROGRAMMING SYSTEM SPECIFICATIONS[4] (Testing of these limits may cause programming of device.) T_A = +25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1]	I_{CCP} = 425 ± 75mA, Transient or steady state	8.5		9.0	V
	Verify limit					V
V_{CCVH}	Upper		5.3		5.7	
V_{CCVL}	Lower		4.3		4.7	
V_S	Verify threshold[2]		1.4		1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	350		500	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0		0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			-500	
V_{OPF}	Forced output voltage (program)[3]	I_{OPF} = 200 ± 20mA, Transient or steady state	16.0		18.0	V
I_{OPF}	Forced output current (program)	V_{OPF} = +17 ± 1V	180		220	mA
T_R	Output pulse rise time		10			μs
t_p	$\overline{CE}$ programming pulse width		100		125	μs
t_D	Pulse sequence delay		5			μs
T_V	$\overline{CE}$ verify pulse width		1			μs
T_{PVA}	Address program-verify cycle				1	ms
T_{PVM}	Memory program-verify time (continuous)				20	sec
F_L	Fusing attempts per link				1	cycle

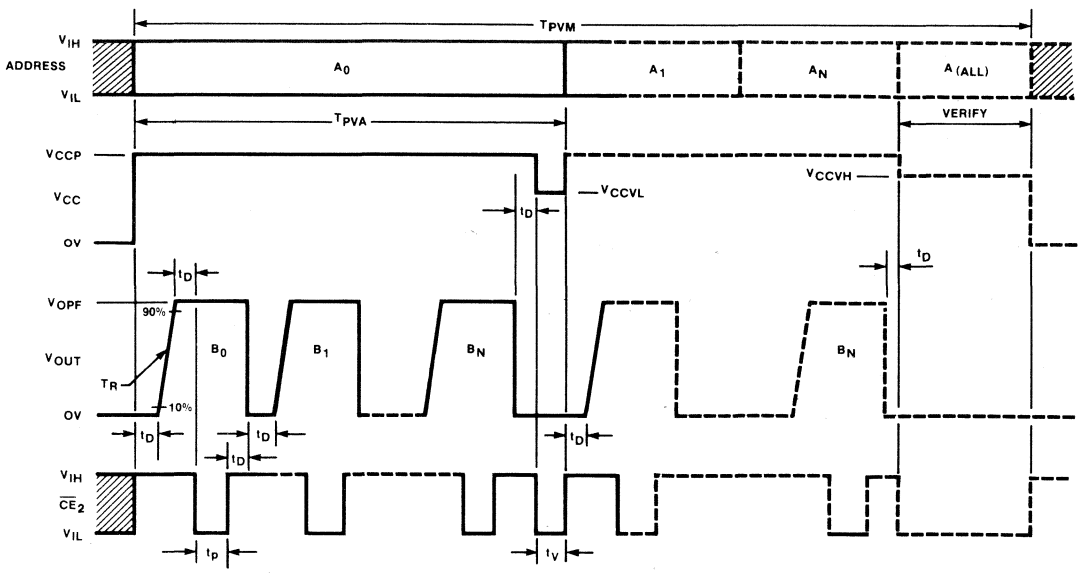
PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150mA, limit voltage spikes to a maximum slew rate of 2V/μs, and 10μs maximum recovery.
4. These are specifications which a Programming System must satisfy in order to be qualified by Signetics. They contain new limits for minimizing total device programming time, which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE_1}$ = Low. $\overline{CE_2}$ = High, CE_3 = High, CE_4 = High.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP}.
3. After t_D delay, apply V_{OPF} to the output to be programmed. Program one output at the time.
4. After t_D delay, pulse the $\overline{CE_2}$ input to logic low for a time t_P.
5. After t_D delay, remove V_{OPF} from the programmed output.
6. Repeat steps 3 through 5 to program other bits at the same address.
7. To verify programming of all bits at the same address, after t_D delay lower V_{CC} to V_{CCVL} and apply a logic low level to the $\overline{CE_2}$ input. All programmed outputs should remain in the logic high state.
8. After t_D delay, repeat steps 2 through 7 to program, and verify all other address locations.
9. After t_D delay raise V_{CC} to V_{CCVH} and verify all memory locations by applying a logic low level to $\overline{CE_2}$, and cycling through all device addresses.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

OBJECTIVE SPECIFICATION 82S146-F • 82S147-F

DESCRIPTION

The 82S146 and 82S147 are field-programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

The 82S146 and 82S147 include on-chip decoding and one chip enable input for ease of memory expansion, and feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S146 and 82S147 devices are available in the commercial temperature range (0°C to +75°C), and are specified as N82S146/147, F.

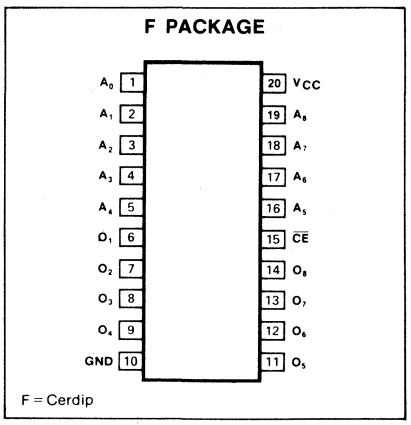
FEATURES

- **Address access time: 45ns max**
- **Power dissipation: 155mA max**
- **Input loading: -100μA max**
- **One chip enable input**
- **On chip address decoding**
- **Output options:**
  - **82S146: Open collector**
  - **82S147: Tri-state**
- **No separate fusing pins**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION

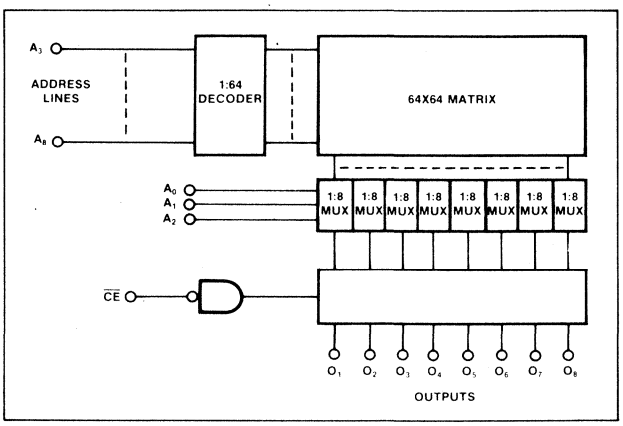


F = Cerdip

PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	A_0	Address
2	A_1	Address
3	A_2	Address
4	A_3	Address
5	A_4	Address
6	O_1	Output
7	O_2	Output
8	O_3	Output
9	O_4	Output
10	GND	Ground
11	O_5	Output
12	O_6	Output
13	O_7	Output
14	O_8	Output
15	$\overline{CE}$	Chip enable bar
16	A_5	Address
17	A_6	Address
18	A_7	Address
19	A_8	Address
20	V_{CC}	Power supply voltage

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S146)	+5.5	
V_O	Off-state (82S147)	+5.5	
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$.

PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low				.85	
V_{IH}	High		2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2	
	Output voltage					V
V_{OL}	Low	I_{OUT} = 9.6mA			0.45	
V_{OH}	High (82S147)	$\overline{CE}$ = Low, I_{OUT} = -2mA, High stored	2.4			
	Input current					μA
I_{IL}	Low	V_{IN} = 0.45V			-100	
I_{IH}	High	V_{IN} = 5.5V			40	
	Output current					
I_{OLK}	Leakage (82S147)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40	μA
$I_{O(OFF)}$	Hi-Z state (82S147)	$\overline{CE}$ = High, V_{OUT} = 0.5V			-40	μA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			40	
I_{OS}	Short circuit (82S147)	V_{OUT} = 0V	-20		-70	mA
I_{CC}	V_{CC} supply current			115	155	mA
	Capacitance	V_{CC} = 5.0V				pF
C_{IN}	Input	V_{IN} = 2.0V		5		
C_{OUT}	Output	V_{OUT} = 2.0V		8		

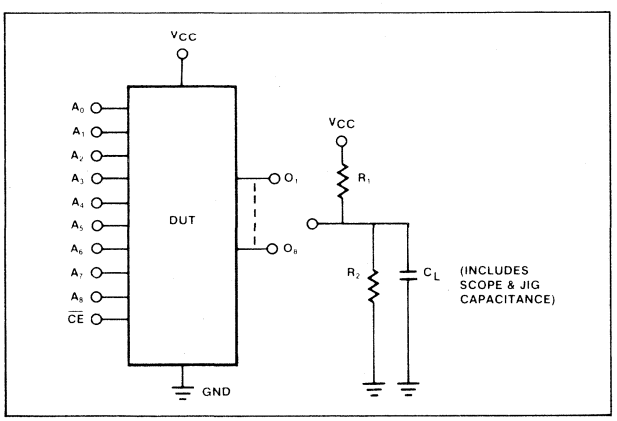
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, C_L = 30pF, $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ[2]	Max	
	Access time						ns
T_{AA}		Output	Address		30	45	
T_{CE}		Output	Chip enable		20	30	
T_{CD}	Disable time	Output	Chip disable		20	30	ns

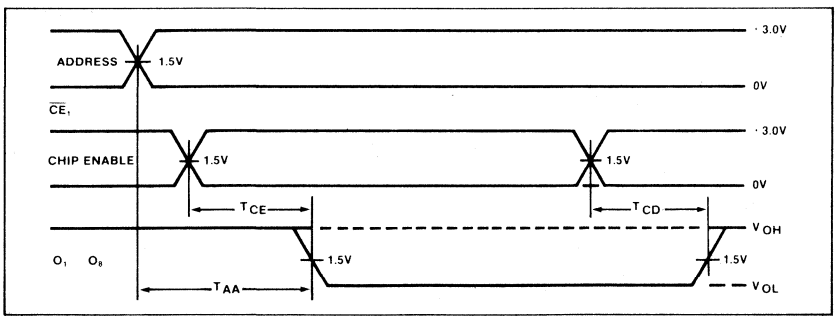
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



PROGRAMMING SYSTEM SPECIFICATIONS[4] T_A = +25° C. (Testing of these limits may cause programming of device.)

PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
	Power supply voltage					V
V_{CCP}	To program[1]	I_{CCP} = 425 ± 75mA, Transient or steady state	8.5		9.0	
	Verify limit					V
V_{CCVH}	Upper		5.3		5.7	
V_{CCVL}	Lower		4.3		4.7	
V_S	Verify threshold[2]		1.4		1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	350		500	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0		0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			-500	
V_{OPF}	Forced output voltage (program)[3]	I_{OPF} = 200 ± 20mA, Transient or steady state	16.0		18.0	V
I_{OPF}	Forced output current (program)	V_{OPF} = +17 ± 1V	180		220	mA
T_R	Output pulse rise time		10			μs
t_P	$\overline{CE}$ programming pulse width		100		125	μs
t_D	Pulse sequence delay		5			μs
t_V	$\overline{CE}$ verify pulse width		1			μs
T_{PVA}	Address program-verify cycle				1	ms
T_{PVM}	Memory program-verify time (continuous)				20	sec
F_L	Fusing attempts per link				1	cycle

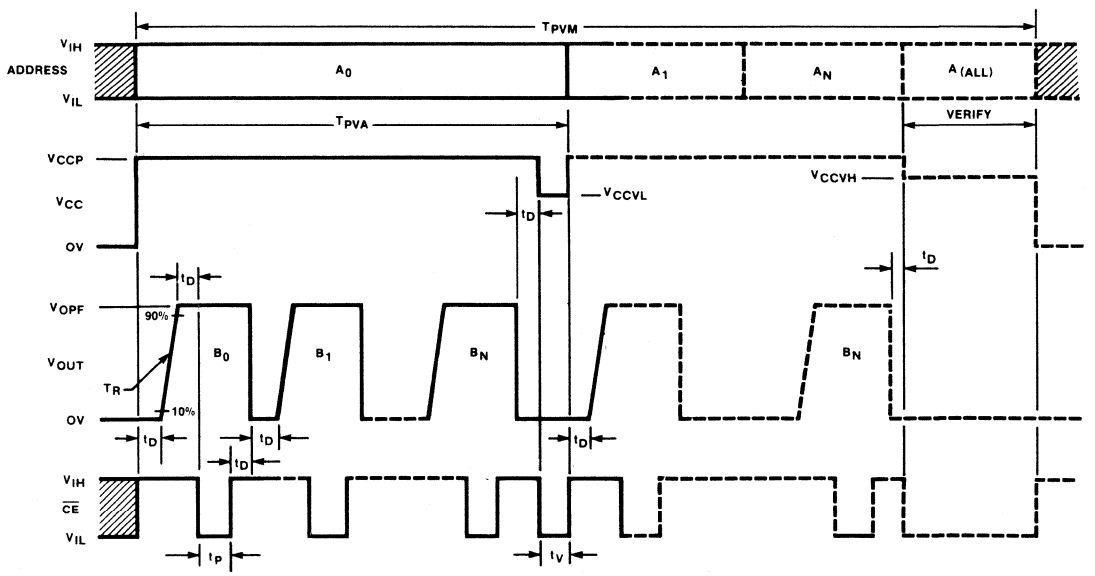
PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150mA, limit voltage spikes to a maximum slew rate of 2V/μs, and 10μs maximum recovery.
4. These are specifications which a Programming System must satisfy in order to be qualified by Signetics. They contain new limits for minimizing total device programming time, which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE}$ = High.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP}.
3. After t_D delay, apply V_{OPF} to the output to be programmed. Program one output at the time.
4. After t_D delay, pulse the $\overline{CE}$ input to logic low for a time t_P.
5. After t_D delay, remove V_{OPF} from the programmed output.
6. Repeat steps 3 through 5 to program other bits at the same address.
7. To verify programming of all bits at the same address after t_D delay lower V_{CC} to V_{CCVL} and apply a logic low level to the $\overline{CE}$ input. All programmed outputs should remain in the logic high state.
8. After t_D delay, repeat steps 2 through 7 to program, and verify all other address locations.
9. After t_D delay raise V_{CC} to V_{CCVH} and verify all memory locations by applying a logic low level to $\overline{CE}$, and cycling through all device addresses.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

82S136/82S136A-F,N • 82S137/82S137A-F,N

DESCRIPTION

The 82S136 and 82S137 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S136 and 82S137 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

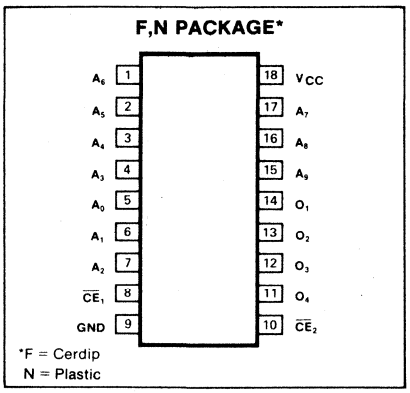
These devices include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S136 and 82S137 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S136/137, F or N, and for the military temperature range (-55°C to +125°C) specify S82S136/137, F.

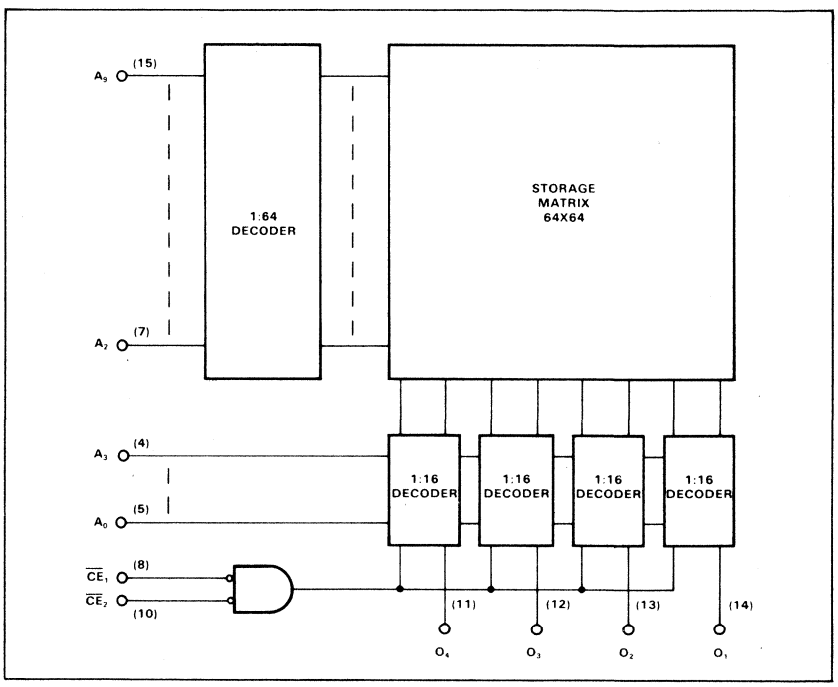
FEATURES

- **Address access time:**
  - **N82S136A/137A: 45ns max**
  - **N82S136/137: 60ns max**
  - **S82S136/137: 80ns max**
- **Power dissipation: .13mW/bit typ**
- **Input loading:**
  - **N82S136/137: -100μA max**
  - **S82S136/137: -150μA max**
- **On-chip address decoding**
- **Output options:**
  - **82S136: Open collector**
  - **82S137: Tri-state**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S136)	+5.5	
V_O	Off-state (82S137)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S136/137	0 to +75	
	S82S136/137	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S136/137; N82S136A/137A: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S136/137; S82S136A/137A: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	N82S136/137 N82S136A/137A			S82S136/137 S82S136A/137A			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High (82S137)	$\overline{CE}$ = Low, I_{OUT} = -2mA, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}	Leakage (82S136)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40			60	μA
$I_{O(OFF)}$	Off-state (82S137)	$\overline{CE}$ = High, V_{OUT} = 0.5V			-40			-60	μA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			40			60	
I_{OS}	Short circuit (82S137)	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			105	140		105	140	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

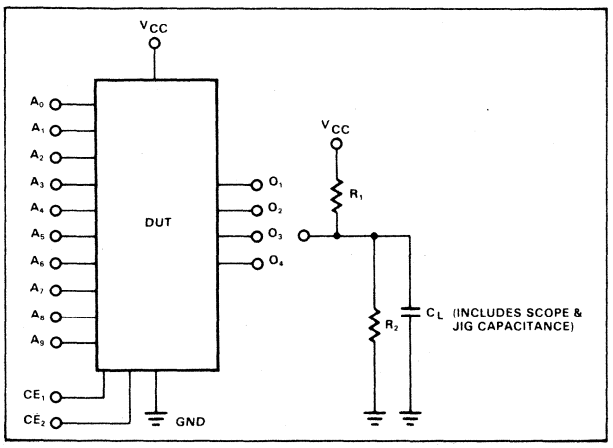
$R_1 = 270\Omega$, $R_2 = 600\Omega$, C_L = 30pF[1]
N82S136/137; N82S136A/137A: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S136/137; S82S136A/137A: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S136/137			S82S136/137			N82S136A/137A			S82S136A/137A			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time															ns
T_{AA}	Output	Address		40	60		40	80		30	45		30	70	
T_{CE}	Output	Chip enable		20	30		20	40		20	30		20	40	
Disable time															ns
T_{CD}	Output	Chip disable		20	30		20	40		20	30		20	40	

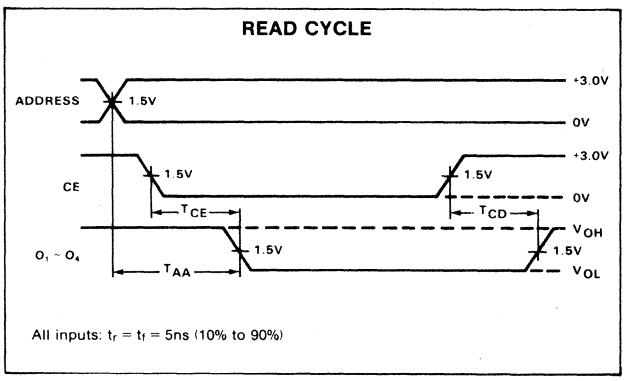
NOTES

1. Positive current is defined as into the terminal referenced.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



PROGRAMMING SYSTEM SPECIFICATIONS[4] (Testing of these limits may cause programming of device.) T_A = +25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1]	I_{CCP} = 425 ± 75mA, Transient or steady state	8.5		9.0	V
	Verify limit					V
V_{CCVH}	Upper		5.3		5.7	
V_{CCVL}	Lower		4.3		4.7	
V_S	Verify threshold[2]		1.4		1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	350		500	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0		0.8	
	Input current					µA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			-500	
V_{OPF}	Forced Output Voltage[3] (program)	I_{OPF} = 200 ± 20mA, Transient or steady state	16.0		18.0	V
I_{OPF}	Forced Output Current (program)	V_{OPF} = +17 ± 1V	180		220	mA
T_R	Output pulse rise time		10			µs
t_P	$\overline{CE}$ programming pulse width		100		125	µs
t_D	Pulse sequence delay		5			µs
t_V	$\overline{CE}$ verify pulse width		1			µs
T_{PVA}	Address program-verify cycle				1	ms
T_{PVM}	Memory program-verify time (continuous)				20	sec
F_L	Fusing attempts per link				1	cycle

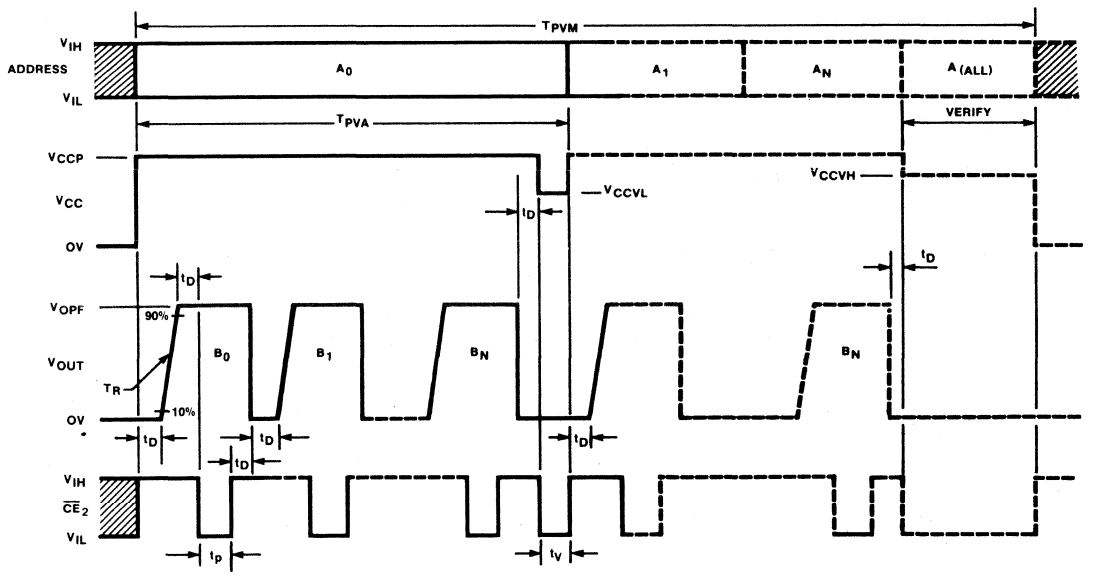
PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01µF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150mA, limit voltage spikes to a maximum slew rate of 2V/µs, and 10µs maximum recovery.
4. These are specifications which a Programming System must satisfy in order to be qualified by Signetics. They contain new limits for minimizing total device programming time, which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE}_1$ = Low, $\overline{CE}_2$ = High.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP}.
3. After t_D delay, apply V_{OPF} to the output to be programmed. Program one output at the time.
4. After t_D delay, pulse the $\overline{CE}_2$ input to logic low for a time t_P.
5. After t_D delay, remove V_{OPF} from the programmed output.
6. Repeat steps 3 through 5 to program other bits at the same address.
7. To verify programming of all bits at the same address after t_D delay lower V_{CC} to V_{CCVL} and apply a logic low level to the $\overline{CE}_2$ input. All programmed outputs should remain in the logic high state.
8. After t_D delay, repeat steps 2 through 7 to program, and verify all other address locations.
9. After t_D delay raise V_{CC} to V_{CCVH} and verify all memory locations by applying a logic low level to $\overline{CE}_2$, and cycling through all device addresses.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

82S180-F,N • 82S181-F,N

DESCRIPTION

The 82S180 and 82S181 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S180 and 82S181 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 4 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

The 82S180 and 82S181 are available in both the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S180/181, F or N, and for the military temperature range (-55°C to +125°C) specify S82S180/181, F.

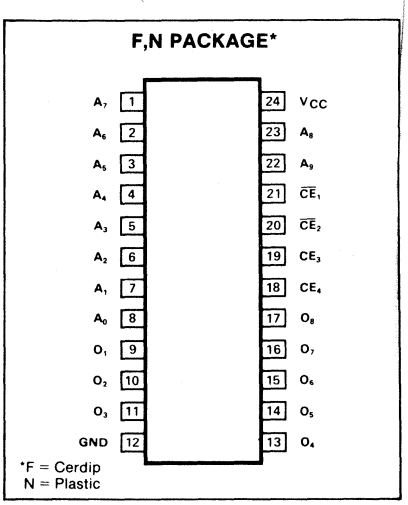
FEATURES

- **Address access time:**
  N82S180/181: 70ns max
  S82S180/181: 90ns max
- **Power dissipation: 85μW/bit typ**
- **Input loading:**
  N82S180/181: -100μA max
  S82S180/181: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S180: Open collector
  82S181: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

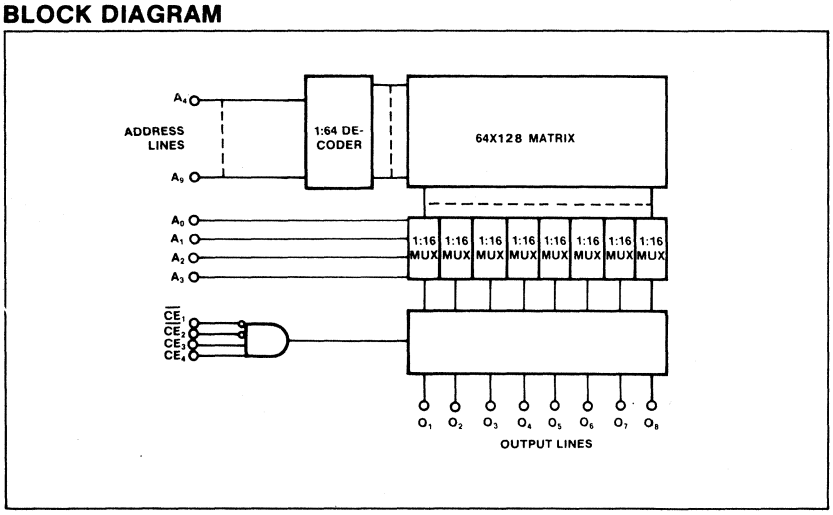
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S180)	+5.5	
V_O	Off-state (82S181)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S180/181	0 to +75	
	S82S180/181	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S180/181: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S180/181: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	N82S180/181			S82S180/181			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.45			0.5	
V_{OH}	High (82S181)	$\overline{CE_1}$ = low, $I_{OUT} = -2mA$, $\overline{CE_2}$ = low, CE_2 = high, CE_4 = high, high stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	$V_{IN} = 0.45V$			-100			-150	
I_{IH}	High	$V_{IN} = 5.5V$			40			50	
	Output current								
I_{OLK}	Leakage (82S180)	$\overline{CE_1}$ = high, $V_{OUT} = 5.5V$, $\overline{CE_2}$ = high, CE_3 = low, CE_4 = low			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S181)	$\overline{CE_1}$ = high, $V_{OUT} = 0.5V$, $\overline{CE_2}$ = high, CE_3 = low, CE_4 = low			-40			-60	μA
		$\overline{CE_1}$ = high, $V_{OUT} = 5.5V$, $\overline{CE_2}$ = high, CE_3 = low, CE_4 = low			40			60	μA
I_{OS}	Short circuit (82S181)	$V_{OUT} = 0V$	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			140	175		140	185	mA
	Capacitance	$V_{CC} = 5.0V$							pF
C_{IN}	Input	$V_{IN} = 2.0V$		5			5		
C_{OUT}	Output	$V_{OUT} = 2.0V$		8			8		

AC ELECTRICAL CHARACTERISTICS

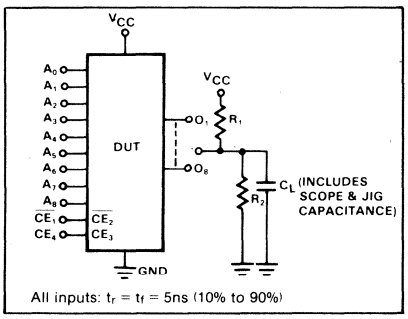
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S180/181: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S180/181: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC}$ 5.5V

PARAMETER	TO	FROM	N82S180/181			S82S180/181			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time									ns
T_{AA}[3]	Output	Address		50	70		50	90	
T_{CE}	Output	Chip enable		20	40		20	50	
Disable time									ns
T_{CD}	Output	Chip disable		20	40		20	50	

NOTES

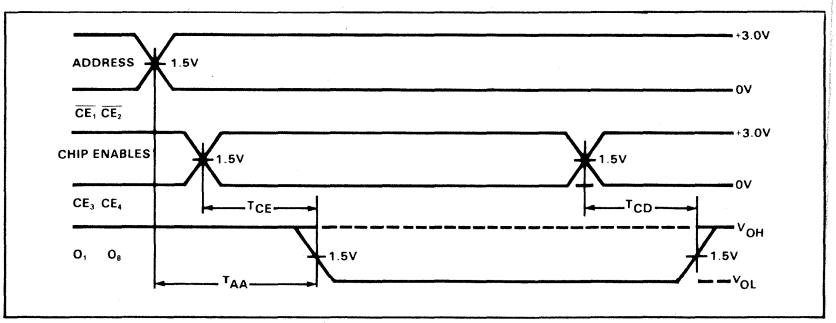
1. Positive current is defined as into the terminal referenced.
2. Typical values are at $V_{CC} = 5.0V$, $T_A = +25°C$.
3. Tested at an address cycle time of 1μsec.

TEST LOAD CIRCUIT



All inputs: $t_r = t_f = 5ns$ (10% to 90%)

VOLTAGE WAVEFORM



PROGRAMMING SYSTEM SPECIFICATIONS[4]

(Testing of these limits may cause programming of device.) $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Power supply voltage					V
V_{CCP}	To program[1]	I_{CCP} = 425 ± 75 mA, Transient or steady state	8.5		9.0	
	Verify limit					V
V_{CCVH}	Upper		5.3		5.7	
V_{CCVL}	Lower		4.3		4.7	
V_S	Verify threshold[2]		1.4		1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	350		500	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0		0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			-500	
V_{OPF}	Forced Output Voltage[3] (program)	I_{OPF} = 200 ± 20mA, Transient or steady state	16.0		18.0	V
I_{OPF}	Forced Output Current (program)	V_{OFP} = + 17 ± 1V	180		220	mA
T_R	Output pulse rise time		10			μs
t_p	$\overline{CE}$ programming pulse width		100		125	μs
t_D	Pulse sequence delay		5			μs
t_V	$\overline{CE}$ verify pulse width		1			μs
T_{PVA}	Address program-verify cycle				1	ms
T_{PVM}	Memory program-verify time (continuous)				20	sec
F_L	Fusing attempts per link				1	cycle

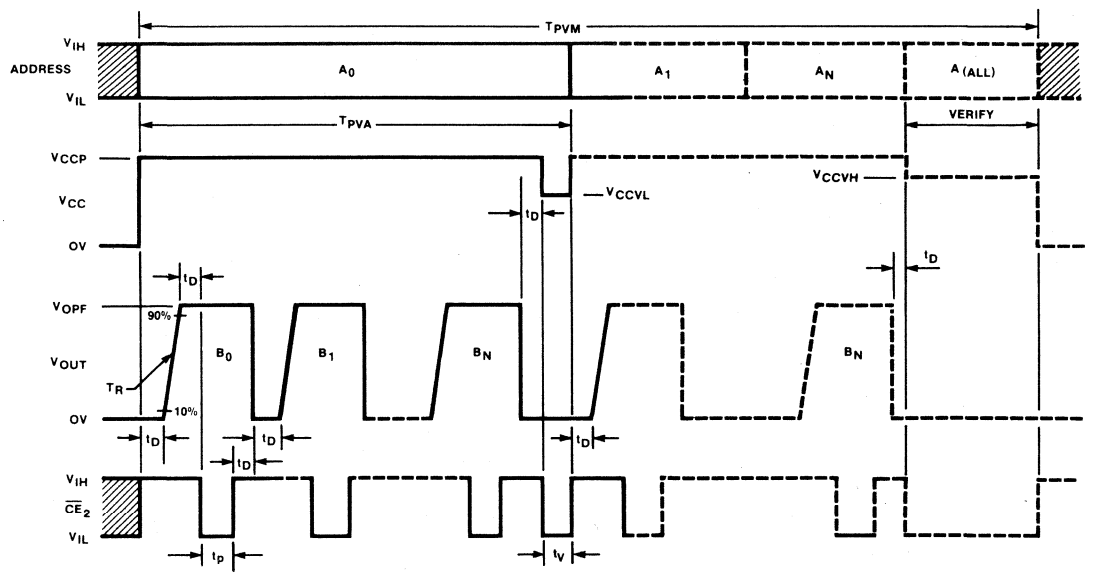
PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150mA, limit voltage spikes to a maximum slew rate of 2V/μs, and 10μs maximum recovery.
4. These are specifications which a Programming System must satisfy in order to be qualified by Signetics. They contain new limits for minimizing total device programming time, which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE}_1$ = Low, $\overline{CE}_2$ = High, CE_3 = High, CE_4 = High.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP}.
3. After t_D delay, apply V_{OPF} to the output to be programmed. Program one output at the time.
4. After t_D delay, pulse the $\overline{CE}_2$ input to logic low for a time t_P.
5. After t_D delay, remove V_{OPF} from the programmed output.
6. Repeat steps 3 through 5 to program other bits at the same address.
7. To verify programming of all bits at the same address, after t_D delay lower V_{CC} to V_{CCVL} and apply a logic low level to the $\overline{CE}_2$ input. All programmed outputs should remain in the logic high state.
8. After t_D delay, repeat steps 2 through 7 to program, and verify all other address locations.
9. After t_D delay raise V_{CC} to V_{CCVH} and verify all memory locations by applying a logic low level to $\overline{CE}_2$, and cycling through all device addresses.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

82LS180-F,N • 82LS181-F,N

DESCRIPTION

The 82LS180 and 82LS181 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82LS180 and 82LS181 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 4 chip enable inputs for ease of memory expansion. They feature either open collector or 3-state outputs for optimization of word expansion in bused organizations.

The 82LS180 and 82LS181 are available in both the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82LS180/181, F or N, and for the military temperature range (−55°C to +125°C) specify S82LS180/181, F.

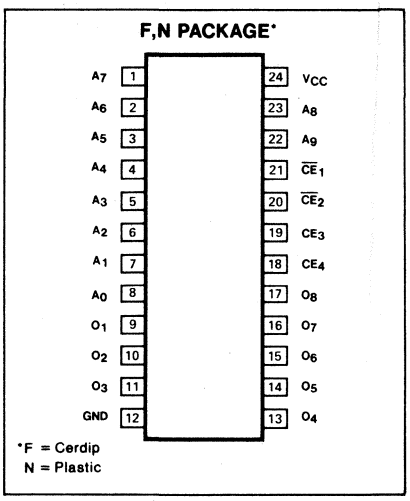
FEATURES

- **Address access time:**
  N82LS180/181: 175ns max
  S82LS180/181: 225ns max
- **Power dissipation: 37μW/bit typ**
- **Input loading:**
  N82LS180/181: −100μA max
  S82LS180/181: −150μA max
- **On-chip address decoding**
- **Output options:**
  82LS180: Open collector
  82LS181: 3-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

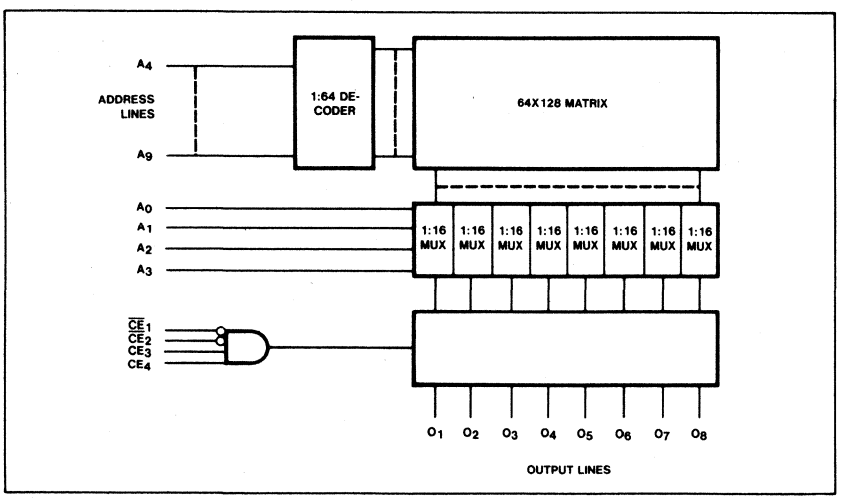
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82LS180)	+5.5	
V_O	Off-state (82LS181)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82LS180/181	0 to +75	
	S82LS180/181	−55 to +125	
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82LS180/181: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82LS180/181: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TEST CONDITIONS[1]		N82LS180/181			S82LS180/181			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage									V
V_{IL}	Low					.85			.80	
V_{IH}	High			2.0			2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$			−0.8	−1.2		−0.8	−1.2	
	Output voltage									V
V_{OL}	Low	$I_{OUT} = 4.8mA$				0.45			0.5	
V_{OH}	High (82LS181)	$\overline{CE}_1$ = low, $I_{OUT} = -1mA$, CE_2 = low, CE_2 = high, $\overline{CE}_4$ = high, high stored		2.4			2.4			
	Input current									μA
I_{IL}	Low	$V_{IN} = 0.45V$				−100			−150	
I_{IH}	High	$V_{IN} = 5.5V$				40			50	
	Output current									
I_{OLK}	Leakage (82LS180)	$\overline{CE}_1 = \overline{CE}_2$ = HIGH, $CE_3 = CE_4$ = LOW	$V_{OUT} = 5.5V$			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82LS181)		$V_{OUT} = 0.5V$			−40			−60	μA
			$V_{OUT} = 5.5V$			40			60	μA
I_{OS}	Short circuit (82LS181)	$\overline{CE}_1 = \overline{CE}_2$ = LOW, $CE_2 = CE_3$ = HIGH	$V_{OUT} = 0V$	−10		−70	−10		−85	mA
I_{CC}	V_{CC} supply current				60	80		60	85	mA
	Capacitance	$V_{CC} = 5.0V$								pF
C_{IN}	Input	$V_{IN} = 2.0V$			5			5		
C_{OUT}	Output	$V_{OUT} = 2.0V$			8			8		

AC ELECTRICAL CHARACTERISTICS

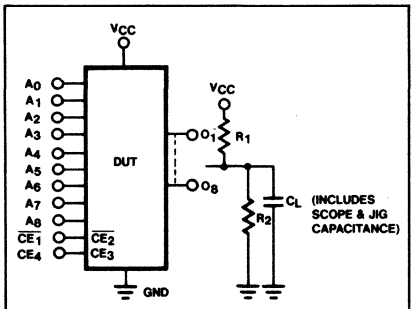
$R_1 = 1k\Omega$, $R_2 = 2k\Omega$, $C_L = 30pF$
N82LS180/181: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82LS180/181: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER	TO	FROM	N82LS180/181			S82LS180/181			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time								ns
T_{AA}	Output	Address		100	175		100	225	
T_{CE}	Output	Chip enable		35	60		35	80	
	Disable time								ns
T_{CD}	Output	Chip disable		35	50		35	70	

NOTES

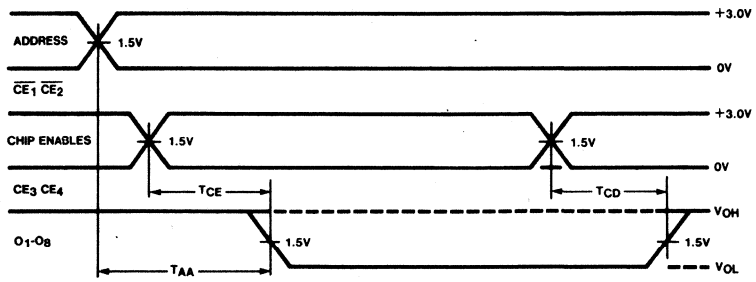
1. Positive current is defined as into the terminal referenced.
2. Typical values are at $V_{CC} = 5.0V$, $T_A = +25°C$.

TEST LOAD CIRCUIT



All inputs: $t_r = t_f = 5ns$ (10% to 90%)

VOLTAGE WAVEFORM



PROGRAMMING SYSTEM SPECIFICATIONS[4] (Testing of these limits may cause programming of device.) $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Power supply voltage					V
V_{CCP}	To program[1]	I_{CCP} = 425 ±75mA, Transient or steady state	8.5		9.0	
	Verify limit					V
V_{CCVH}	Upper		5.3		5.7	
V_{CCVL}	Lower		4.3		4.7	
V_S	Verify threshold[2]		1.4		1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ±.25V	350		500	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0		0.8	
	Input current					µA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			−500	
V_{OPF}	Forced output voltage[3] (program)	I_{OPF} = 200 ±20mA, Transient or steady state	16.0		18.0	V
I_{OPF}	Forced output current (program)	V_{OPF} = +17 ±1V	180		220	mA
T_R	Output pulse rise time		10			µs
t_p	$\overline{CE}$ programming pulse width		100		125	µs
t_D	Pulse sequence delay		5			µs
t_V	$\overline{CE}$ verify pulse width		1			µs
T_{PVA}	Address program verify cycle				1	ms
T_{PVM}	Memory program verify time (continuous)				20	sec
F_L	Fusing attempts per link				1	cycle

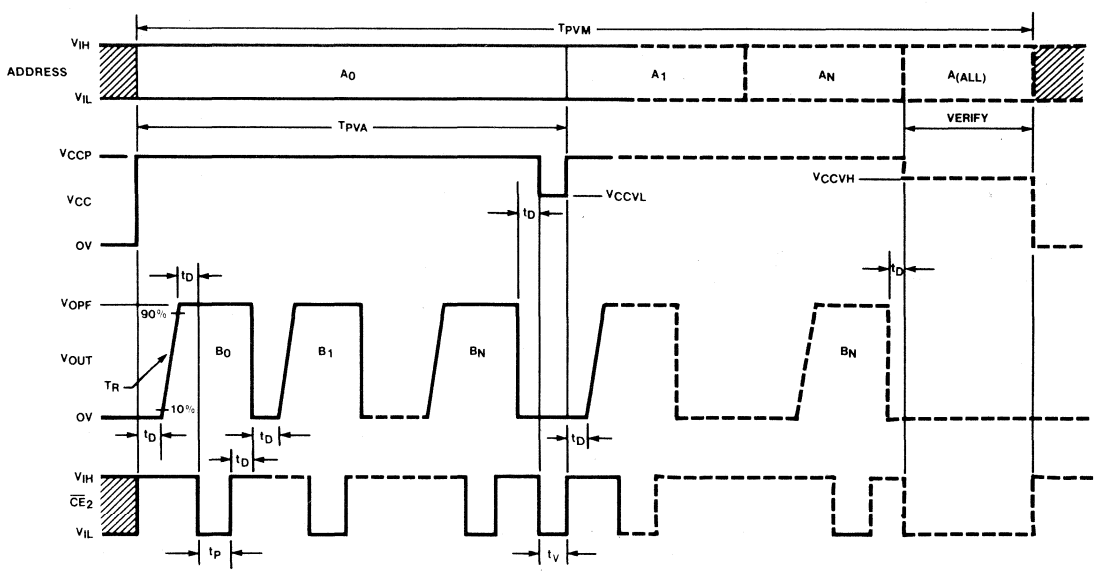
NOTES

1. Bypass V_{CC} to GND with a 0.01µF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150mA, limit voltage spikes to a maximum slew rate of 2V/µs, and 10µs maximum recovery.
4. These are specifications which a Programming System must satisfy in order to be qualified by Signetics. They contain new limits for minimizing total device programming time, which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE}_1$ = Low, $\overline{CE}_2$ = High, CE_3 = High, CE_4 = High.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP}.
3. After t_D delay, apply V_{OPF} to the output to be programmed. Program one output at the time.
4. After t_D delay, pulse the $\overline{CE}_2$ input to logic low for a time t_P.
5. After t_D delay, remove V_{OPF} from the programmed output.
6. Repeat steps 3 through 5 to program other bits at the same address.
7. To verify programming of all bits at the same address after t_D delay, lower V_{CC} to V_{CCVL} and apply a logic low level to the $\overline{CE}_2$ input. All programmed outputs should remain in the logic high state.
8. After t_D delay, repeat steps 2 through 7 to program and verify all other address locations.
9. After t_D delay, raise V_{CC} to V_{CCVH} and verify all memory locations by applying a logic low level to $\overline{CE}_2$, and cycling through all device addresses.

TYPICAL PROGRAMMING SEQUENCE



82S2708-F

DESCRIPTION

The 82S2708 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S2708 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and 1 chip enable input for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

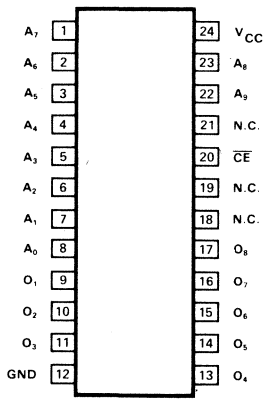
The 82S2708 is available only in the military temperature range. For the military temperature range (-55°C to +125°C) specify S82S2708, F.

FEATURES

- **Address access time:**
  S82S2708: 90ns max
- **Power dissipation: 85μW/bit typ**
- **Input loading:**
  S82S2708: -150μA max
- **Chip enable input**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Pin for pin replacement for 2708 EROM**
- **Fully TTL compatible**

PIN CONFIGURATION

F PACKAGE*

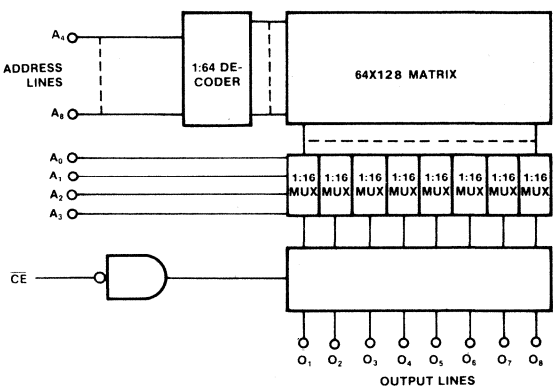


*F = Cerdip
NC = No connection

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High	+5.5	
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	S82S2708	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

S82S2708: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	S82S2708 Min	S82S2708 Typ[2]	S82S2708 Max	UNIT
	Input voltage					V
V_{IL}	Low				.80	
V_{IH}	High		2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2	
	Output voltage					V
V_{OL}	Low	I_{OUT} = 9.6mA			0.5	
V_{OH}	High	I_{OUT} = -2.0mA, $\overline{CE}$ = Low, High stored	2.4			
	Input current					μA
I_{IL}	Low	V_{IN} = 0.45V			-150	
I_{IH}	High	V_{IN} = 5.5V			50	
	Output current					
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}$ = High, V_{OUT} = 0.5V			-60	μA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			60	
I_{OS}	Short circuit	V_{OUT} = 0V	-15		-85	mA
I_{CC}	V_{CC} supply current			140	185	mA
	Capacitance	V_{CC} = 5.0V				pF
C_{IN}	Input	V_{IN} = 2.0V		5		
C_{OUT}	Output	V_{OUT} = 2.0V		8		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, C_L = 30pF

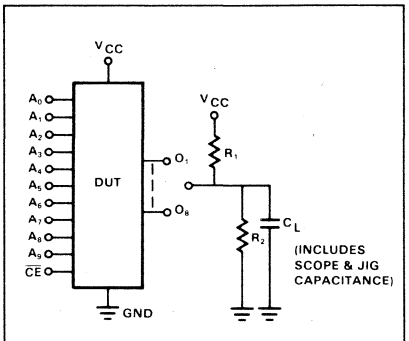
S82S2708: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	S82S2708 Min	S82S2708 Typ[2]	S82S2708 Max	UNIT
	Access time						ns
T_{AA}		Output	Address		50	90	
T_{CE}		Output	Chip enable		20	50	
	Disable time						ns
T_{CD}		Output	Chip disable		20	50	

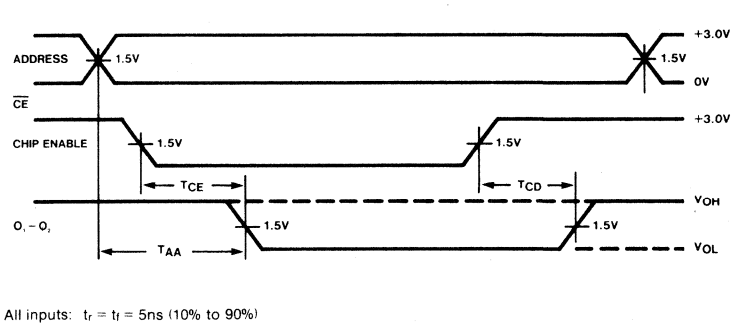
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are V_{CC} = 5.0V, T_A = +25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs: $t_r = t_f$ = 5ns (10% to 90%)

PROGRAMMING SYSTEM SPECIFICATIONS[4] (Testing of these limits may cause programming of device.) T_A = +25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1]	I_{CCP} = 425 ± 75mA, Transient or steady state	8.5		9.0	V
	Verify limit					V
V_{CCVH}	Upper		5.3		5.7	
V_{CCVL}	Lower		4.3		4.7	
V_S	Verify threshold[2]		1.4		1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	350		500	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0		0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			-500	
V_{OPF}	Forced Output Voltage[3] (program)	I_{OPF} = 200 ± 20mA, Transient or steady state	16.0		18.0	V
I_{OPF}	Forced Output Current (program)	V_{OPF} = +17 ± 1V	180		220	mA
T_R	Output pulse rise time		10			μs
t_P	$\overline{CE}$ programming pulse width		100		125	μs
t_D	Pulse sequence delay		5			μs
t_V	$\overline{CE}$ verify pulse width		1			μs
T_{PVA}	Address program-verify cycle				1	ms
T_{PVM}	Memory program-verify time (continuous)				20	sec
F_L	Fusing attempts per link				1	cycle

PROGRAMMING NOTES

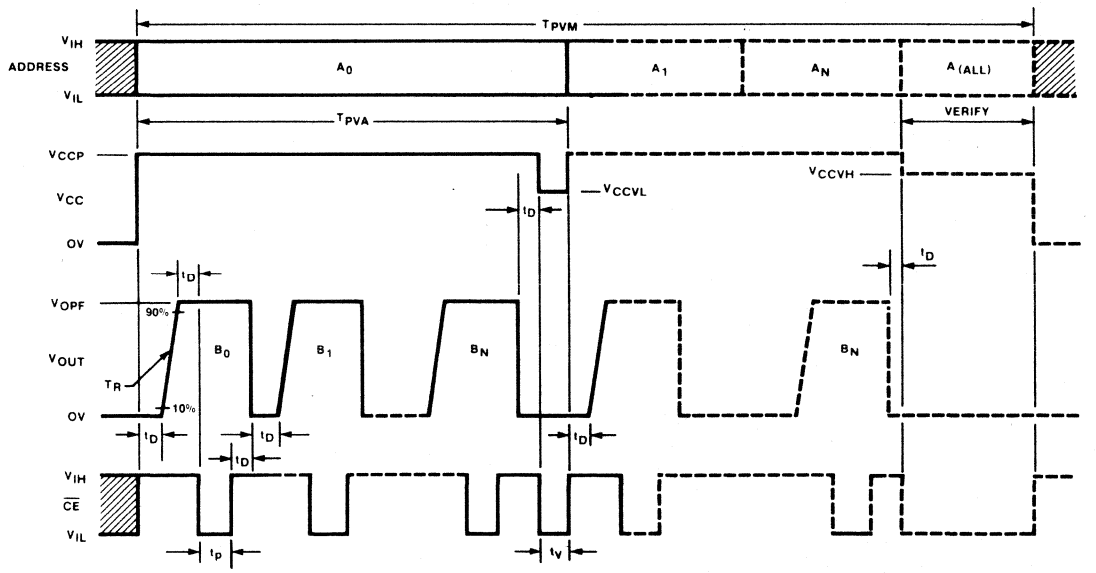
1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150mA, limit voltage spikes to a maximum slew rate of 2V/μs, and 10μs maximum recovery.
4. These are specifications which a programming system must satisfy in order to be qualified by Signetics. They contain new limits for minimizing total device programming time, which supercedes, but do not obsolete the performance requirements of previously manufactured programming equipment.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE}$ = High.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP}.
3. After t_D delay, apply V_{OPF} to the output to be programmed. Program one output at the time.
4. After t_D delay, pulse the $\overline{CE}$ input to logic low for a time t_P.
5. After t_D delay, remove V_{OPF} from the programmed output.
6. Repeat steps 3 through 5 to program other bits at the same address.
7. To verify programming of all bits at the same address, after t_D delay lower V_{CC} to V_{CCVL} and apply a logic low level to the $\overline{CE}$ input. All programmed outputs should remain in the logic high state.
8. After t_D delay, repeat steps 2 through 7 to program, and verify all other address locations.
9. After t_D delay raise V_{CC} to V_{CCVH} and verify all memory locations by applying a logic low level to $\overline{CE}$, and cycling through all device addresses.

82S2708-F

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

DESCRIPTION

The 82S182 and 82S183 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S182 and 82S183 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

A D-type latch is used to enable the tri-state output drivers. In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe high. In this mode the output drivers are controlled solely by $\overline{CE}_1$, $\overline{CE}_2$, and CE_3 lines.

In the Latched Read mode, outputs are held in their previous state (high, low, or high Z) as long as Strobe is low, regardless of the state of address or chip enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the high Z state if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the high Z condition if the chip was disabled.

The 82S182 and 82S183 are available in both the commerical and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S182/183, for F or N, and for the military temperature range (−55°C to 125°C) specify S82S182/183, F.

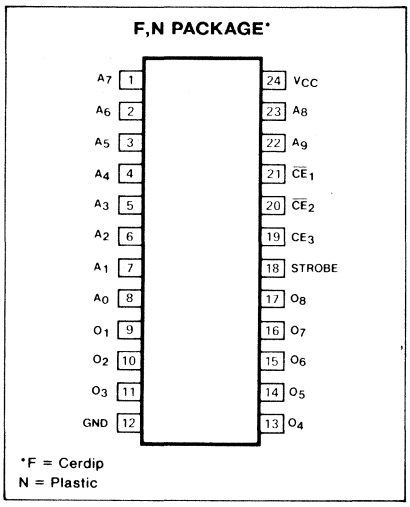
FEATURES

- **Address access time:**
  N82S182/183: 60ns max
  S82S182/183: 90ns max
- **Power dissapation: 85μW/bit typ**
- **Input loading:**
  N82S182/183: −100μA max
  S82S182/183: −150μA max
- **On-chip address decoding**
- **Output options:**
  82S182: Open collector
  82S183: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

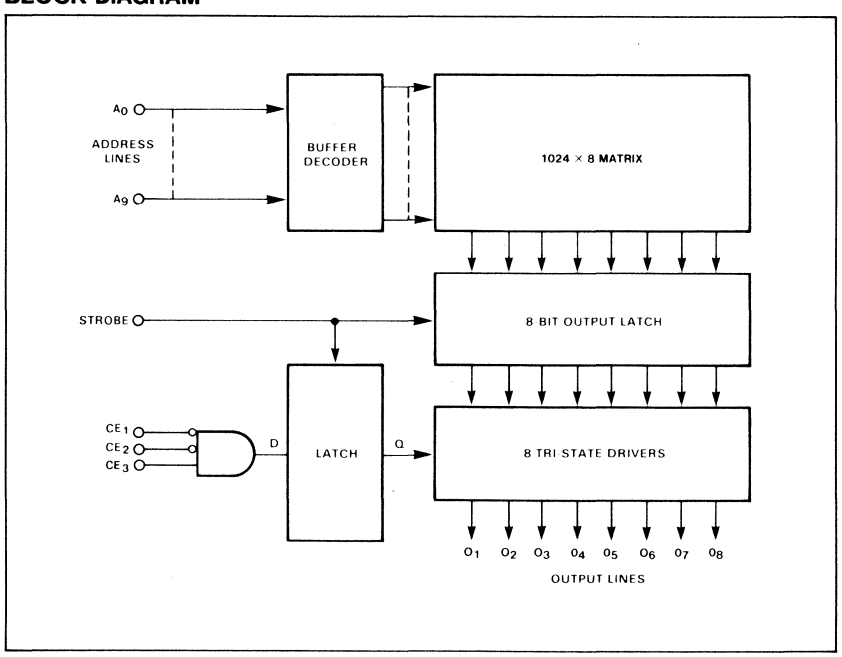
- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



*F = Cerdip
N = Plastic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Temperature range		°C
T_A	Operating		
	N82S182/3	0 to +75	
	S82S183/3	−55 to +125	
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S182/3: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

S82S182/3: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TEST CONDITIONS[6]	N82S 182/3			S82S 182/3			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
	Input voltage								V
V_{IL}	Low				.85			.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$		−0.8	−1.2		−0.8	−1.2	
	Output voltage								V
V_{OL}	Low	$I_{OUT} = 9.6mA$		0.4	0.45		0.4	0.5	
V_{OH}	High	$\overline{CE}$ = Low, CE = High, $I_{OUT} = -2mA$, High stored	2.7	3.3		2.4	3.3		
	Input current[6]								μA
I_{IL}	Low	$V_{IN} = 0.45V$			−100			−150	
I_{IH}	High	$V_{IN} = 5.5V$			25			50	
	Output current[6]								
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}$ = High or CE = O, $V_{OUT} = 5.5V$			40			100	μA
		$\overline{CE}$ = High or CE = O, $V_{OUT} = 0.5V$			−40			−100	
I_{OS}	Short circuit[2]	$V_{OUT} = OV$	−20		−70	−15		−85	mA
I_{CC}	V_{CC} supply current			130	175		130	185	mA
	Capacitance	$V_{CC} = 5.0V$, $V_{IN} = 2.0V$							pF
C_{IN}	Input	$V_{CC} = 5.0V$, $V_{OUT} = 2.0V$		5			5		
C_{OUT}	Output	$\overline{CE}$ = High or CE = 0		8			8		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$

N82S182/3: $0° \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

S82S182/3: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

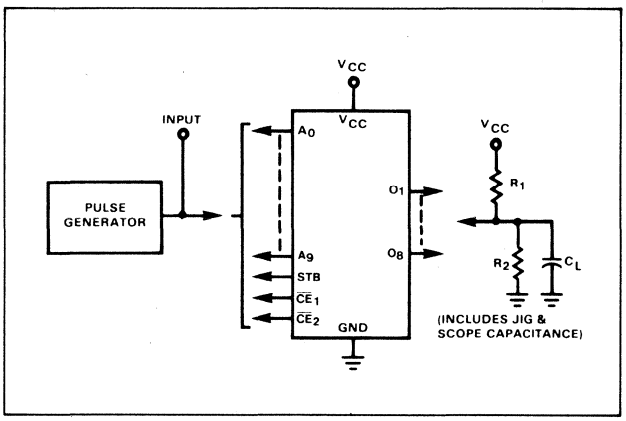
PARAMETER		TO	FROM	TEST CONDITIONS	N82S182/3			S82S182/3			UNIT
					Min	Typ[1]	Max	Min	Typ[1]	Max	
	Access time[3]			Latched or transparent read							ns
T_{AA}		Output	Address			35	60		35	90	
T_{CE}		Output	Chip enable			20	40		20	50	
T_{CD}	Disable time[3]	Output	Chip disable	Latched or transparent read		20	40		20	50	ns
	Setup and hold time[4]			Latched read only							ns
T_{CDS}	Setup time	Output	Chip enable		40			50			
T_{CDH}	Hold time				10	0		10	0		
T_{ADH}	Hold time	Output	Address		0	−10		5	−10		
	Pulse width[4]			Latched read only							ns
T_{SW}	Strobe				30	20		40	20		
	Latch time[4]			Latched read only							ns
T_{SL}	Strobe				60	35		90	35		
	Delatch time[4]			Latched read only							ns
T_{DL}	Strobe						30			35	

NOTES on following page.

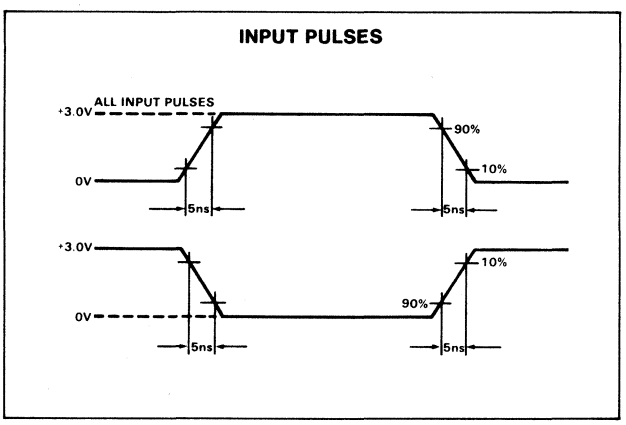
NOTES

1. Typical values are at V_{CC} = +5.0V and T_A = +25°C.
2. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in high state.
3. If the strobe is high, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid date will appear T_{AA} nanoseconds after the address has changed the T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an off or high impedance state after it has been enabled.
4. In Latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.
5. During operation the fusing pins FE1 and FE2 may be grounded or left floating.
6. Positive current is defined as into the terminal referenced.

TEST LOAD CIRCUIT

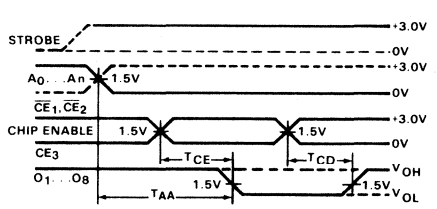


VOLTAGE WAVEFORM



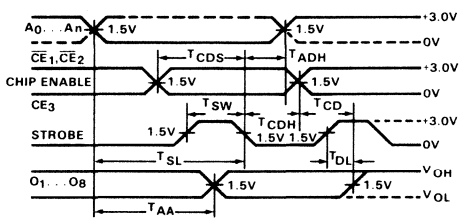
TIMING DIAGRAMS

TRANSPARENT READ[4]



Output Latches Not Used

LATCHED READ[5]



Output Latches Used

PROGRAMMING SYSTEM SPECIFICATIONS[4] (Testing of these limits may cause programming of device.) T_A = +25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1]	I_{CCP} = 425 ± 75 mA, Transient or steady state	8.5		9.0	V
	Verify limit					V
V_{CCVH}	Upper		5.3		5.7	
V_{CCVL}	Lower		4.3		4.7	
V_S	Verify threshold[2]		1.4		1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	350		500	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0		0.8	
	Input current					µA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			−500	
V_{OPF}	Forced output voltage[3] (program)	I_{OPF} = 200 ± 20 mA, Transient or steady state	16.0		18.0	V
I_{OPF}	Forced output current (program)	V_{OPF} = +17 ± 1V	180		220	mA
T_R	Output pulse rise time		10			µs
t_p	$\overline{CE}$ programming pulse width		100		125	µs
t_D	Pulse sequence delay		5			µs
t_V	$\overline{CE}$ verify pulse width		1			µs
T_{PVA}	Address program-verify cycle				2	ms
T_{PVM}	Memory program-verify time (continuous)				20	sec
F_L	Fusing attempts per link				1	cycle

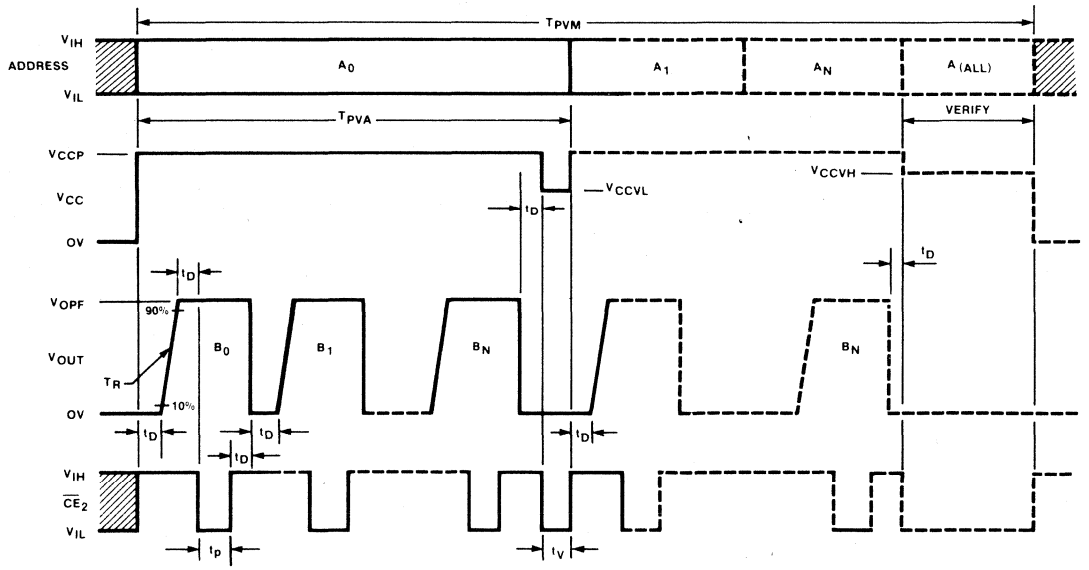
PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01µF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150 mA, limit voltage spikes to a maximum slew rate of 2V/µs, and 10 µs maximum recovery.
4. These are specifications which a Programming System must satisfy in order to be qualified by Signetics. They contain new limits for minimizing total device programming time, which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with 10kΩ resistor to V_{CC}. Set CE_3 = $\overline{CE}_2$ = Strobe = High, and $\overline{CE}_1$ = Low.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP}.
3. After t_D delay, apply V_{OPF} to the output to be programmed. Program one output at the time.
4. After t_D delay, pulse the $\overline{CE}_2$ input to logic low for a time t_p.
5. After t_D delay, remove V_{OPF} from the programmed output.
6. Repeat steps 3 through 5 to program other bits at the same address.
7. To verify programming of all bits at the same address after t_D delay lower V_{CC} to V_{CCVL} and apply a logic low level to the $\overline{CE}_2$ input. All programmed outputs should remain in the logic high state.
8. After t_D delay, repeat steps 2 through 7 to program, and verify all other address locations.
9. After t_D delay raise V_{CC} to V_{CCVH} and verify all memory locations by applying a logic low level to $\overline{CE}_2$, and cycling through all device addresses.

TYPICAL PROGRAMMING SEQUENCE



DESCRIPTION

The 82S184 and 82S185 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S184 and 82S185 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

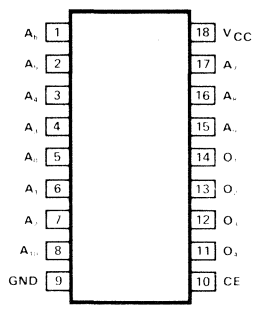
These devices include on-chip decoding and 1 chip enable input for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S184 and 82S185 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C specify N82S184/185, I, and for the military temperature range (-55°C to +125°C) specify S82S184/185, I.

FEATURES

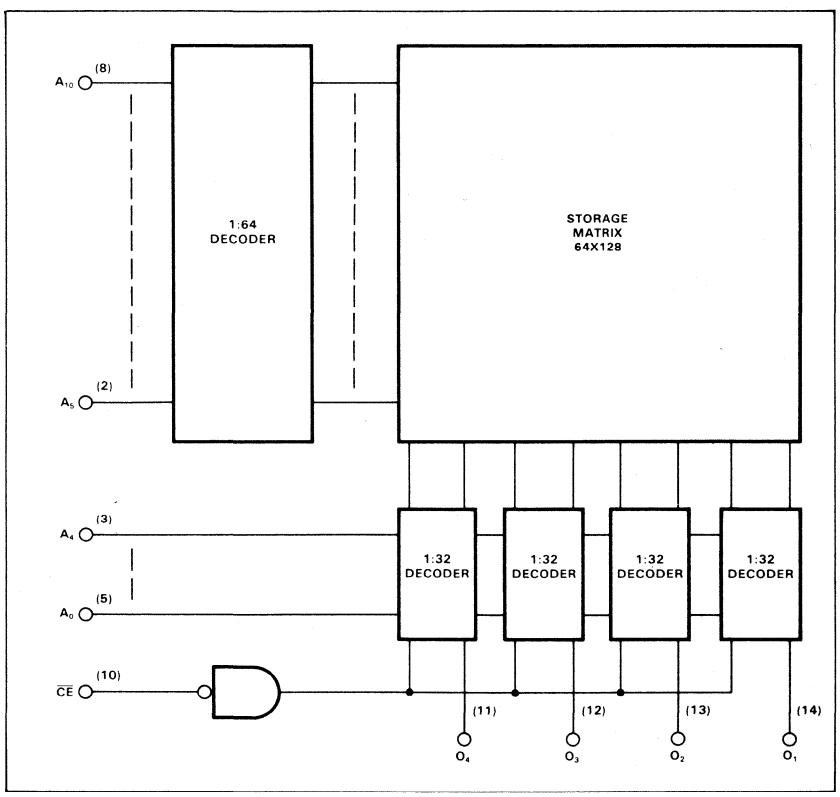
- **Low power dissipation: 50μW/bit typ**
- **Address access time:**
  - **N82S184/185: 100ns max**
  - **S82S184/185: 150ns max**
- **Input loading:**
  - **N82S184/185: -100μA max**
  - **S82S184/185: -150μA max**
- **On-chip address decoding**
- **Output options:**
  - **82S184: Open collector**
  - **82S185: Tri-state**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

I PACKAGE*



*I = Cerdip

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S184)	+5.5	
V_O	Off-state (82S185)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S184/185	0 to +75	
	S82S184/185	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S184/185: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S184/185: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1,3]	N82S184/185			S82S184/185			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage[1]								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage[1]								V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High (82S185)	$\overline{CE}$ = Low, I_{OUT} = -2mA, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN}= 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}	Leakage (82S184)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40			60	μA
I_O (OFF)	Hi-Z state (82S185)	$\overline{CE}$ = High, V_{OUT} = 0.5V			-40			-60	μA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			40			60	
I_{OS}	Short circuit (82S185)[4]	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			80	120		80	130	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

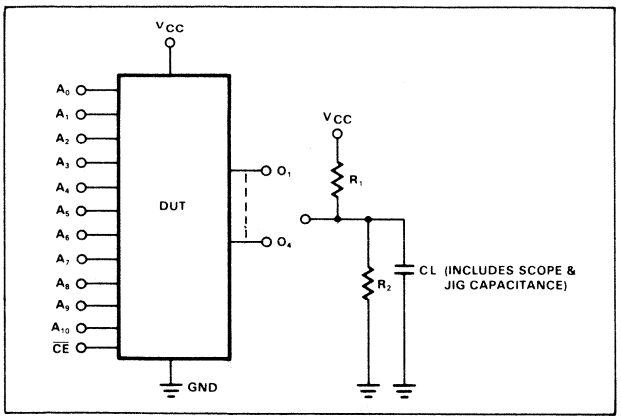
$R_1 = 270\Omega$, $R_2 = 600\Omega$, C_L = 30pF
N82S184/185: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S184/185: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S184/185			S82S184/185			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time									ns
T_{AA}[5]	Output	Address		70	100		70	125	
T_{CE}	Output	Chip enable		30	40		30	60	
Disable time									ns
T_{CD}	Output	Chip disable		30	40		30	60	

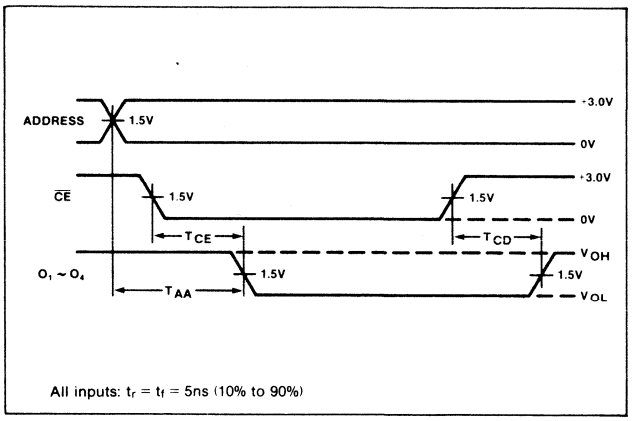
NOTES

1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Positive current is defined as into the terminal referenced.
4. Duration of the short circuit should not exceed 1 second.
5. Tested at an address cycle time of 1μsec.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



PROGRAMMING SYSTEM SPECIFICATIONS[4] (Testing of these limits may cause programming of device.) T_A = +25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1]	I_{CCP} = 425 ± 75mA, Transient or steady state	8.5		9.0	V
	Verify limit					V
V_{CCVH}	Upper		5.3		5.7	
V_{CCVL}	Lower		4.3		4.7	
V_S	Verify threshold[2]		1.4		1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	350		500	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0		0.8	
	Input current					µA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			-500	
V_{OPF}	Forced Output Voltage[3] (program)	I_{OPF} = 200 ± 20mA, Transient or steady state	16.0		18.0	V
I_{OPF}	Forced Output Current (program)	V_{OPF} = +17 ± 1V	180		220	mA
T_R	Output pulse rise time		10			µs
t_P	$\overline{CE}$ programming pulse width		100		125	µs
t_D	Pulse sequence delay		5			µs
t_V	$\overline{CE}$ verify pulse width		1			µs
T_{PVA}	Address program-verify cycle				1	ms
T_{PVM}	Memory program-verify time (continuous)				20	sec
F_L	Fusing attempts per link				1	cycle

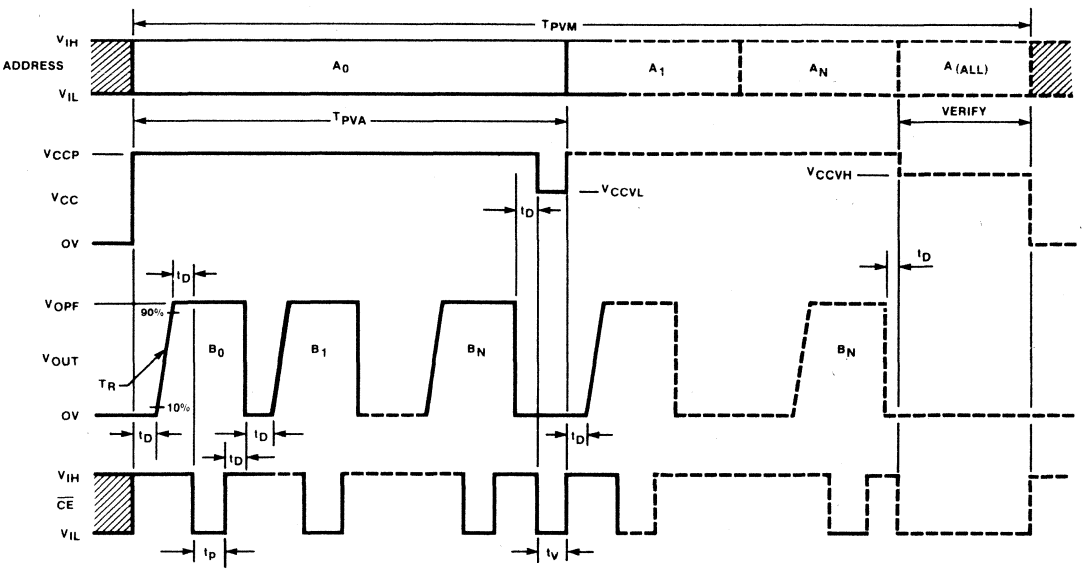
PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150mA, limit voltage spikes to a maximum slew rate of 2V/μs, and 10μs maximum recovery.
4. These are specifications which a Programming System must satisfy in order to be qualified by Signetics. They contain new limits for minimizing total device programming time, which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE}$ = High.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP}.
3. After t_D delay, apply V_{OPF} to the output to be programmed. Program one output at the time
4. After t_D delay, pulse the $\overline{CE}$ input to logic low for a time t_P.
5. After t_D delay, remove V_{OPF} from the programmed output.
6. Repeat steps 3 through 5 to program other bits at the same address.
7. To verify programming of all bits at the same address, after t_D delay lower V_{CC} to V_{CCVL} and apply a logic low level to the $\overline{CE}$ input. All programmed outputs should remain in the logic high state.
8. After t_D delay, repeat steps 2 through 7 to program, and verify all other address locations.
9. After t_D delay raise V_{CC} to V_{CCVH} and verify all memory locations by applying a logic low level to $\overline{CE}$, and cycling through all device addresses.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

82S190-I • 82S191-I

DESCRIPTION

The 82S190 and 82S191 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S190 and 82S191 are supplied with all outputs at a logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 3 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S190 and 82S191 devices are available in the commercial and military ranges. For the commercial temperature range (0°C to +75°C) specify N82S190/191, I, and for the military temperature range (-55°C to +125°C) specify S82S190/191, I.

FEATURES

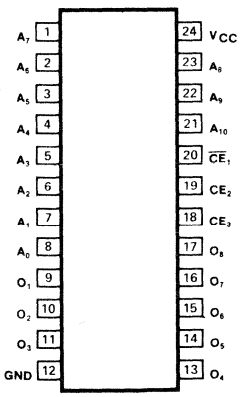
- **Address access time:**
  N82S190/191: 80ns max
  S82S190/: 100ns max
- **Power dissipation : 40μW/bit typ**
- **Input loading:**
  N82S190/191: -100μA max
  S82S190/191: -150μA max
- **3 chip enable inputs**
- **On-chip address decoding**
- **Output options:**
  82S190: Open collector
  82S191: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

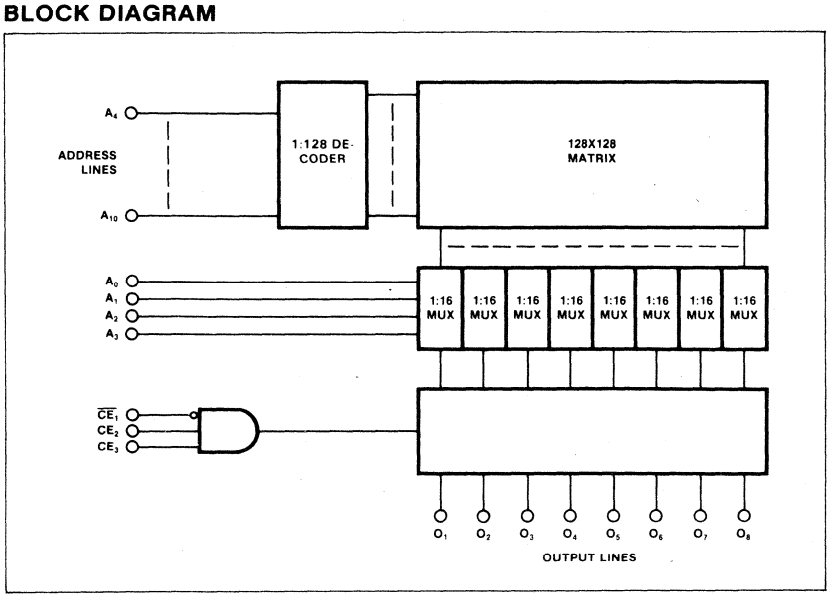
PIN CONFIGURATION

I PACKAGE*



*I = Ceramic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S140)	+5.5	
V_O	Off-state (82S141)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S190/191	0 to +75	
	S82S190/191	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S190/191: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S190/191: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	N82S190/191			S82S190/191			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 9.6mA			0.45			0.5	
V_{OH}	High (82S191)	I_{OUT} = -2mA, $\overline{CE_1}$ = Low, CE_2 = High, CE_3 = High, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}	Leakage (82S190)	V_{OUT} = 5.5V, $\overline{CE_1}$ = High, CE_2 = Low, $\overline{CE_3}$ = Low			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S191)	V_{OUT} = 0.5V, $\overline{CE_1}$ = High, CE_2 = Low, $\overline{CE_3}$ = Low			-40			-60	μA
		V_{OUT} = 5.5V, $\overline{CE_1}$ = High, CE_2 = Low, CE_3 = Low			40			60	
I_{OS}	Short circuit (82S191)	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			130	175		130	185	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

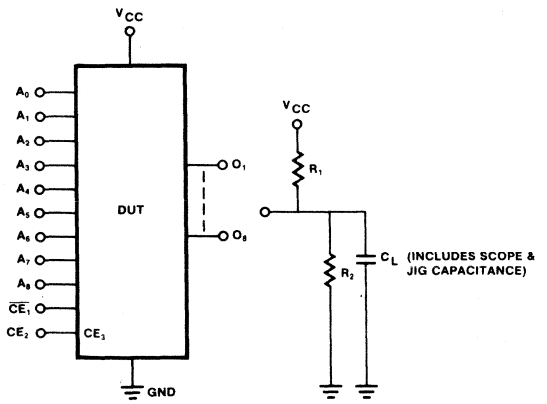
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, C_L = 30pF
N82S190/191: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S190/191: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S190/191			S82S190/191			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time									ns
T_{AA}[3]	Output	Address		50	80		50	100	
T_{CE}	Output	Chip enable		20	40		20	50	
Disable time									ns
T_{CD}	Output	Chip disable		20	40		20	50	

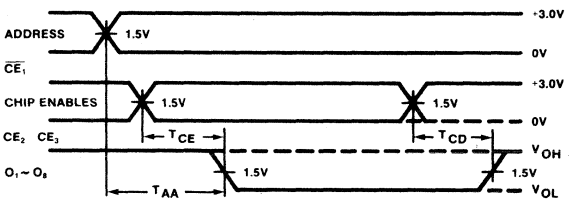
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.
3. Tested at an address cycle time of 1μsec.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs: $t_r = t_f = 5ns$ (10% to 90%)

PROGRAMMING SYSTEM SPECIFICATIONS[4] (Testing of these limits may cause programming of device.) T_A = +25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1]	I_{CCP} = 425 ± 75mA, Transient or steady state	8.5		9.0	V
	Verify limit					V
V_{CCVH}	Upper		5.3		5.7	
V_{CCVL}	Lower		4.3		4.7	
V_S	Verify threshold[2]		1.4		1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	350		500	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0		0.8	
	Input current					µA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			-500	
V_{OPF}	Forced Output Voltage[3] (program)	I_{OPF} = 200 ± 20mA, Transient or steady state V_{OPF} = +17 ± 1V	16.0		18.0	V
I_{OPF}	Forced Output Current (program)		180		220	mA
T_R	Output pulse rise time		10			µs
t_p	$\overline{CE}$ programming pulse width		100		125	µs
t_D	Pulse sequence delay		5			µs
t_V	$\overline{CE}$ verify pulse width		1			µs
T_{PVA}	Address program-verify cycle				1	ms
T_{PVM}	Memory program-verify time (continuous)				20	sec
F_L	Fusing attempts per link				1	cycle

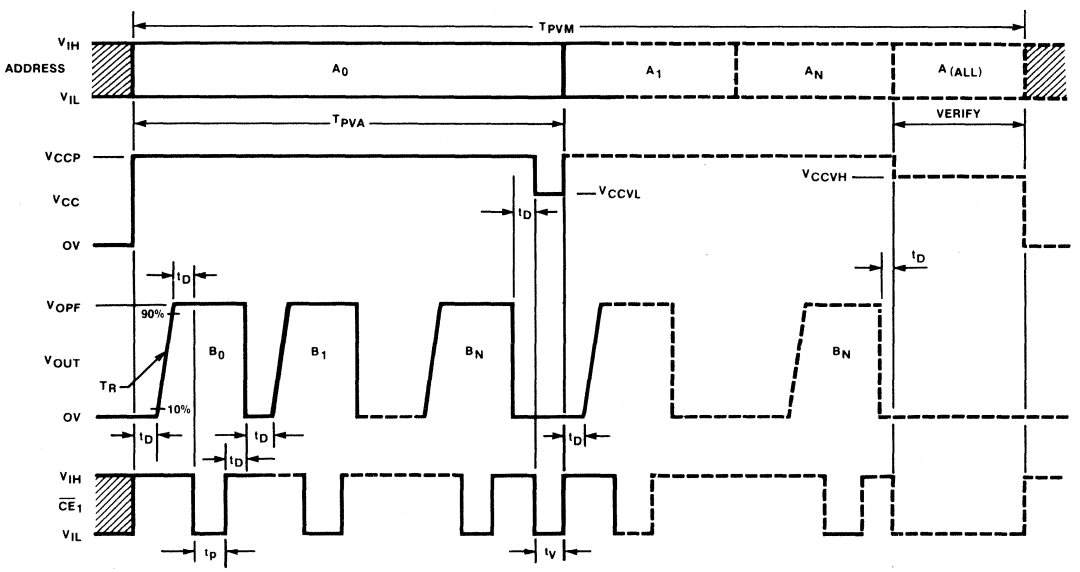
PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current to 150mA, limit voltage spikes to a maximum slew rate of 2V/μs, and 10μs maximum recovery.
4. These are specifications which a Programming System must satisfy in order to be qualified by Signetics. They contain new limits for minimizing total device programming time, which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE}_1$ = High, CE_2 = High, CE_3 = High.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP}.
3. After t_D delay, apply V_{OPF} to the output to be programmed. Program one output at the time.
4. After t_D delay, pulse the $\overline{CE}_1$ input to logic low for a time t_P.
5. After t_D delay, remove V_{OPF} from the programmed output.
6. Repeat steps 3 through 5 to program other bits at the same address.
7. To verify programming of all bits at the same address, after t_D delay lower V_{CC} to V_{CCVL} and apply a logic low level to the $\overline{CE}_1$ input. All programmed outputs should remain in the logic high state.
8. After t_D delay, repeat steps 2 through 7 to program, and verify all other address locations.
9. After t_D delay raise V_{CC} to V_{CCVH} and verify all memory locations by applying a logic low level to $\overline{CE}_1$, and cycling through all device addresses.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

DESCRIPTION

The 82S200 (tri-state outputs) and the 82S201 (open collector outputs) are Bipolar Programmable Logic Arrays, containing 48 product terms (AND terms), and 8 sum terms (OR tems). Each OR term controls an output function which can be programmed either true active-high (F_P), or true active-low (F_P^*). The true state of each output function is activated by any logical combination of 16-input variables, or their complements, up to 48 terms. Both devices are mask programmable by supplying to Signetics Program Table data in one of the formats specified in this data sheet.

The 82S200 and 82S201 are fully TTL compatible, and include chip enable control for expansion of input variables, and output inhibit. They feature either open collector or tri-state outputs for ease of expansion of product terms and application in bus-organized systems.

Both devices are available in commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S200/201, I or N, and for the military temperature range (-55°C to +125°C) specify S82S200/201, I.

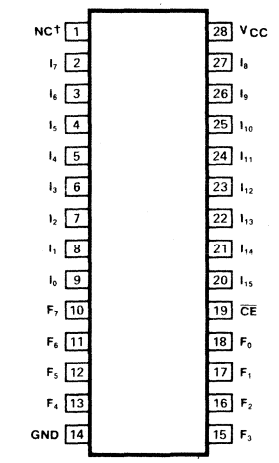
APPLICATIONS*

- **CRT display systems**
- **Random logic**
- **Code conversion**
- **Peripheral controllers**
- **Function generators**
- **Look-up and decision tables**
- **Microprogramming**
- **Address mapping**
- **Character generators**
- **Sequential controllers**
- **Data security encoders**
- **Fault detectors**
- **Frequency synthesizers**

*For diagrams of Typical Applications reference 82S100 (T.S.)/82S101 (O.C.) Data Sheet.

PIN CONFIGURATION

I,N PACKAGE*



*I = Ceramic
N = Plastic
†Open during normal operation

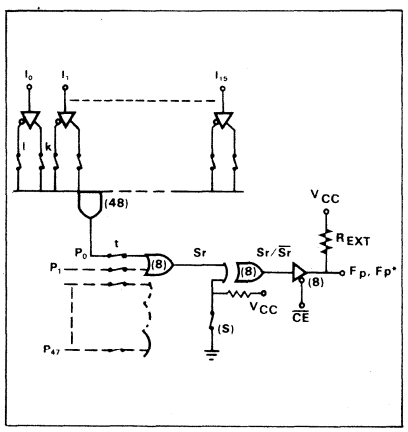
TRUTH TABLE

MODE	Pn	$\overline{CE}$	Sr ? f(Pn)	Fp	F_p^*
Disabled (82S201)	X	1	X	1	1
Disabled (82S200)				Hi-Z	Hi-Z
Read	1	0	Yes	1	0
	0	0		0	1
	X	0	No	0	1

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

PLA EQUIVALENT LOGIC PATH



LOGIC FUNCTION

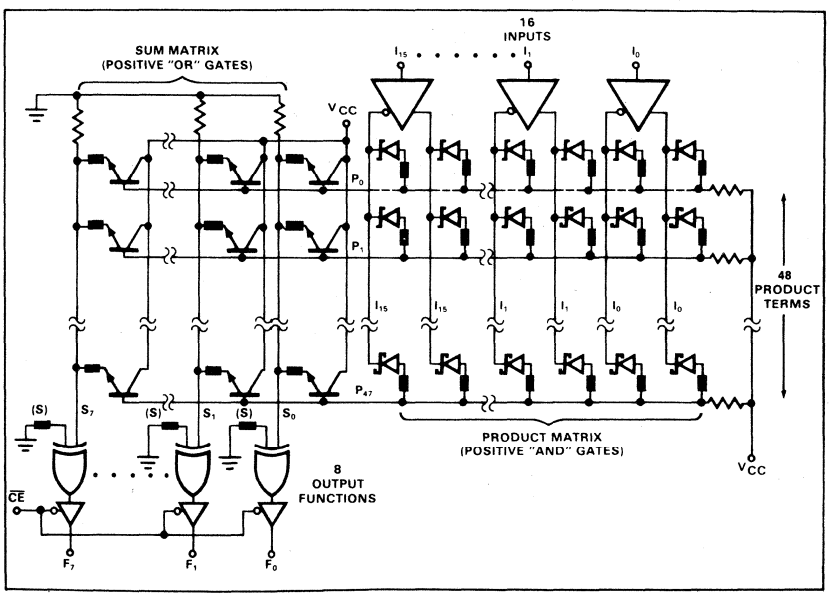
Typical Product Term:
$P_0 = I_0 \bullet I_1 \bullet \overline{I_2} \bullet I_5 \bullet \overline{I_{13}}$

Typical Output Functions:
$F_0 = (\overline{CE}) + (P_0 + P_1 + P_2)$ @ S = Closed
$F_0^* = (\overline{CE}) + (\overline{P_0} \bullet \overline{P_1} \bullet \overline{P_2})$ @ S = Open

NOTE

For each of the 8 outputs, either the function Fp (active-high) or $F\dot{p}$ (active low) is available, but not both. The required function polarity is programmed via link (S).

LOGIC DIAGHAM



ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER		RATING		UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			°C
T_A	Operating			
	N82S200/201	0	+75	
	S82S200/201	-55	+125	
T_{STG}	Storage	-65	+150	

DC ELECTRICAL CHARACTERISTICS

N82S200/201: $0° \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S200/201: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TEST CONDITIONS	N82S200/201			S82S200/201			UNIT
			Min	Typ [2]	Max	Min	Typ [2]	Max	
	Input voltage[3]								V
V_{IH}	High	V_{CC} = Max	2			2			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp[3,4]	V_{CC} = Min, I_{IN} 7 -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage	V_{CC} = Min							V
V_{OH}	High (82S200)[3,5]	I_{OH} = -2mA	2.4			2.4			
V_{OL}	Low[3,6]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
	Input current								μA
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage[7]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S200)[7]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		-1	-40		-1	-60	
I_{OS}	Short circuit (82S200)[4,8]	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} Max		120	170		120	180	mA
	Capacitance[7]	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output	V_{OUT} = 2.0V		17			17		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$

N82S200/201: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

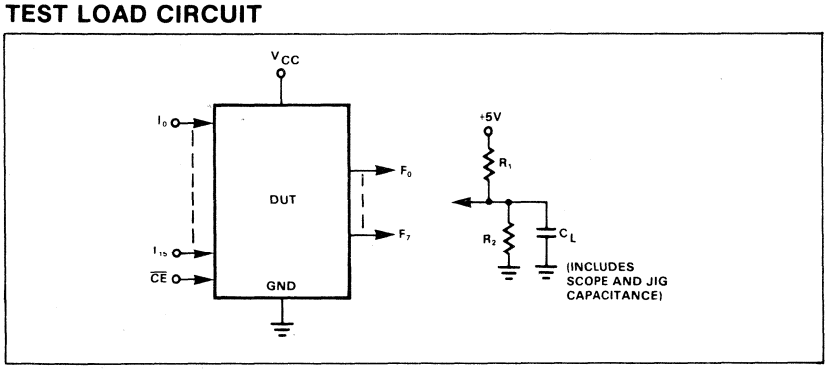
S82S200/201: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TO	FROM	N82S200/201			S82S200/201			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time									ns
T_{IA}	Input	Output	Input		35	50		35	80	
T_{CE}	Chip enable	Output	Chip enable		15	30		15	50	
	Disable time									ns
T_{CD}	Chip disable	Output	Chip enable		15	30		15	50	

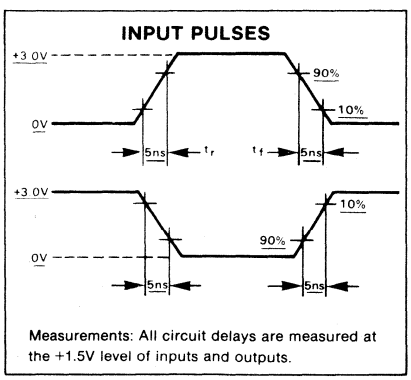
NOTES

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation of the device specifications is not implied.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. All voltage values are with respect to network ground terminal.
4. Test one at the time.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
6. Measured with a programmed logic condition for which the output test is at a low logic level. Output sink current is applied thru a resistor to V_{CC}.
7. Measured with: V_{IH} applied to $\overline{CE}$.
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

TEST LOAD CIRCUIT

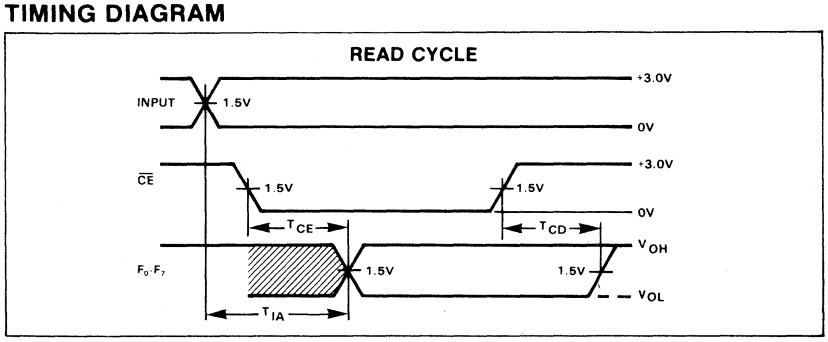


VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the +1.5V level of inputs and outputs.

TIMING DIAGRAM



TIMING DEFINITIONS

T_{CE} Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.

T_{CD} Delay between when Chip Enable becomes high and Data Output is in off state (Hi-Z or high).

T_{IA} Delay between beginning of valid Input (with Chip Enable low) and when Data Output becomes valid.

16X48X8 PLA PROGRAM TABLE

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) _____

CUSTOMER SYMBOLIZED PART # _____

DATE RECEIVED _____

COMMENTS _____

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____

REV _____ DATE _____

PROGRAM TABLE ENTRIES						
INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
Im	$\overline{Im}$	Don't Care	Prod. Term Present in F_P	Prod. Term Not Present in F_P	Active High	Active Low
H	L	— (dash)	A	• (period)	H	L
NOTE Enter (—) for unused inputs of used P-terms.			NOTES 1. Entries independent of output polarity 2. Enter (A) for unused outputs of used P-terms		NOTES 1. Polarity programmed once only 2. Enter (H) for all unused outputs.	

NO.	PRODUCT TERM* INPUT VARIABLE*																ACTIVE LEVEL* OUTPUT FUNCTION*							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0																								
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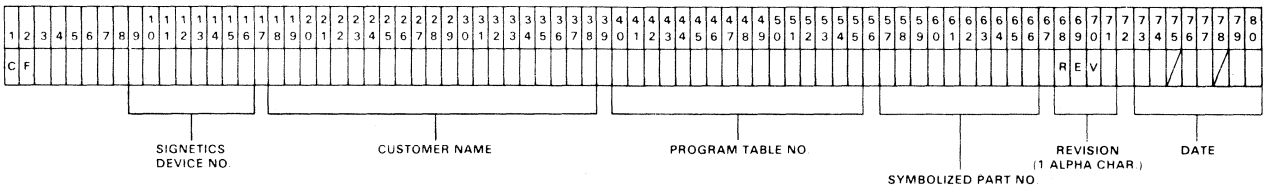
47																								

*Input and Output fields of unused P-terms can be left blank. Unused inputs and outputs are PLA terminals left floating.

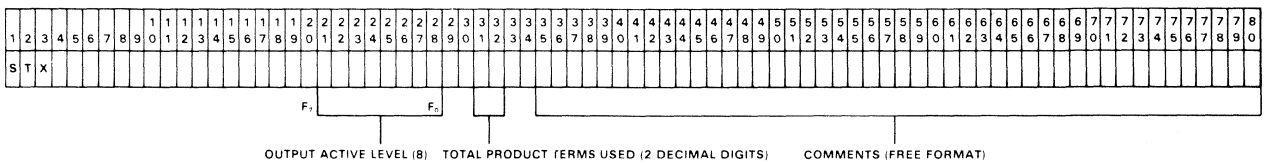
PUNCHED CARD CODING FORMAT

The PLA Program Table can be supplied directly to Signetics in punched card form, using standard 80-column IBM cards. For each PLA Program Table, the customer should prepare an input card deck in accordance with the following format. Product Term cards 3 through 50 can be in any order. Not all 48 Product Terms need to be present. Unused Product Terms require no entry cards, and will be skipped during the actual programming sequence:

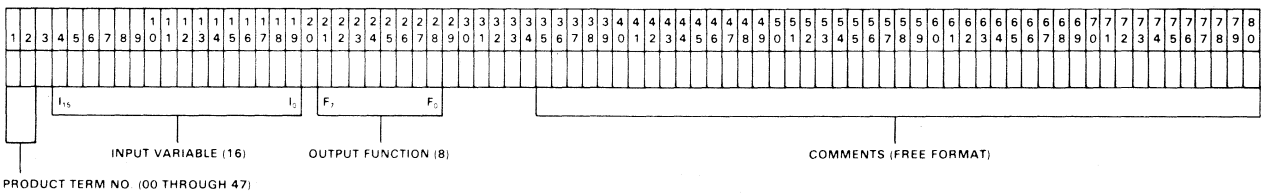
CARD NO.1—Free format within designated fields.



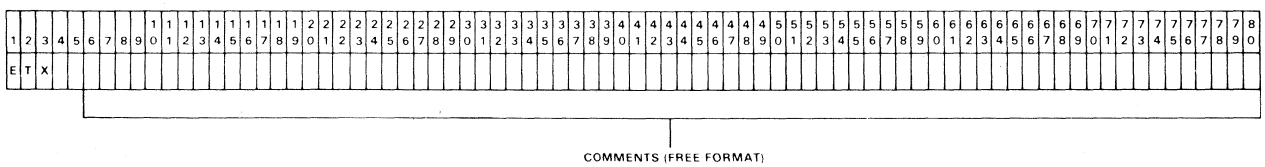
CARD NO. 2—



CARD NO. 3 through NO. 50



CARD NO. 51



Output Active Level entries are determined in accordance with the following table:

OUTPUT ACTIVE LEVEL	
Active high H	**Active low** L

NOTES

1. Polarity programmed once only.
2. Enter (H) for all unused outputs.

Input Variable entries are determined in accordance with the following table:

INPUT VARIABLE		
Im H	$\overline{Im}$ L	Don't care — (dash)

NOTE

Enter (—) for unused inputs of used P-terms.

Output Function entries are determined in accordance with the following table:

OUTPUT FUNCTION	
Product term present in Fp A	Product term not present in Fp • (period)

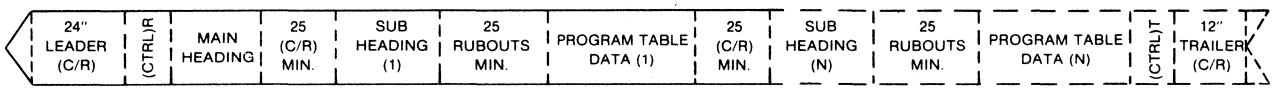
NOTES

1. Entries independent of output polarity.
2. Enter (A) for unused outputs of used P-terms.

TWX TAPE CODING FORMAT

The PLA Program Table can be sent to Signetics in ASCII code format via airmail using any type of 8-level tape (paper, mylar, fanfold, etc.), or via TWX: just dial (910) 339-9283, tell the operator to turn the paper puncher on, and acknowledge. At the end of transmission instruct the operator to send tape to Signetics Order Entry.

A number of Program Tables can be sequentially assembled on a continuous tape as follows, however limit tape length to a roll of 1.75 inch inside diameter, and 4.25 inch outside diameter:



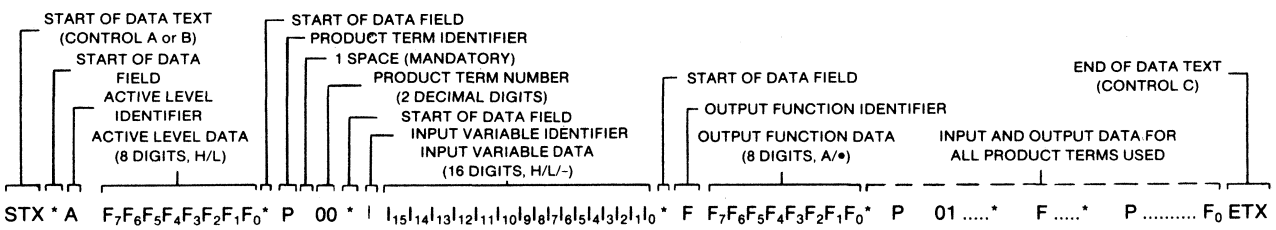
A. The MAIN HEADING at the beginning of tape includes the following information, with each entry preceded by a ($) character, whether used or not:

1. Customer Name _____
2. Customer TWX No. _____
3. Date _____
4. Purchase Order No. _____
5. Number of Program Tables _____
6. Total Number of Parts _____

B. Each SUB HEADING should contain specific information pertinent to each Program Table as follows, with each entry preceded by a ($) character, whether used or not:

1. Signetics Device No. _____
2. Program Table No. _____
3. Revision _____
4. Date _____
5. Customer Symbolized Part No. _____
6. Number of Parts _____

C. Program Table data blocks are initiated with an STX character, and terminated with an ETX character. The body of the data consists of Output Active Level, Product Term, and Output Function information separated by appropriate identifiers in accordance with the following format:



Entries for the 3 Data Fields are determined in accordance with the following Table:

INPUT VARIABLE		
I_m	$\overline{I}_m$	Don't care
H	L	— (dash)

NOTE

Enter (—) for unused inputs of used P-terms.

OUTPUT FUNCTION	
Product term present in Fp	Product term not present in Fp
A	• (period)

NOTES

1. Entries independent of output polarity.
2. Enter (A) for unused outputs of used P-terms.

OUTPUT ACTIVE LEVEL	
Active high	**Active low**
H	L

NOTES

1. Polarity programmed once only.
2. Enter (H) for all unused outputs.

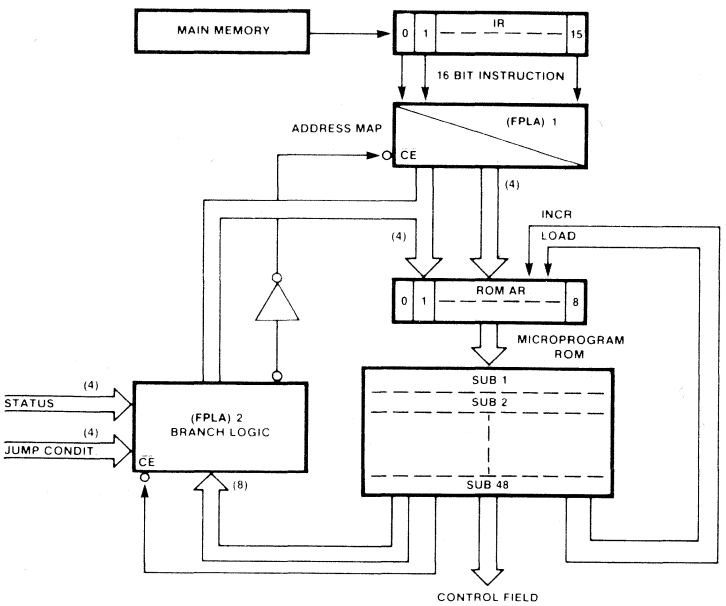
Although the Product Term data are shown entered in sequence, this is not necessary. It is possible to input only one Product Term, if desired. Unused Product Terms require no entry. ETX signalling end of Program Table may occur with less than the maximum number of Product Terms entered.

NOTES

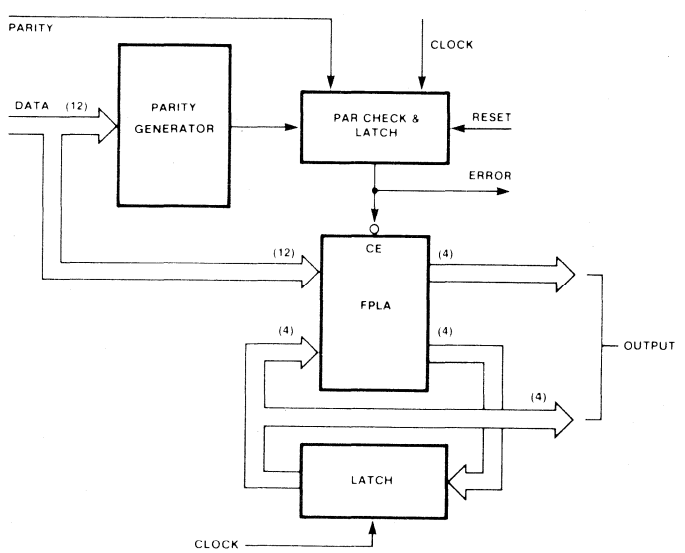
1. Corrections to any entry can be made by backspace and rubout. However, limit consecutive rubouts to less than 25.
2. P-Terms can be re-entered any number of times. The last entry for a particular P-Term will be interpreted as valid data.
3. Any P-Term can be deleted entirely by inserting the character (E) immediately following the P-Term number to be deleted, i.e., *P 25E deletes P-Term 25.
4. To facilitate an orderly Teletype print out, carriage returns, line feeds, spaces, rubouts etc. may be interspersed between data groups, but only preceding an asterisk (*).
5. Comments are allowed between data fields, provided that an asterisk (*) is not used in any Heading or Comment entry.

TYPICAL APPLICATIONS

SUBROUTINE ADDRESS MAP



SEQUENTIAL CONTROLLER



DESCRIPTION

The 82S100 (tri-state outputs) and the 82S101 (open collector outputs) are Bipolar Programmable Logic Arrays, containing 48 product terms (AND terms), and 8 sum terms (OR terms). Each OR term controls an output function which can be programmed either true active-high (F_p), or true active-low (F_p^*). The true state of each output function is activated by any logical combination of 16-input variables, or their complements, up to 48 terms. Both devices are field programmable, which means that custom patterns are immediately available by following the fusing procedure outlined in this data sheet.

The 82S100 and 82S101 are fully TTL compatible, and include chip-enable control for expansion of input variables, and output inhibit. They feature either open collector or tri-state outputs for ease of expansion of product terms and application in bus-organized systems.

Both devices are available in commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S100/101,I or N, and for the military temperature range (-55°C to +125°C) specify S82S100/101,I.

LOGIC FUNCTION

Typical Product Term:
$P_0 = I_0 \bullet I_1 \bullet \overline{I_2} \bullet I_5 \bullet \overline{I_{13}}$

Typical Output Functions:
$F_0 = (\overline{CE}) + (P_0 + P_1 + P_2)$ @ S = Closed
$F_0^* = (\overline{CE}) + (\overline{P_0} \bullet \overline{P_1} \bullet \overline{P_2})$ @ S = Open

NOTE

For each of the 8 outputs, either the function Fp (active-high) or F_p^* (active low) is available, but not both. The required function polarity is programmed via link (S).

FEATURES

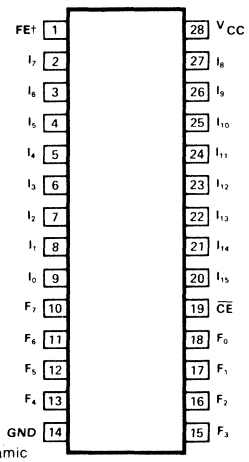
- **Field programmable (Ni-Cr link)**
- **Input variables: 16**
- **Output functions: 8**
- **Product terms: 48**
- **Address access time:**
  - **S82S100/101—80ns Max**
  - **N82S100/101—50ns Max**
- **Power dissipation: 600mW typ**
- **Input loading:**
  - **S82S100/101: -50μA Max**
  - **N82S100/101: -100μA Max**
- **Chip enable input**
- **Output option:**
  - **82S100: Tri-state**
  - **82S101: Open collector**
- **Output disable function:**
  - **Tri-state—Hi-Z**
  - **Open collector—Hi**

APPLICATIONS

- **CRT display systems**
- **Random logic**
- **Code conversion**
- **Peripheral controllers**
- **Function generators**
- **Look-up and decision tables**
- **Microprogramming**
- **Address mapping**
- **Character generators**
- **Sequential controllers**
- **Data security encoders**
- **Fault detectors**
- **Frequency synthesizers**

PIN CONFIGURATION

I,N PACKAGE*

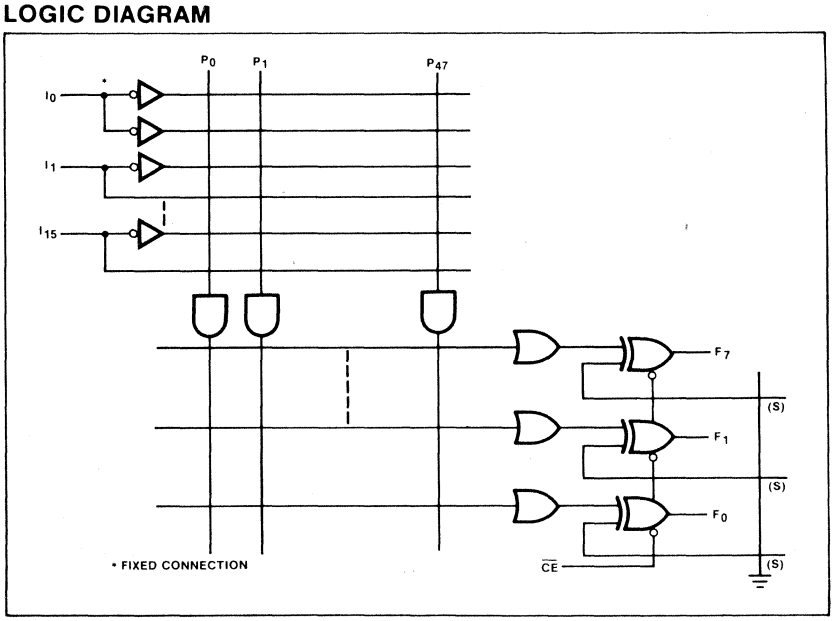


* I = Ceramic
N = Plastic
†Open during normal operation

TRUTH TABLE

MODE	Pn	$\overline{CE}$	Sr ? f(Pn)	Fp	F_p^*
Disabled (82S101)	X	1	X	1	1
Disabled (82S100)				Hi-Z	Hi-Z
Read	1	0	Yes	1	0
	0	0		0	1
	X	0	No	0	1

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			°C
T_A	Operating			
	N82S100/101	0	+75	
	S82S100/101	-55	+125	
T_{STG}	Storage	-65	+150	

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHARACTERISTICS

N82S100/101: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

S82S100/101: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N82S100/101 Min	N82S100/101 Typ[2]	N82S100/101 Max	S82S100/101 Min	S82S100/101 Typ[2]	S82S100/101 Max	UNIT
	Input voltage[3]								V
V_{IH}	High	V_{CC} = Max	2			2			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp[3,4]	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage	V_{CC} = Min							V
V_{OH}	High (82S100)[3,5]	I_{OH} = -2mA	2.4			2.4			
V_{OL}	Low[3,6]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
	Input current								μA
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage[7]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S100)[7]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		-1	-40		-1	-60	
I_{OS}	Short circuit (82S100)[4,8]	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} = Max		120	170		120	180	mA
	Capacitance[7]	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output	V_{OUT} = 2.0V		17			17		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$

N82S100/101: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

S82S100/101: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

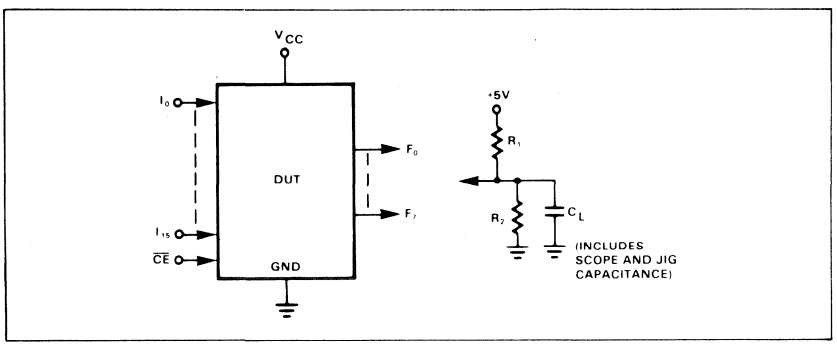
PARAMETER		TO	FROM	N82S100/101 Min	N82S100/101 Typ[2]	N82S100/101 Max	S82S100/101 Min	S82S100/101 Typ[2]	S82S100/101 Max	UNIT
	Access time									ns
T_{IA}	Input	Output	Input		35	50		35	80	
T_{CE}	Chip enable	Output	Chip enable		15	30		15	50	
	Disable time									ns
T_{CD}	Chip disable	Output	Chip enable		15	30		15	50	

NOTES on following page.

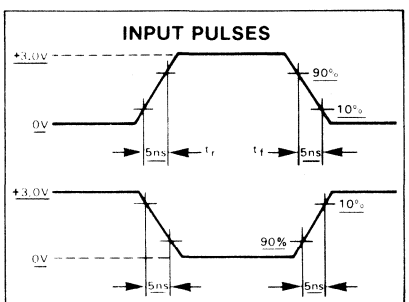
NOTES

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other condition above those indicated in the operation of the device specifications is not implied.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at the time.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
6. Measured with a programmed logic condition for which the output test is at a low logic level. Output sink current is applied thru a resistor to V_{CC}.
7. Measured with V_{IH} applied to $\overline{CE}$.
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

TEST LOAD CIRCUIT

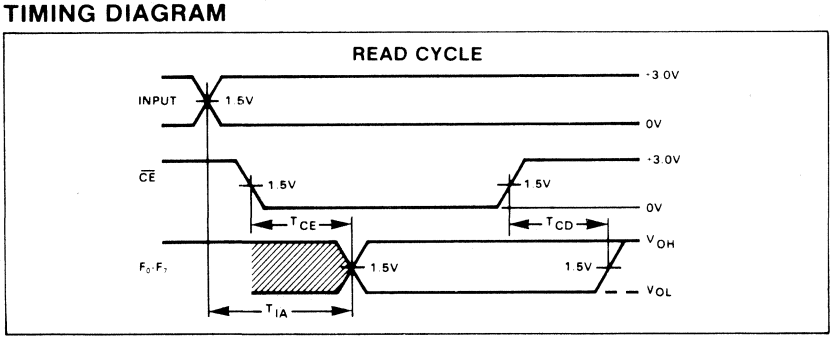


VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the +1.5V level of inputs and outputs.

TIMING DIAGRAM



TIMING DEFINITIONS

T_{CE} Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.

T_{CD} Delay between when Chip Enable becomes high and Data Output is in off state (Hi-Z or high).

T_{IA} Delay between beginning of valid Input (with Chip Enable low) and when Data Output becomes valid.

VIRGIN DEVICE

The 82S100/101 are shipped in an unprogrammed state, characterized by:

1. All internal Ni-Cr links are intact.
2. Each product term (P-term) contains both true and complement values of every input variable I_m (P-terms always logically "false").
3. The "OR" Matrix contains all 48-P-terms.
4. The polarity of each output is set to active high (Fp function).
5. All outputs are at a low logic level.

RECOMMENDED PROGRAMMING PROCEDURE

To program each of 8 Boolean logic functions of 16 true or complement variables, including up to 48 P-terms, follow the Program/Verify procedures for the "AND" matrix, "OR" matrix, and output polarity outlined below. To maximize recovery from programming errors, leave all links in unused device areas intact.

SET-UP

Terminate all device outputs with a 10K resistor to +5V. Set GND (pin 14) to 0V.

Output Polarity

PROGRAM ACTIVE LOW ($F\dot{p}$ FUNCTION)

Program output polarity before programming "AND" matrix and "OR" matrix. Program 1 output at the time. (S) links of unused outputs are not required to be fused.

1. Set FE (pin 1) to V_{FEL}.
2. Set V_{CC} (pin 28) to V_{CCL}.
3. Set $\overline{CE}$ (pin 19), and I_0 through I_{15} to V_{IH}.
4. Apply V_{OPH} to the appropriate output, and remove after a period t_p.
5. Repeat step 4 to program other outputs.

VERIFY OUTPUT POLARITY

1. Set FE (pin 1) to V_{FEL}; set V_{CC} (pin 28) to V_{CCS}.
2. Enable the chip by setting $\overline{CE}$ (pin 19) to V_{IL}.
3. Address a non-existent P-term by applying V_{IH} to all inputs I_0 through I_{15}.
4. Verify output polarity by sensing the logic state of outputs F_0 through F_7. All outputs at a high logic level are programmed active low (F_p function), while all outputs at a low logic level are programmed active high (F_p function).
5. Return V_{CC} to V_{CCP} or V_{CCL}.

"AND" Matrix

PROGRAM INPUT VARIABLE

Program one input at the time and one P-term at the time. All input variable links of unused P-terms are not required to be fused. However, unused input variables must be programmed as Don't Care for all programmed P-terms.

1. Set FE (pin 1) to V_{FEL}, and V_{CC} (pin 28) to V_{CCP}.
2. Disable all device outputs by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.
4. Address the P-term to be programmed (No. 0 through 47) by forcing the corresponding binary code on outputs F_0 through F_5 with F_0 as LSB. Use standard TTL logic levels V_{OHF} and V_{OLF}.

5a. If the P-term contains neither I_0 nor $\overline{I_0}$ (input is a Don't Care), fuse both I_0 and $\overline{I_0}$ links by executing both steps 5b and 5c, before continuing with step 7.

5b. If the P-term contains I_0, set to fuse the $\overline{I_0}$ link by lowering the input voltage at I_0 from V_{IX} to V_{IH}. Execute step 6.

5c. If the P-term contains $\overline{I_0}$, set to fuse the I_0 link by lowering the input voltage at I_0 from V_{IX} to V_{IL}. Execute step 6.

6a. After t_D delay, raise FE (pin 1) from V_{FEL} to V_{FEH}.

6b. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IX} for a period t_p.

6c. After t_D delay, return FE input to V_{FEL}.

7. Disable programmed input by returning I_0 to V_{IX}.
8. Repeat steps 5 through 7 for all other input variables.
9. Repeat steps 4 through 8 for all other P-terms.
10. Remove V_{IX} from all input variables.

VERIFY INPUT VARIABLE

1. Set FE (pin 1) to V_{FEL}; set V_{CC} (pin 28) to V_{CCP}.
2. Enable F_7 output by setting $\overline{CE}$ to V_{IX}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.
4. Address the P-term to be verified (No. 0 through 47) by forcing the corresponding binary code on outputs F_0 through F_5.
5. Interrogate input variable I_0 as follows:
   A. Lower the input voltage at I_0 from V_{IX} to V_{IH}, and sense the logic state of output F_7.
   B. Lower the input voltage at I_0 from V_{IH} to V_{IL}, and sense the logic state output F_7.

The state of I_0 contained in the P-term is determined in accordance with the following truth table:

I_0	F_7	INPUT VARIABLE STATE CONTAINED IN P-TERM
0 1	1 0	$\overline{I_0}$
0 1	0 1	I_0
0 1	1 1	Don't Care
0 1	0 0	(I_0), $(\overline{I_0})$

Note that 2 tests are required to uniquely determine the state of the input variable contained in the P-term.

6. Disable verified input by returning I_0 to V_{IX}.
7. Repeat steps 5 and 6 for all other input variables.
8. Repeat steps 4 through 7 for all other P-terms.
9. Remove V_{IX} from all input variables.

"OR" MATRIX

PROGRAM PRODUCT TERM

Program one output at the time for one P-term at the time. All P_n links in the "OR" matrix corresponding to unused outputs and unused P-terms are not required to be fused.

1. Set FE (pin 1) to V_{FEL}.
2. Disable the chip by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. After t_D delay, set V_{CC} (pin 28) to V_{CCS}, and inputs I_6 through I_{15} to V_{IH}, V_{IL}, or V_{IX}.
4. Address the P-term to be programmed (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5, with I_0 as LSB.

5a. If the P-term is contained in output function F_0 ($F_0 = 1$ or $F_0^* = 0$), got to step 6, (fusing cycle not required).

5b. If the P-term is **not** contained in output function F_0 ($F_0 = 0$ or $F_0^* = 1$), set to fuse the P_n link by forcing output F_0 to V_{OPF}.

6a. After t_D delay, raise FE (pin 1) from V_{FEL} to V_{FEH}.

6b. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IX} for a period t_p.

6c. After t_D delay, return FE input to V_{FEL}.

6d. After t_D delay, remove V_{OPF} from output F_0.

7. Repeat steps 5 and 6 for all other output functions.
8. Repeat steps 4 through 7 for all other P-terms.
9. Remove V_{CCS} from V_{CC}.

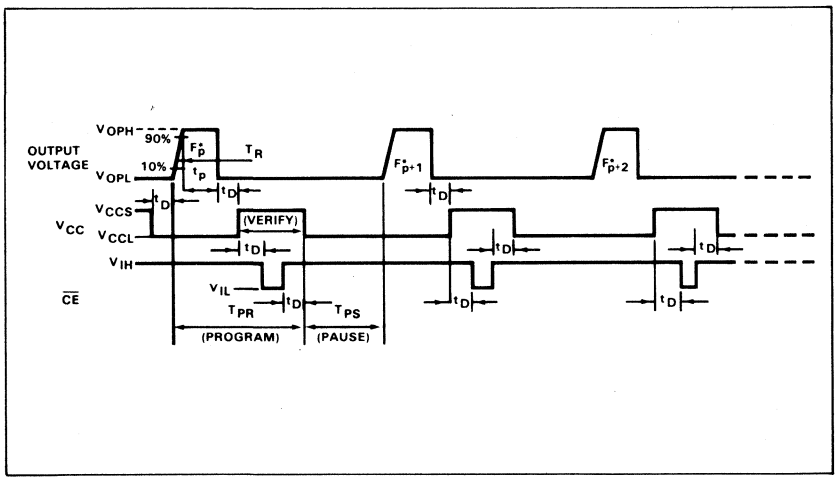
VERIFY PRODUCT TERM

1. Set FE (pin 1) to V_{FEL}.
2. Disable the chip by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. After t_D delay, set V_{CC} (pin 28) to V_{CCS}, and inputs I_0 through I_{15} to V_{IH}, V_{IL}, or V_{IX}.
4. Address the P-term to be verified (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5.
5. After t_D delay, enable the chip by setting $\overline{CE}$ (pin 19) to V_{IL}.
6. To determine the status of the P_n link in the "OR" matrix for each output function F_p or F_p^*, sense the state of outputs F_0 through F_7. The status of the link is given by the following truth table:

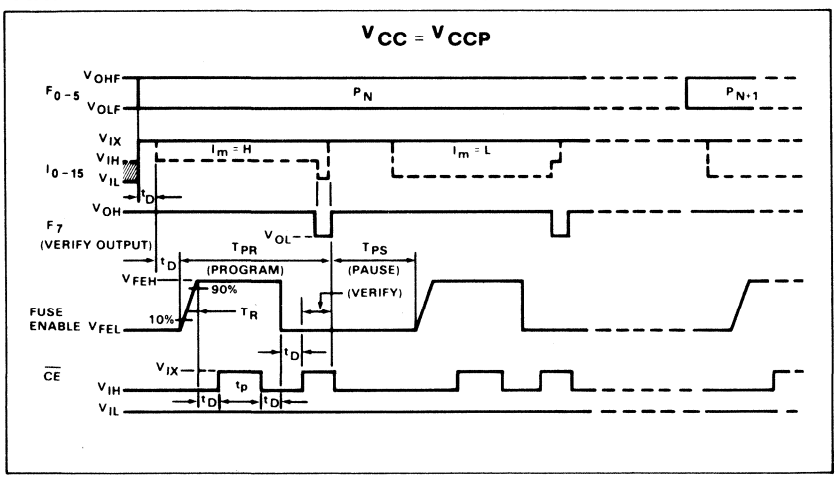
OUTPUT		P-TERM LINK
Active High (Fp)	Active Low (F_p^*)	
0 1	1 0	**Fused** **Present**

7. Repeat steps 4 through 6 for all other P-terms.
8. Remove V_{CCS} from V_{CC}.

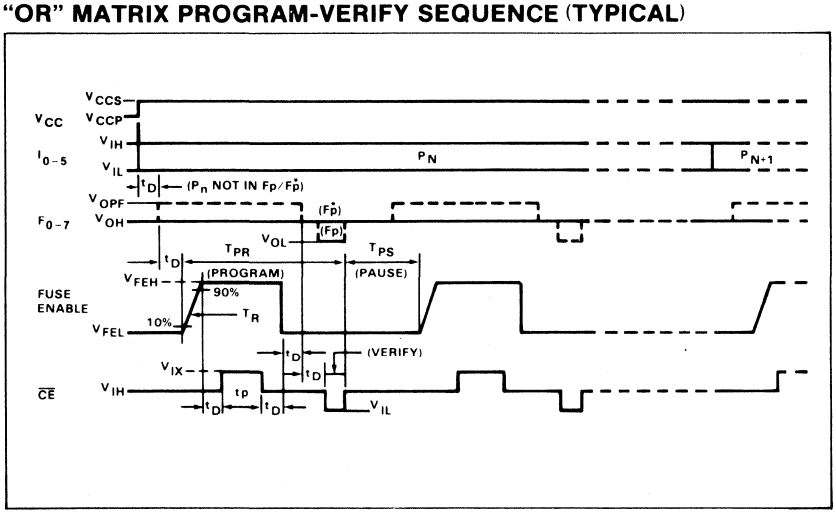
OUTPUT POLARITY PROGRAM-VERIFY SEQUENCE (TYPICAL)



"AND" MATRIX PROGRAM-VERIFY SEQUENCE (TYPICAL)



"OR" MATRIX PROGRAM-VERIFY SEQUENCE (TYPICAL)



PROGRAMMING SYSTEM SPECIFICATIONS[1] (T_A = +25°C)

	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
V_{CCS}	V_{CC} supply (program/verify "OR", verify output polarity)[2]	I_{CCS} = 550mA, min, Transient or steady state	8.25	8.5	8.75	V
V_{CCL}	V_{CC} supply (program output polarity)		0	0.4	0.8	V
I_{CCS}	I_{CC} limit (program "OR")	V_{CCS} = +8.5 ± .25V	550		1,000	mA
	Output voltage					V
V_{OPH}	Program output polarity[3]	I_{OPH} = 300 ± 25mA	16.0	17.0	18.0	
V_{OPL}	Idle		0	0.4	0.8	
I_{OPH}	Output current limit (Program output polarity)	V_{OPH} = +17 ± 1V	275	300	325	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					µA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = 0V			-500	
	Forced output voltage					V
V_{OHF}	High		2.4		5.5	
V_{OLF}	Low		0	0.4	0.8	
	Output current					
I_{OHF}	High	V_{OHF} = +5.5V			100	µA
I_{OLF}	Low	V_{OLF} = 0V			-1	mA
V_{IX}	$\overline{CE}$ program enable level		9.5	10	10.5	V
I_{IX1}	Input variables current	V_{IX} = +10V			2.5	mA
I_{IX2}	$\overline{CE}$ input current	V_{IX} = +10V			5.0	mA
V_{FEH}	FE supply (program)[3]	I_{FEH} = 300 ± 25mA, Transient or steady state	16.0	17.0	18.0	V
V_{FEL}	FE supply (idle)	I_{FEL} = -1mA, max	1.25	1.5	1.75	V
I_{FEH}	FE supply current limit	V_{FEH} = +17 ± 1V	275	300	325	mA
V_{CCP}	Vcc supply (program/verify "AND")	I_{CCP} = 550mA, min, Transient or steady state	4.75	5.0	5.25	V
I_{CCP}	I_{CC} limit (program "AND")	V_{CCP} = +5.0 ± .25V	550		1,000	mA
V_{OPF}	Forced output (program)		9.5	10	10.5	V
I_{OPF}	Output current (program)				10	mA
T_R	Output pulse rise time		10		50	µs
t_P	$\overline{CE}$ programming pulse width		0.3	0.4	0.5	ms[5]
t_D	Pulse sequence delay		10			µs
T_{PR}	Programming time			0.6		ms
$\frac{T_{PR}}{T_{PR} + T_{PS}}$	Programming duty cycle				50	%
F_L	Fusing attempts per link				2	cycle
V_S	Verify threshold[4]		1.4	1.5	1.6	V

NOTES

1. These are specifications which a Programming System must satisy in order to be qualified by Signetics.
2. Bypass V_{CC} to GND with a 0.01µf capacitor to reduce voltage spikes.
3. Care should be taken to ensure that the voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
4. V_S is the sensing threshold of the FPLA output voltage for a programmed link. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
5. These are new limits resulting from device improvements, and which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment.

16X48X8 FPLA PROGRAM TABLE

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX)[1] _____

CUSTOMER SYMBOLIZED PART # _____

DATE RECEIVED _____

COMMENTS _____

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____

REV _____ DATE _____

PROGRAM TABLE ENTRIES						
INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
Im	$\overline{Im}$	Don't Care	Prod. Term Present in FP	Prod. Term Not Present in FP	Active High	Active Low
H	L	— (dash)	A	• (period)	H	L
NOTE Enter "—" for unused inputs of used P-terms			NOTES 1. Entries independent of output polarity 2. Enter "A" for unused outputs of used P-terms		NOTES 1. Polarity programmed once only 2. Enter "H" for all unused outputs	

	PRODUCT TERM[1]															
	INPUT VARIABLE[1]															
NO	1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0
0																
1																
2																
3																
4																
5																
6																
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47																

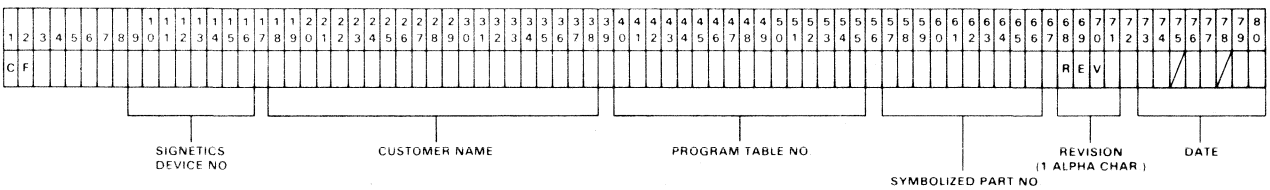
ACTIVE LEVEL[1]							
OUTPUT FUNCTION[1]							
7	6	5	4	3	2	1	0

(1) Input and Output fields of unused P-terms can be left blank. Unused inputs and outputs are FPLA terminals left floating.

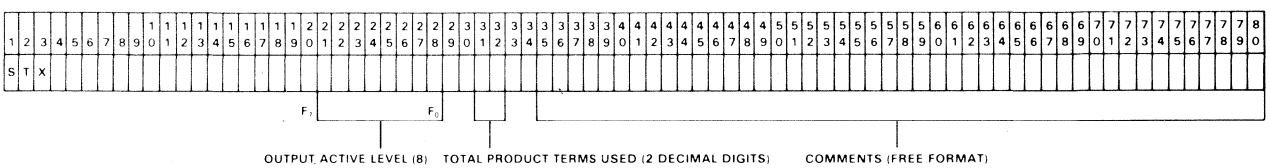
PUNCHED CARD CODING FORMAT

The FPLA Program Table can be supplied directly to Signetics in punched card form, using standard 80-column IBM cards. For each FPLA Program Table, the customer should prepare in input card deck in accordance with the following format. Product Term cards 3 through 50 can be in any order. Not all 48 Product Terms need to be present. Unused Product Terms require no entry cards, and will be skipped during the actual programming sequence:

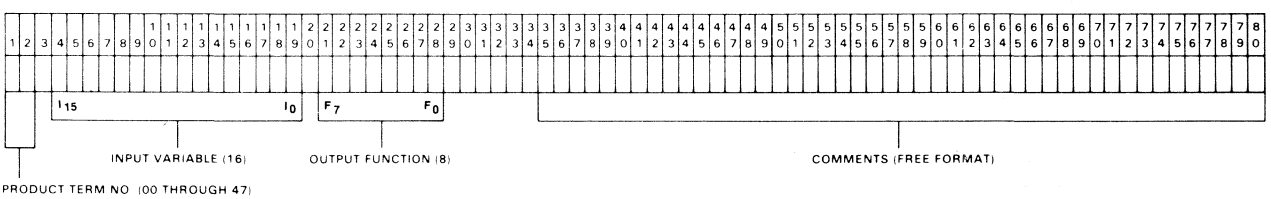
CARD NO.1—Free format within designated fields.



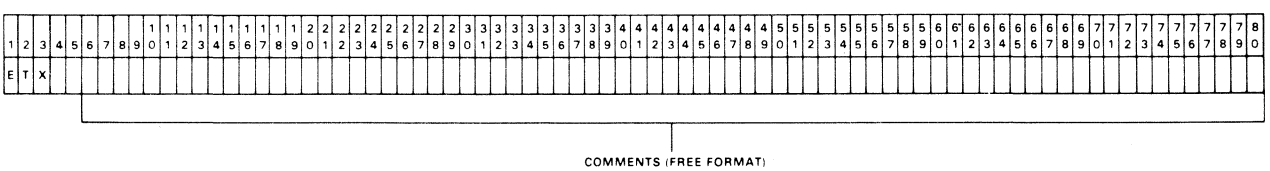
CARD NO. 2—



CARD NO. 3 through NO. 50



CARD NO. 51



Output Active Level entries are determined in accordance with the following table:

OUTPUT ACTIVE LEVEL	
Active high H	**Active low** L

NOTES

1. Polarity programmed once only.
2. Enter (H) for all unused outputs.

Input Variable entries are determined in accordance with the following table:

INPUT VARIABLE		
Im H	$\overline{\text{Im}}$ L	Don't care — (dash)

NOTE

Enter (—) for unused inputs of used P-terms.

Output Function entries are determined in accordance with the following table:

OUTPUT FUNCTION	
Product term present in F_P A	Product term *not* present in F_P • (period)

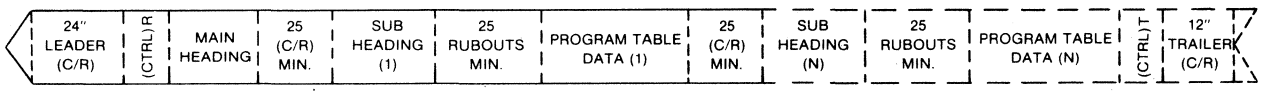
NOTES

1. Entries independent of output polarity.
2. Enter (A) for unused outputs of used P-terms.

TWX TAPE CODING FORMAT

The FPLA Program Table can be sent to Signetics in ASCII code format via airmail using any type of 8-level tape (paper, mylar, fanfold, etc.), or via TWX: just dial (910) 339-9283, tell the operator to turn the paper puncher on, and acknowledge. At the end of transmission instruct the operator to send tape to Signetics Order Entry.

A number of Program Tables can be sequentially assembled on a continuous tape as follows, however limit tape length to a roll of 1.75 inch inside diameter, and 4.25 inch outside diameter:



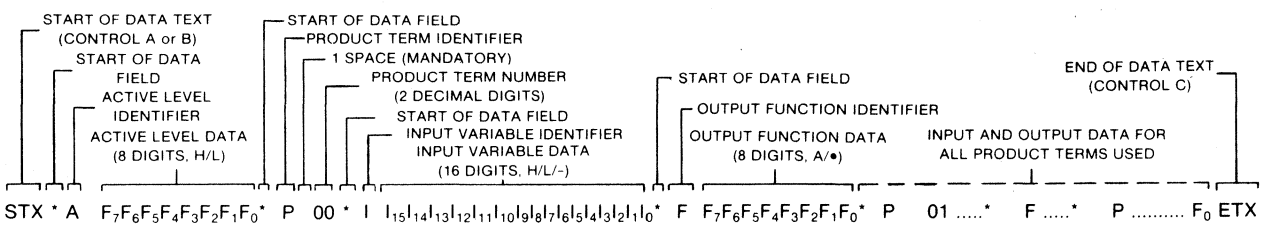
A. The MAIN HEADING at the beginning of tape includes the following information, with each entry preceded by a ($) character, whether used or not:

1. Customer Name _____
2. Customer TWX No. _____
3. Date _____
4. Purchase Order No. _____
5. Number of Program Tables _____
6. Total Number of Parts _____

B. Each SUB HEADING should contain specific information pertinent to each Program Table as follows, with each entry preceded by a ($) character, whether used or not:

1. Signetics Device No. _____
2. Program Table No. _____
3. Revision _____
4. Date _____
5. Customer Symbolized Part No. _____
6. Number of Parts _____

C. Program Table data blocks are initiated with an STX character, and terminated with an ETX character. The body of the data consists of Output Active Level, Product Term, and Output Function information separated by appropriate identifiers in accordance with the following format:



Entries for the 3 Data Fields are determined in accordance with the following Table:

INPUT VARIABLE		
I_m H	$\overline{I_m}$ L	Don't care — (dash)

NOTE

Enter (—) for unused inputs of used P-terms.

OUTPUT FUNCTION	
Product term present in Fp A	Product term not present in Fp • (period)

NOTES

1. Entries independent of output polarity.
2. Enter (A) for unused outputs of used P-terms.

OUTPUT ACTIVE LEVEL	
Active high H	**Active low** L

NOTES

1. Polarity programmed once only.
2. Enter (H) for all unused outputs.

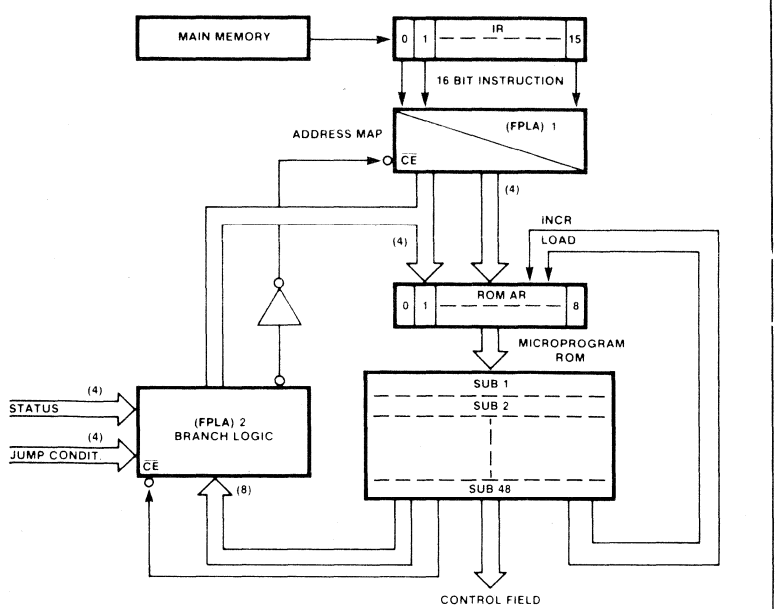
Although the Product Term data are shown entered in sequence, this is not necessary. It is possible to input only one Product Term, if desired. Unused Product Terms require no entry. ETX signalling end of Program Table may occur with less than the maximum number of Product Terms entered.

NOTES

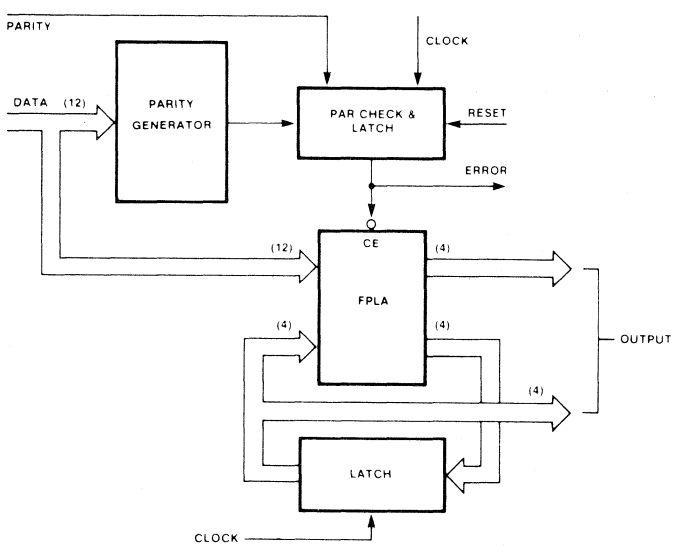
1. Corrections to any entry can be made by backspace and rubout. However, limit consecutive rubouts to less than 25.
2. P-Terms can be re-entered any number of times. The last entry for a particular P-Term will be interpreted as valid data.
3. Any P-Term can be deleted entirely by inserting the character (E) immediately following the P-Term number to be deleted, i.e., *P 25E deletes P-Term 25.
4. To facilitate an orderly Teletype print out, carriage returns, line feeds, spaces, rubouts etc. may be interspersed between data groups, but only preceding an asterisk (*).
5. Comments are allowed between data fields, provided that an asterisk (*) is not used in any Heading or Comment entry.

TYPICAL APPLICATIONS

SUBROUTINE ADDRESS MAP



SEQUENTIAL CONTROLLER



82S102-I,N • 82S103-I,N

DESCRIPTION

The 82S102 and 82S103 are Bipolar programmable AND/NAND gate arrays, containing 9 gates sharing 16 common inputs. On-chip input buffers enable the user to individually program for each gate either the True (I_m), Complement ($\overline{I_m}$), or Don't Care (X) logic state of each input. In addition, the polarity of each gate output is individually programmable to implement either AND or NAND logic functions.

Alternately, if desired, OR/NOR logic functions can also be realized by programming for each gate the complement of its input variables, and output (DeMorgan theorem).

Both devices are field-programmable, which means that custom patterns are immediately available by following the fusing procedure outlined in this data sheet.

The 82S102 and 82S103 include chip-enable control for output strobing and inhibit. They feature either open collector or tri-state outputs for ease of expansion of input variables and application in bus-organized systems.

Both devices are available in the commercial and military temperature ranges. For the commercial range (0°C to +75°C) specify N82S102/103, I or N, and for the military range (−55°C to +125°C) specify S82S102/103, I.

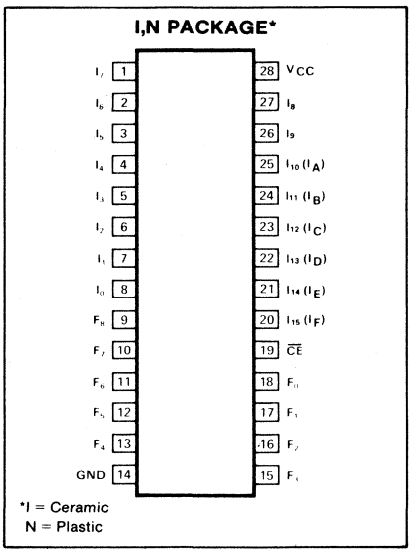
FEATURES

- **Field programmable (Ni-Cr link)**
- **16 input variables**
- **9 output functions**
- **Chip enable input**
- **I/O propagation delay:**
  N82S102/103: 35ns max
  S82S102/103: 50ns max
- **Power dissipation: 600mW typ**
- **Input loading:**
  N82S102/103: −100μA max
  S82S102/103: −150μA max
- **Output options:**
  82S102: Open collector
  82S103: Tri-state
- **Output disable function:**
  82S102: Hi
  82S103: Hi-Z
- **Fully TTL compatible**

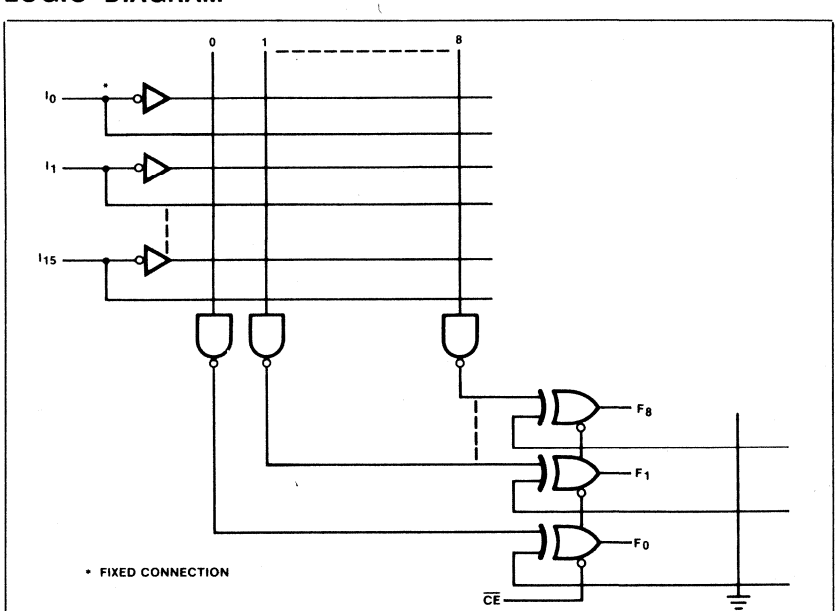
APPLICATIONS

- **Random logic**
- **Address decoders**
- **Code detectors**
- **Peripheral selectors**
- **Fault monitors**
- **Machine state decoders**

PIN CONFIGURATION



LOGIC DIAGRAM

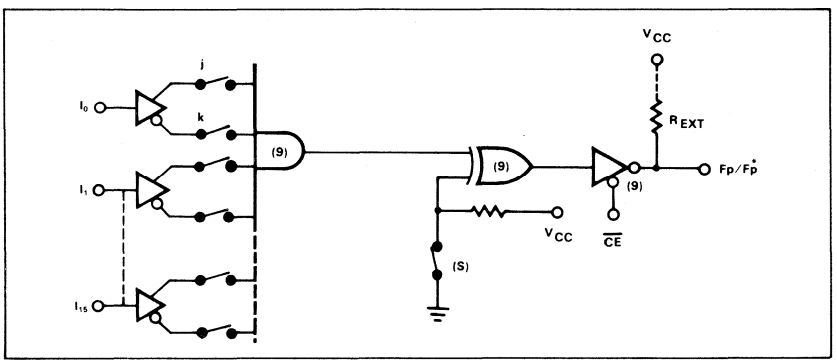


For each of the 9 outputs, either the function Fp (active high) or Fp (active low) is available, but not both. The required function polarity is user programmable via fuse (S).

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S102)	+5.5	
V_O	Off-state (82S103)	+5.5	
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
	Temperature range		°C
T_A	Operating		
	N82S102/103	0 to +75	
	S82S102/103	-55 to +125	
T_{STG}	Storage	-65 to +150	

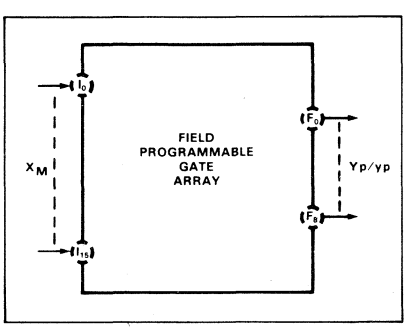
EQUIVALENT LOGIC PATH



The Field Programmable Gate Array consists of 9 gates with individually programmable inputs and outputs.

The inputs to each gate can be programmed either True (I_m), Complement ($\overline{I_m}$), or Don't Care via corresponding links (j) and (k). The outputs of each gate can be programmed active-high (F_p) or active-low (F_p^*) via corresponding links (S). Thus, each gate provides either of 2 output logic functions in terms of *external* input logic variables X_m as defined below (positive logic):

At S = Open:
$F_p = \overline{CE} + (X_0 \bullet X_1 \bullet X_2 \bullet \ldots . X_m) = Y_p$
At S = Closed:
$F_p^* = \overline{CE} + (\overline{X}_0 + \overline{X}_1 + \overline{X}_2 + \ldots . X_m) = y_p$
$m = 0, 1, 2, \ldots . 15$

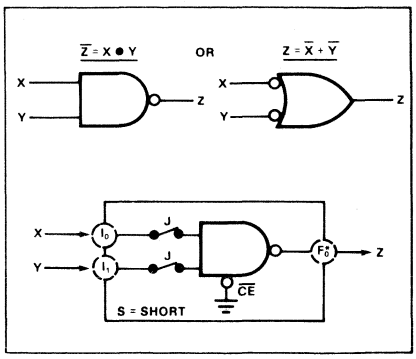


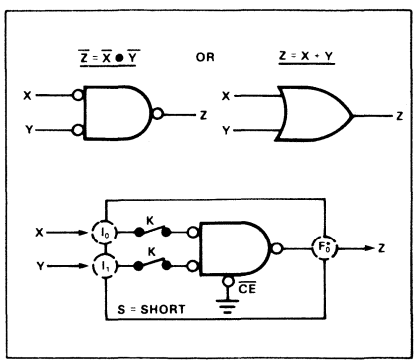
$p = 0, 1, 2, \ldots . 8$
and where $X_m = I_m, \overline{I_m}$, Don't Care, as assigned by programming polarity of inputs I_0–I_{15}.

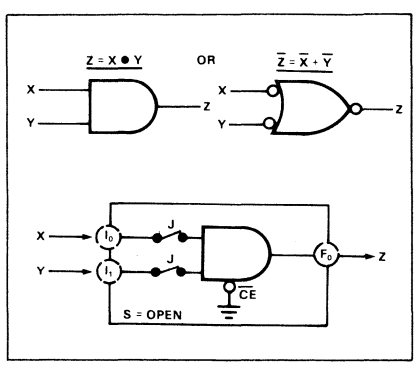
When $\overline{CE}$ = low, all gates are enabled, and $F_p^* = \overline{F}_p$ giving $y_p = \overline{Y}_p$.

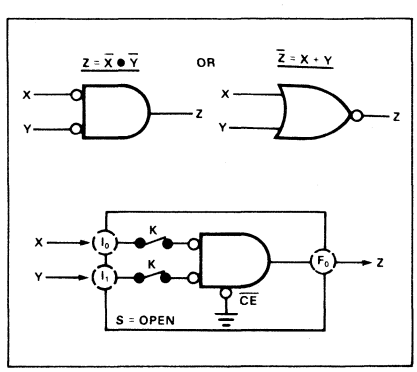
PROGRAMMABLE LOGIC FUNCTIONS

All internal links of virgin FPGAs are intact. Therefore, as shown in the Equivalent Logic Path, all symbolic switches are initially closed. Selective programming (opening) of links (J), (K), and (S) enables the user to assign input and output polarities to each gate for implementing NAND, NOR, AND, OR logic functions without changing the routing of input and output wires. This is shown in the following diagrams for a typical gate in terms of 2 input variables, which can be readily extended up to 16.









DC ELECTRICAL CHARACTERISTICS

N82S102/103: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S102/103: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER[1]		TEST CONDITIONS	N82S102/103			S82S102/103			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low[1]	V_{CC} = Min			0.85			0.8	
V_{IH}	High[1]	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp[1,3]	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[1,4]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
V_{OH}	High (82S103)[1,5]	I_{OH} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage (82S102)[6]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S103)[6]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		-1	-40		-1	-60	
I_{OS}	Short circuit (82S103)[3,7]	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		120	170		120	180	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output[6]	V_{OUT} = 2.0V		15			15		

AC ELECTRICAL CHARACTERISTICS

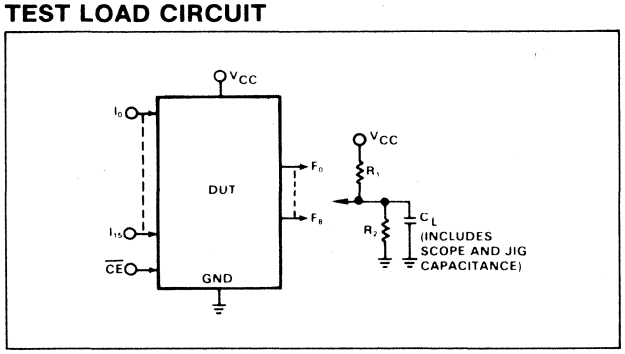
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S102/103: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S102/103: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N82S102/103			S82S103/103			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time									ns
T_{IA}	Input	Output	Input		20	35		20	55	
T_{CE}	Chip enable	Output	Chip enable		15	30		15	45	
	Disable time									ns
T_{CD}	Chip disable	Output	Chip enable		15	30		15	45	

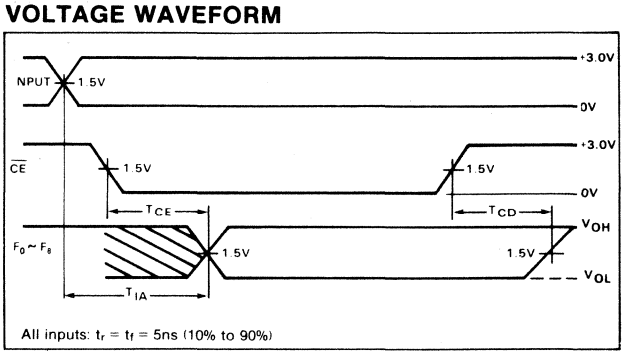
NOTES

1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Test each output one at a time.
4. Measured with a programmed logic condition for which the output under test is at a low logic level. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high at the output.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

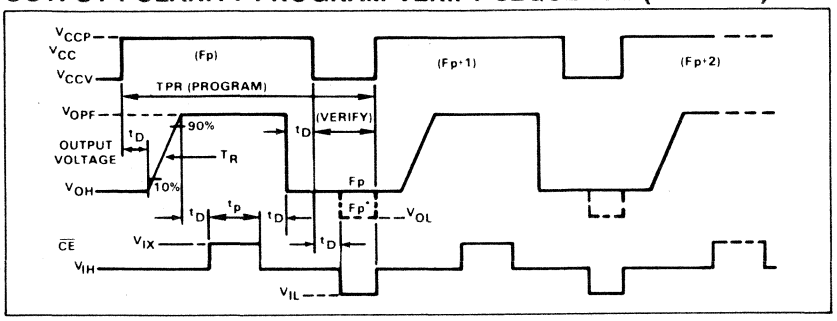
TEST LOAD CIRCUIT



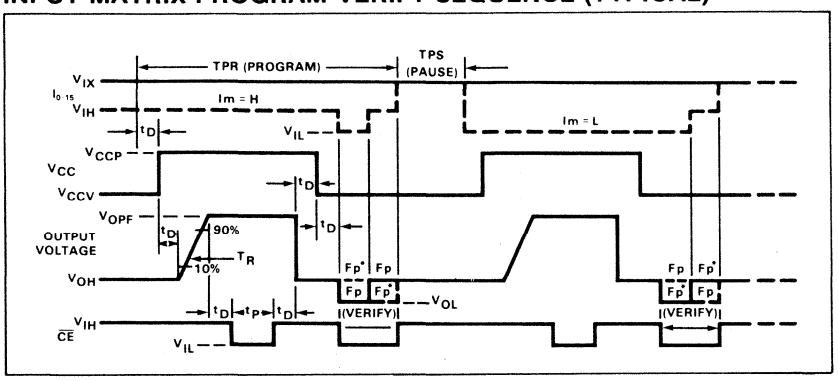
VOLTAGE WAVEFORM



OUTPUT POLARITY PROGRAM-VERIFY SEQUENCE (TYPICAL)



INPUT MATRIX PROGRAM-VERIFY SEQUENCE (TYPICAL)



VIRGIN DEVICE

The 82S102/103 are shipped in an unprogrammed state, characterized by:

1. All internal Ni-Cr links are intact.
2. Each gate contains both true and complement values of every input variable I_m (logic Null state).
3. The polarity of each output is set to active low (F_p function).
4. All outputs are at a high logic level.

RECOMMENDED PROGRAMMING PROCEDURE

To program each of 9 Boolean logic functions of 16 True, Complement, or Don't Care input variables follow the program/verify procedures for the Input Matrix and Output Polarity outlined below. To maximize recovery from programming errors, leave all links of unused gates intact.

SET-UP

Terminate all device outputs with a 10KΩ resistor to +5V.

Output Polarity

PROGRAM ACTIVE HIGH (Fp FUNCTION)

Program output polarity before programming inputs (for convenience). Program one output at a time. (S) links of unused outputs are not required to be fused.

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to V_{CCV}.
2. Disable all device outputs by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

A. Raise V_{CC} (pin 28) from V_{CCV} to V_{CCP}.
B. After t_D delay, force output to be programmed to V_{OPF}.
C. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IX} for a period t_p.
D. After t_D delay, remove V_{OPF} voltage source from output being programmed.
E. After t_D delay, return V_{CC} (pin 28) to V_{CCV}, and verify.
F. Repeat steps A through E for any other output.

VERIFY OUTPUT POLARITY

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to V_{CCV}.
2. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

A. After t_D delay, set the $\overline{CE}$ input to V_{IL}.
B. Verify output polarity by sensing the logic state of outputs F_0 through F_8. All outputs at a low logic level are programmed active low (F_p^* function), while all outputs at a high logic level are programmed active high (F_p function).

Input Matrix

PROGRAM INPUT VARIABLE

Program one input at a time for one gate at a time. Input variable links of unused gates are not required to be fused. However, unused input variables must be programmed at Don't Care for all used gates.

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to V_{CCV}.
2. Disable all device outputs by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

A-1. If a gate contains nether I_0 nor $\overline{I_0}$ (input is a Don't Care), fuse both j and k links by executing both steps A-2 and A-3, before continuing with step C.
A-2. If a gate contains I_0, set to fuse the k link by lowering the input voltage at I_0 from V_{IX} to V_{IH}. Execute step B.
A-3. If a gate contains $\overline{I_0}$, set to fuse the j link by lowering the input voltage at I_0 from V_{IX} to V_{IL}. Execute step B.
B-1. After t_D delay, raise V_{CC} from V_{CCV} to V_{CCP}.
B-2. After t_D delay, force output of gate to be programmed to V_{OPF}.
B-3. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IL} for a period t_p.
B-4. After t_D delay, remove V_{OPF} voltage source from output of gate being programmed.
B-5. After t_D delay, return V_{CC} (pin 28) to V_{CCV}, and verify.
C. Disable programmed input by returning I_0 to V_{IX}.
D. Repeat steps A through C for all other input variables.
E. Repeat steps A through D for all other gates to be programmed.
F. Remove V_{IX} from all input variables.

VERIFY INPUT VARIABLE

Unambiguous verification of the logic state programmed for the inputs of each gate requires prior knowledge of its programmed output polarity. Therefore, the output polarity verify procedure must precede input variable verify.

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to V_{CCV}.
2. Enable all outputs by setting $\overline{CE}$ (pin 19) to V_{IL}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

A. Interrogate input variable I_0 as follows: Lower the input voltage to I_0 from V_{IX} to V_{IL}, and sense the logic state of outputs F_{0-8}.

Raise the input voltage to I_0 from V_{IL} to V_{IH} and sense the logic state of outputs F_{0-8}.

The state of I_0 contained in each gate is determined in accordance with the given truth table. Note that 2 tests are required to uniquely determine the state of the input variable contained in each gate.

B. Disable verified input by returning I_0 to V_{IX}.

C. Repeat steps A and B for all other input variables.

D. Remove V_{IX} from all input variables.

TRUTH TABLE FOR INPUT VERIFICATION

I_0	Fp	$F\dot{p}$	INPUT VARIABLE STATE	LINK FUSED
0	1	0	$\overline{I_0}$	j
1	0	1		
0	0	1	I_0	k
1	1	0		
0	1	0	Don't care	Both
1	1	0		
0	0	1	(I_0), $(\overline{I_0})$	Neither
1	0	1		

PROGRAMMING SYSTEMS SPECIFICATIONS[1] $T_A = 25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	V_{CC} supply					V
V_{CCP}	Program[2]	I_{CCP} = 350 ± 50mA, Transient or steady state	8.5	8.75	9.0	
V_{CCV}	Verify		4.75	5.0	5.25	
I_{CCP}	I_{CC} limit (program)	V_{CCP} = +8.75 ± .25V, Transient or steady state	400	450	500	mA
V_{OPF}	Forced output voltage[3] (program)	I_{OP} = 150 ± 25mA, Transient or steady state	16.0	17.0	18.0	V
I_{OPF}	Output current limit (program)	V_{OP} = +17 ± 1V, Transient or steady state	125	150	175	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = 0V			-500	
V_{IX}	$\overline{CE}$ program enable level		9.5	10	10.5	V
I_{IX1}	Input variables current	V_{IX} = +10V			5.0	mA
I_{IX2}	$\overline{CE}$ input current	V_{IX} = +10V			10.0	mA
T_R	Output pulse rise time		10		50	μs
t_P	$\overline{CE}$ programming pulse width		0.3	0.4	0.5	ms
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time			0.6		ms
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle				100	%
F_L	Fusing attempts per link				2	cycle
V_S	Verify threshold[4]		1.4	1.5	1.6	V

NOTES

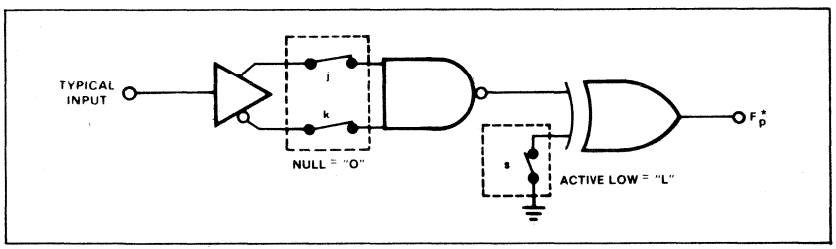
1. These are specifications which a Programming System must satisfy in order to be qualified by Signetics.
2. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
3. Care should be taken to ensure that the voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
4. V_S is the sensing threshold of a gate output voltage for a programmed link. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

PROGRAMMING

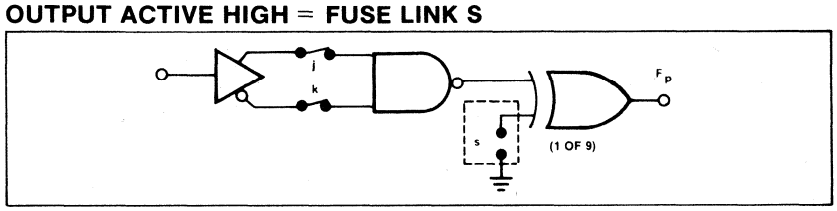
In a virgin device all Ni-Cr links are intact. The initial programmed state of each gate is shown in the Typical Gate illustration.

To program inputs and outputs of each gate for implementing the desired logic function, fuse Ni-Cr links as indicated in the fuse link diagrams.

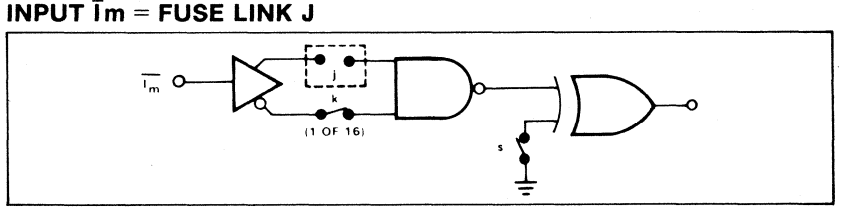
TYPICAL GATE



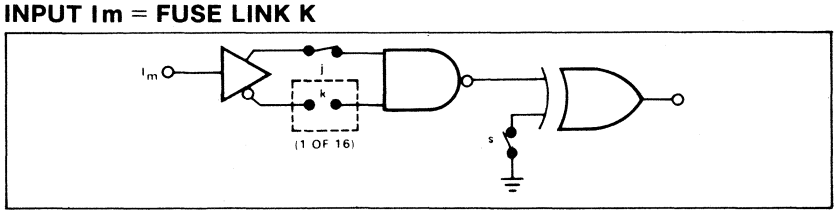
OUTPUT ACTIVE HIGH = FUSE LINK S



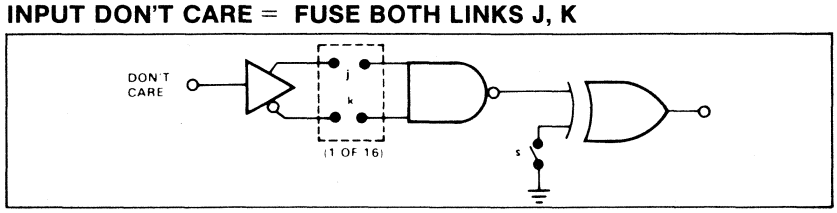
INPUT $\bar{I}m$ = FUSE LINK J



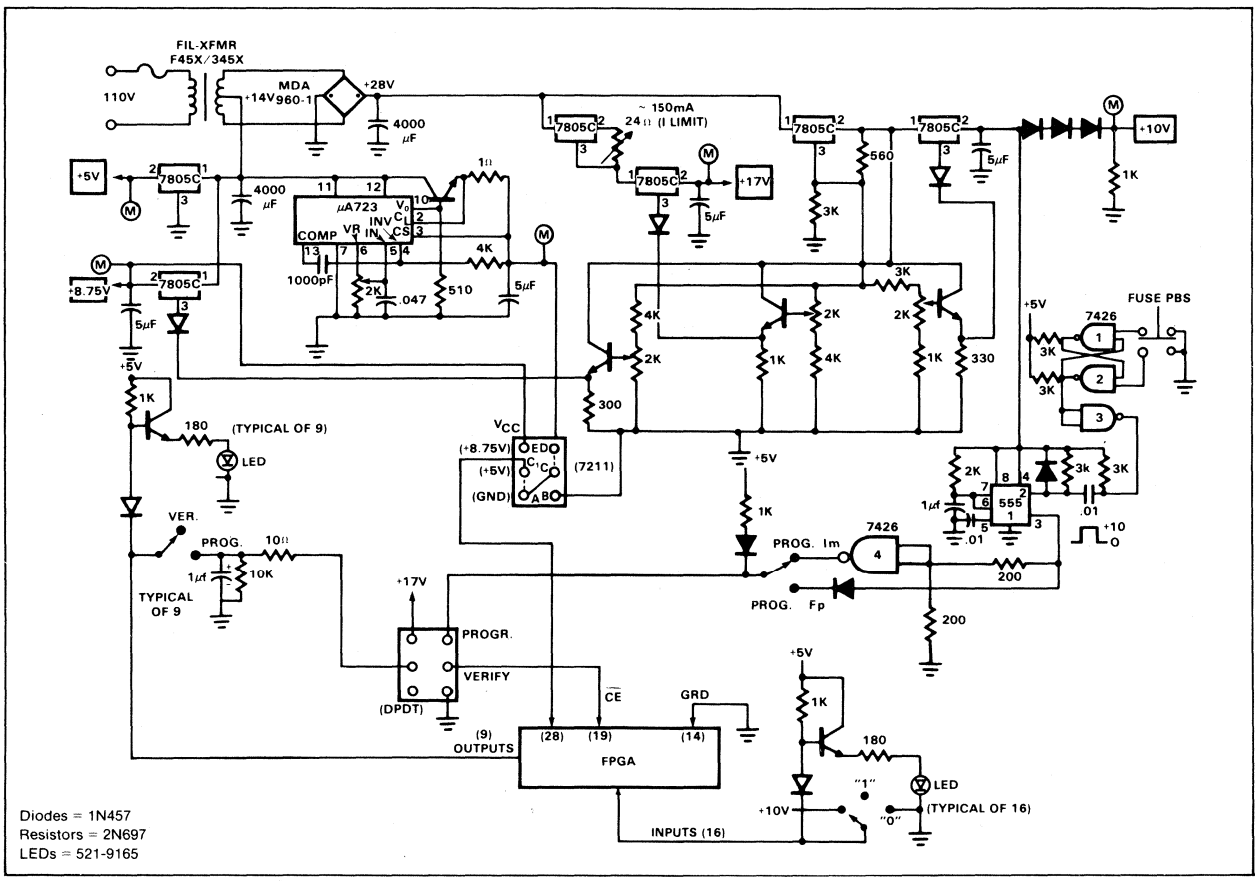
INPUT Im = FUSE LINK K



INPUT DON'T CARE = FUSE BOTH LINKS J, K



FPGA MANUAL FUSER



16X9 FPGA PROGRAM TABLE

CUSTOMER NAME _____	*THIS PORTION TO BE COMPLETED BY SIGNETICS*
PURCHASE ORDER # _____	*CF (XXXX)* _____
SIGNETICS DEVICE # _____	*CUSTOMER SYMBOLIZED PART #* _____
TOTAL NUMBER OF PARTS _____	*DATE RECEIVED* _____
PROGRAM TABLE # _____	*COMMENTS* _____

F_0 = _____

F_1 = _____

F_2 = _____

F_3 = _____

F_4 = _____

F_5 = _____

F_6 = _____

F_7 = _____

F_8 = _____

OUTPUT POLARITY		INPUT VARIABLE															
		I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_A	I_B	I_C	I_D	I_E	I_F
F_0	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
F_1	16	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
F_2	32	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
F_3	48	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
F_4	64	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
F_5	80	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
F_6	96	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
F_7	112	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
F_8	128	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
Active-high = H Active-low = L		I_m = H $\overline{I_m}$ = L Don't Care = —															

The number in each cell in the table denotes its address for programmers with a decimal address display.

DESCRIPTION

The 82S104 (open collector outputs) and the 82S105 (tri-state outputs) are bipolar, programmable state machines of the Mealy type. They contain logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip State and Output registers. These consist respectively of 6 Q_S, and 8 Q_F edge triggered, clocked S/R flip-flops, with asynchronous Preset option. All flip-flops are unconditionally preset to "1" during power turn on.

The AND array combines 16 external inputs $I_{0\text{-}15}$ with 6 internal inputs $Q_{0\text{-}5}$ fed back from the State register to form up to 48 Transition terms (AND terms). All Transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the Low to High transition of the Clock pulse. Both True and Complement Transition terms can be generated by optional use of the internal input variable (C) from the Complement array. Also, if desired, the Preset input can be converted to $\overline{\text{Output-Enable}}$ function, as an additional user programmable option.

Both devices are available in commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S104/105, I or N, and for the military temperature range (−55°C to +125°C) specify S82S104/105, I.

FEATURES

- **Field programmable (Ni-Cr link)**
- **16 input variables**
- **8 output functions**
- **48 transition terms**
- **6-BIT state register**
- **8-BIT output register**
- **Transition complement array**
- **Positive edge trigger clock**
- **Programmable asynchronous preset or output enable**
- **Power-on preset to all "1" of internal registers**
- **90ns maximum I/O delay**
- **650mW power dissipation (typical)**
- **TTL compatible**
- **Single +5V supply**

APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Elevator controllers**
- **Security locking systems**

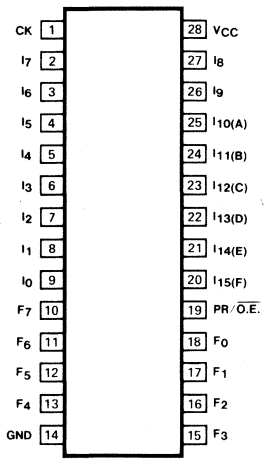
TRUTH TABLE (Output Control)

I_O	INPUT OPTION		F_N
	PR	$\overline{\text{O.E.}}$	
X	H		H
+10V	L		Q_S
X		H	H/Hi-Z
X		L	Q_F
+10V		L	Q_S

NOTES

1. Positive Logic:
   $S/R = T_0 + T_1 + T_2 \ldots\ldots T_{47}$
   $T_n = (I_0 \bullet I_1 \bullet I_2 \ldots) \bullet (P_0 \bullet \overline{P_1 \ldots P_5})$
2. Either Preset (active-High) or $\overline{\text{Output Enable}}$ (active-Low) are available, but not both. The desired function is a user programmable option.
3. ↑ denotes transition from Low to High level.
4. R = S = High is an illegal input condition.

PIN CONFIGURATION

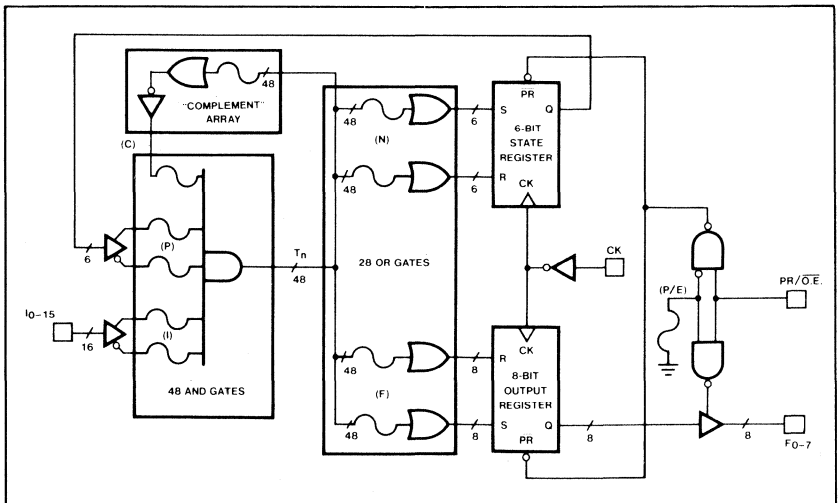


I = Ceramic
N = Plastic

TRUTH TABLE (All flip-flops)

V_{CC}	INPUT OPTION		CK	R	S	STATE REGISTER	OUTPUT REGISTER
	PR	$\overline{\text{O.E.}}$				Q_S	Q_F
+5V	H		X	X	X	H	H
	L	X	↑	L	L	Q_S	Q_F
	L	X	↑	L	H	L	L
	L	X	↑	H	L	H	H
	L	X	↑	H	H	INDET.	INDET.
↑	X	X	X	X	X	H	H

BLOCK DIAGRAM



NOTE I, P, C, N, F, and P/E are user programmable connections.

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			°C
T_A	Operating			
	N82S104/105	0	+75	
	S82S104/105	−55	+125	
T_{STG}	Storage	−65	+150	

THERMAL RATINGS

TEMPERATURE	MILITARY-	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHARACTERISTICS

N82S104/105: $0° \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S104/105: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TEST CONDITIONS[6]	N82S104/105 Min	N82S104/105 Typ[1]	N82S104/105 Max	S82S104/105 Min	S82S104/105 Typ[1]	S82S104/105 Max	UNIT
	Input voltage[3]								V
V_{IH}	High	V_{CC} = Max	2			2			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp[3,4]	V_{CC} = Min, I_{IN} = −18mA		−0.8	−1.2		−0.8	−1.2	
	Output voltage	V_{CC} = Min							V
V_{OH}	High (82S105)[3,5]	I_{OH} = −2mA	2.4			2.4			
V_{OL}	Low[3,6]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
	Input current								μA
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
I_{IL}	Low	V_{IN} = 0.45V		−10	−100		−10	−150	
I_{IL}	Low (CK input)	V_{IN} = 0.45V		−50	−250		−50	−350	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage[7]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S105)[7]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		−1	−40		−1	−60	
I_{OS}	Short circuit (82S105)[4,5]	V_{OUT} = 0V	−20		−70	−15		−85	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} = Max		120	170		120	180	mA
	Capacitance[7]	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output	V_{OUT} = 2.0V		10			10		

NOTES
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other condition above those indicated in the operation of the device specifications is not implied.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with V_{IL} applied to $\overline{O.E.}$ and a logic high stored, or with V_{IH} applied to PR.
6. Measured with a programmed logic condition for which the output is at a low logic level, and V_{IL} applied to PR/$\overline{O.E.}$. Output sink current is supplied thru a resistor to V_{CC}.
7. Measured with V_{IH} applied to PR/$\overline{O.E.}$.
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the PR/$\overline{O.E.}$ input grounded, all other inputs at 4.5V and the outputs open.

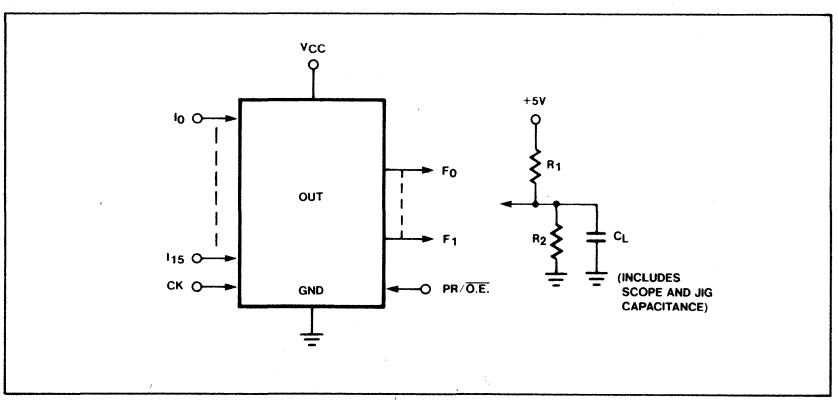
AC ELECTRIC CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S104/105: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S104/105: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

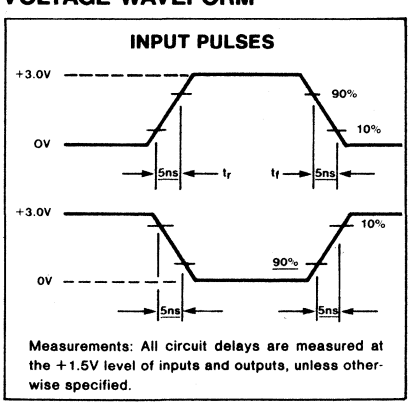
	PARAMETER	TO	FROM	N82S104/105			S82S104/105			UNIT
				Min	Typ[1]	Max	Min	Typ[1]	Max	
	Clock pulse									ns
T_{CKH}	Clock high	CK–	CK+		10			10		
T_{CKL}	Clock low	CK+	CK–		10			10		
T_{CKP}	Period	CK+	CK+		65			65		
	Set up time									ns
T_{IS1}	Input	CK+	Input ±		40			40		
T_{IS2}	Input (through Complement array)	CK+	Input ±		70			70		
T_{VS}	Power-on preset	CK–	V_{CC}+		10			10		
T_{PRS}	Preset	CK–	PR–		–10			–10		
	Hold time									ns
T_{IH}	Input	Input ±	CK+		–15			–15		
	Propagation delay									ns
T_{CKO}	Clock	Output ±	CK+		25			25		
T_{OE}	Output enable	Output–	$\overline{O.E.}$–		25			25		
T_{OD}	Output disable	Output+	$\overline{O.E.}$+		25			25		
T_{SRE}	State register enable	Output ±	I_O+		50			50		
T_{SRD}	State register disable	Output ±	I_O–		50			50		
T_{PR}	Preset	Output+	PR+		50			50		
T_{PPR}	Power-on preset	Output+	V_{CC}+		70			70		

NOTE
1. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.

TEST LOAD CIRCUIT



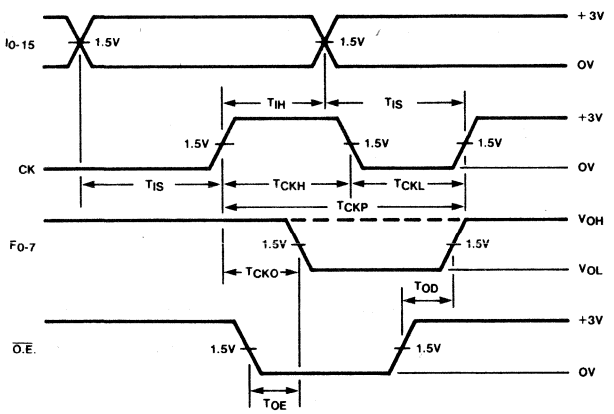
VOLTAGE WAVEFORM



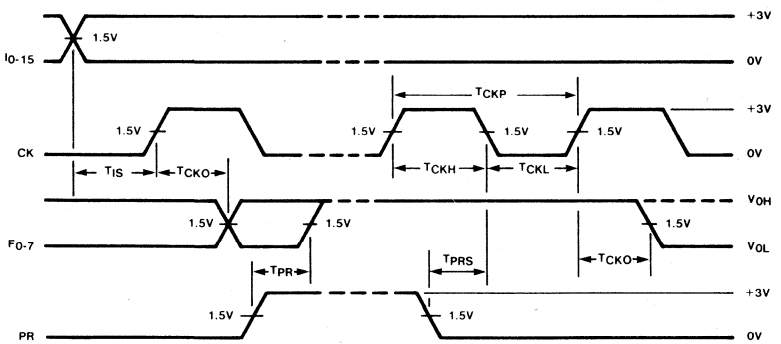
Measurements: All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

TIMING DIAGRAMS

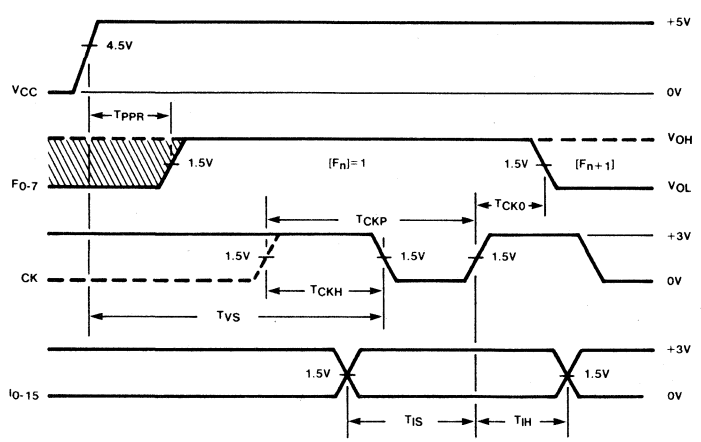
SEQUENTIAL MODE



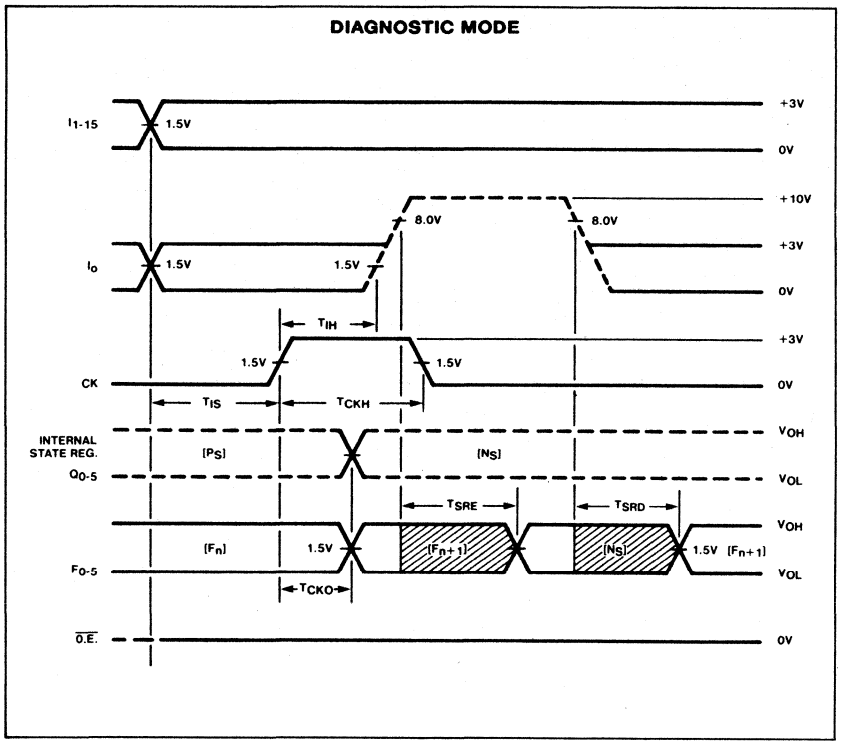
ASYNCHRONOUS PRESET



POWER-ON PRESET



TIMING DIAGRAMS (Cont'd)



MEMORY TIMING DEFINITIONS

T_{CKH} Width of input clock pulse.

T_{CKL} Interval between clock pulses.

T_{CKP} Clock period.

T_{IS1} Required delay between beginning of valid Input and positive transition of clock.

T_{IS2} Required delay between beginning of valid Input and positive transition of clock, when using optional Complement Array (two passes necessary through the AND array).

T_{VS} Required delay between V_{CC} (after power-on) and negative transition of clock preceding first reliable clock pulse.

T_{PRS} Required delay between negative transition of asynchronous Preset and negative transition of clock preceding first reliable clock pulse.

T_{IH} Required delay between positive transition of clock and end of valid Input data.

T_{CKO} Delay between positive transition of clock and when Outputs become valid (with PR/$\overline{O.E.}$ low).

T_{OE} Delay between beginning of Output Enable Low and when Outputs become valid.

T_{OD} Delay between beginning of Output Enable High and when Outputs are in the off state.

T_{SRE} Delay between input I_O transition to Diagnostic mode and when the Outputs reflect the contents of the State Register.

T_{SRD} Delay between input I_O transition to Logic mode and when the Outputs reflect the contents of the Output Register.

T_{PR} Delay between positive transition of Preset and when Outputs become valid at "1".

T_{PPR} Delay. between V_{CC} (after power-on) and when Outputs become preset at "1".

DESCRIPTION

The 82S106 (Open collector outputs) and 82S107 (3-state outputs) are bipolar Programmable ROM Patches organized as 48 words by 8 bits, addressed via a 16 bit programmable address comparator. Each word can be assigned a unique address code, P_n, within a 64K (2^{16}) address range by programming the comparator inputs High, Low, or Don't care via True/Complement input buffers.

The contents of each word are also programmable, and are enabled to the active-High Patch outputs only when a programmed address is detected, which causes the $\overline{\text{Flag}}$ output to go Low. For all unprogrammed addresses, the device outputs remain High (82S106) or Hi-Z (82S107) while the $\overline{\text{Flag}}$ output remains High. The $\overline{\text{Flag}}$ is open collector to allow wire-ANDing for expansion to more than 48 patch words.

The 82S106 and 82S107 are fully TTL compatible and can be programmed in the field by following the fusing procedure outlined in this data sheet, or by means of commercially available equipment.

Both devices are available in commercial and military temperature ranges. For the commercial range (0°C to +75°C) specify N82S106/107, I or N, and for the military temperature range (-55°C to +125°C) specify S82S106/107, I.

FEATURES

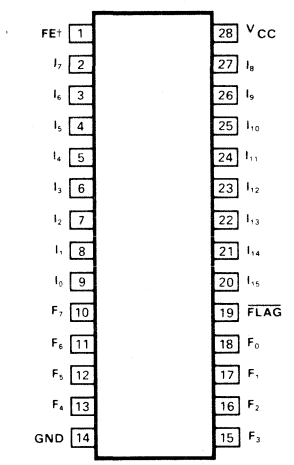
- **Field programmable (Ni-Cr link)**
- **Address Inputs: 16**
- **Data Outputs: 8**
- **Patch Words: 48**
- **Address access time:**
  S82S106/107—100ns Max
  N82S106/107—70ns Max
- **Power dissipation: 600mW typ**
- **Input loading:**
  S82S106/107: -150μA Max
  N82S106/107: -100μA Max
- **Open collector $\overline{\text{Flag}}$**
- **Output option:**
  82S106: Open collector
  82S107: 3-state
- **Output disabled state**
  3-state—Hi-Z
  Open collector—Hi

APPLICATIONS

- **ROM data modifications**
- **Memory address trap**
- **Digital filter**
- **Interrupt request/vector generator**
- **Data security encoder**

PIN CONFIGURATION

I,N PACKAGE*

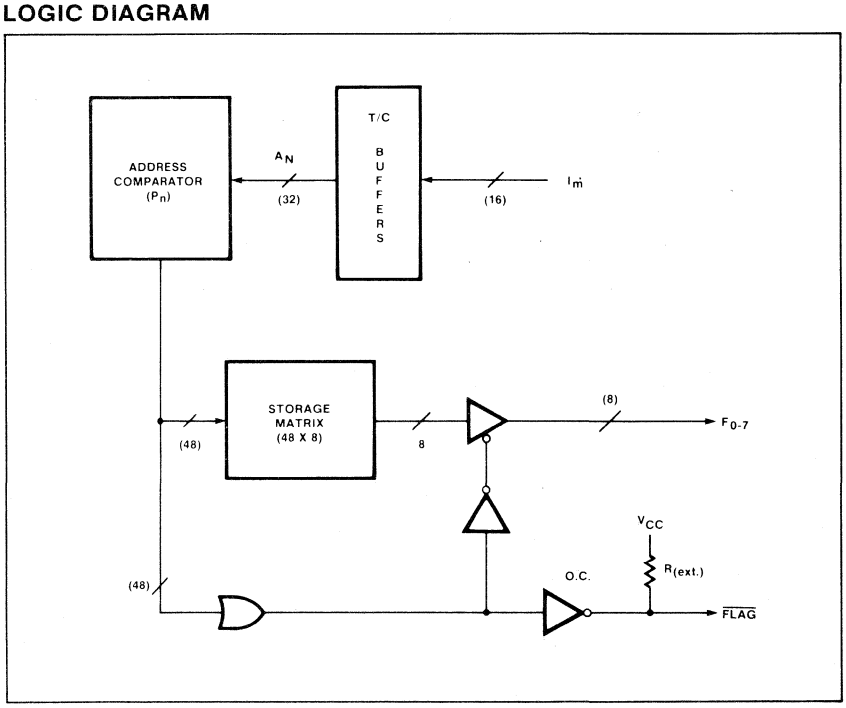


*I = Ceramic
N= Plastic
†Open during normal operation

TRUTH TABLE

? $A_N = P_N$	$\overline{\text{Flag}}$	F_{0-7}	
		82S106	82S107
NO	1	1	Hi-Z
YES	0	Stored Data	

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			°C
T_A	Operating			
	N82S106/107	0	+75	
	S82S106/107	-55	+125	
T_{STG}	Storage	-65	+150	

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHARACTERISTICS

N82S106/107: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S106/107: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N82S106/107 Min	N82S106/107 Typ[2]	N82S106/107 Max	S82S106/107 Min	S82S106/107 Typ[2]	S82S106/107 Max	UNIT
	Input voltage[3]								V
V_{IH}	High	V_{CC} = Max	2			2			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp[3,4]	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage	V_{CC} = Min							V
V_{OH}	High (82S107)[3,5]	I_{OH} = -2mA	2.4			2.4			
V_{OL}	Low[3,6] (F_{0-7})	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
V_{OL}	Low[3,6] ($\overline{Flag}$)	I_{OL} = 4.8mA		0.35	0.45		0.35	0.50	
	Input current								μA
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage[7]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S107)[7]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		-1	-40		-1	-60	
I_{OS}	Short circuit (82S107)[4,8]	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} = Max		120	170		120	180	mA
	Capacitance[7]	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output	V_{OUT} = 2.0V		17			17		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S106/107: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S106/107: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

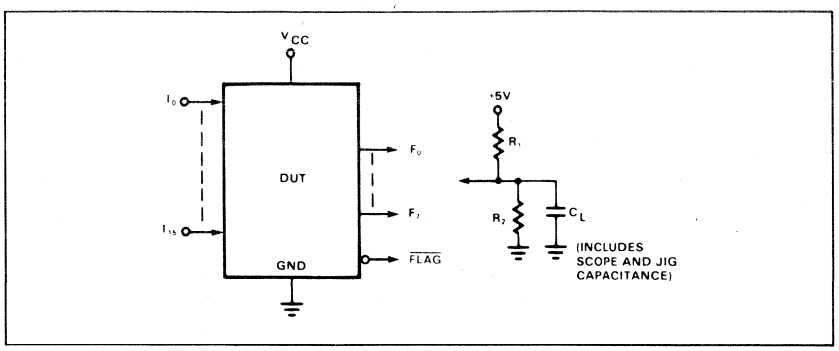
PARAMETER		TO	FROM	N82S106/107 Min	N82S106/107 Typ[2]	N82S106/107 Max	S82S106/107 Min	S82S106/107 Typ[2]	S82S106/107 Max	UNIT
	Access time									ns
T_{IA}	Address	Output	Input		45	70		45	100	
T_{FL}	Enable	$\overline{Flag}$	Input		40	70		40	100	

NOTES on following page.

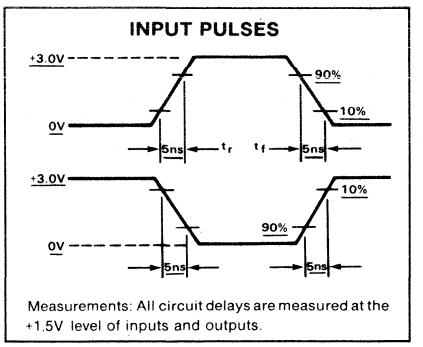
NOTES

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation of the device specification is not implied.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at the time.
5. Measured with the Patch enabled ($A_N = P_N$) and a logic high stored.
6. Measured with a programmed logic condition for which the output under test is at a low logic level when the Patch is enabled ($A_N = P_N$). Output sink current is applied thru a resistor to V_{CC}.
7. Measured with the Patch disabled ($A_N \neq P_N$).
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with all inputs at 4.5V and the outputs open.

TEST LOAD CIRCUIT

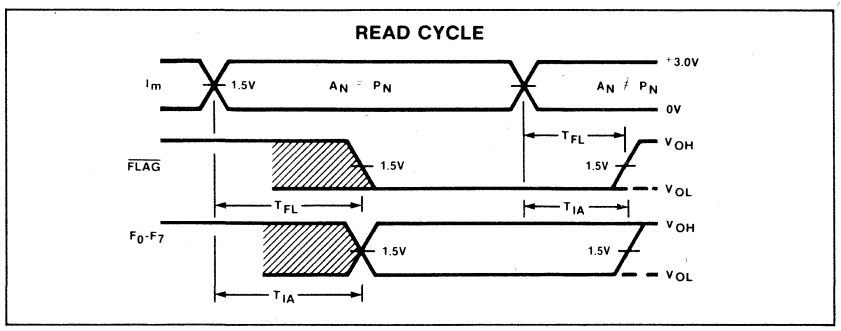


VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the +1.5V level of inputs and outputs.

TIMING DIAGRAM



TIMING DEFINITIONS

T_{IA} Delay between latest Address variable change and when Data Output becomes stable.

T_{FL} Delay between latest Address variable change and when $\overline{Flag}$ output becomes stable.

VIRGIN DEVICE

The 82S106/107 are shipped in an unprogrammed state, characterized by:

1. All internal Ni-Cr links are intact.
2. Each comparator address (P-term) contains both true and complement values of every input variable I_m (P-terms always logically "false").
3. The storage Matrix contains all "1".
4. The polarity of each output is set to active high.
5. All outputs are at a low logic level.

RECOMMENDED PROGRAMMING PROCEDURE

To program up to 48 address-data pair locations, follow the Program/Verify procedures outlined below. To maximize recovery from programming errors, leave all links corresponding to unused address-data pairs intact.

SET-UP

Terminate all device outputs with a 10K resistor to +5V. Set GND (pin 14) to 0V.

ADDRESS COMPARATOR

Program Pn Address

Program one input at the time and one P-term at the time. Unused comparator inputs must be programmed as Don't Care for all programmed P-terms.

1. Set FE (pin 1) to V_{FEL}, and V_{CC} (pin 28) to V_{CCP}.
2. Disable all device outputs by setting $\overline{Flag}$ (pin 19) to V_{IH}.
3. Disable all comparator inputs by applying V_{IX} to inputs I_0 through I_{15}.
4. Address the P-term to be programmed (No. 0 through 47) by forcing the corresponding binary code on outputs F_0 through F_5 with F_0 as LSB. Use standard TTL logic levels V_{OHF} and V_{OLF}.

5a. If the P-term contains neither I_0 nor $\overline{I_0}$ (input is a Don't Care), fuse both I_0 and $\overline{I_0}$ links by executing both steps 5b and 5c, before continuing with step 7.

5b. If the P-term contains I_0, set to fuse the $\overline{I_0}$ link by lowering the input voltage at I_0 from V_{IX} to V_{IH}. Execute step 6.

5c. If the P-term contains $\overline{I_0}$, set to fuse the I_0 link by lowering the input voltage at I_0 from V_{IX} to V_{IL}. Execute step 6.

6a. After t_D delay, raise FE from V_{FEL} to V_{FEH}.

6b. After t_D delay, pulse the $\overline{Flag}$ input from V_{IH} to V_{IX} for a period t_p.

6c. After t_D delay, return FE input to V_{FEL}.

7. Disable programmed input by returning I_0 to V_{IX}.
8. Repeat steps 5 through 7 for all other input variables.
9. Repeat steps 4 through 8 for all other P-terms.
10. Remove V_{IX} from all input variables.

VERIFY P_n ADDRESS

1. Set FE to V_{FEL}, and V_{CC} to V_{CCP}.
2. Enable F_7 output by setting $\overline{Flag}$ to V_{IX}.
3. Disable all comparator inputs by applying V_{IX} to inputs I_0 through I_{15}.
4. Address the P-term to be verified (No. 0 through 47) by forcing the corresponding binary code on outputs F_0 through F_5.
5. Interrogate Input I_0 as follows:
   A. Lower the input voltage at I_0 from V_{IX} to V_{IH}, and sense the logic state of output F_7.
   B. Lower the input voltage at I_0 from V_{IH} to V_{IL}, and sense the logic state output F_7.

The state of I_0 contained in the P-term is determined in accordance with the following truth table:

I_0	F_7	COMPARATOR INPUT STATE CONTAINED IN P-TERM
0 1	1 0	$\overline{I_0}$
0 1	0 1	I_0
0 1	1 1	Don't Care
0 1	0 0	(I_0), ($\overline{I_0}$)

Note that 2 tests are required to uniquely determine the state of the input contained in the P-term.

6. Disable verified input by returning I_0 to V_{IX}.
7. Repeat steps 5 and 6 for all other input variables.
8. Repeat steps 4 through 7 for all other P-terms.
9. Remove V_{IX} from all comparator inputs.

STORAGE MATRIX

Program Output Data

Program one output at the time for one P-term at the time.

1. Set FE to V_{FEL}.
2. Disable the chip by setting $\overline{Flag}$ to V_{IH}.
3. After t_D delay, set V_{CC} to V_{CCS}, and inputs I_6 through I_{15} to V_{IH}, V_{IL}, or V_{IX}.
4. Address the P-term to be programmed (No. 0 through 47) by applying the corresponding binary code to comparator inputs I_0 through I_5, with I_0 as LSB.
5. To program a logic "0" at output F_0, force F_0 to V_{OPF}.

6a. After t_D delay, raise FE (pin 1) from V_{FEL} to V_{FEH}.

6b. After t_D delay, pulse the $\overline{Flag}$ input from V_{IH} to V_{IX} for a period t_p.

6c. After t_D delay, return FE input to V_{FEL}.

6d. After t_D delay, remove V_{OPF} from output F_0.

7. Repeat steps 5 and 6 for all other output functions.
8. Repeat steps 4 through 7 for all other P-terms.
9. Remove V_{CCS} from V_{CC}.

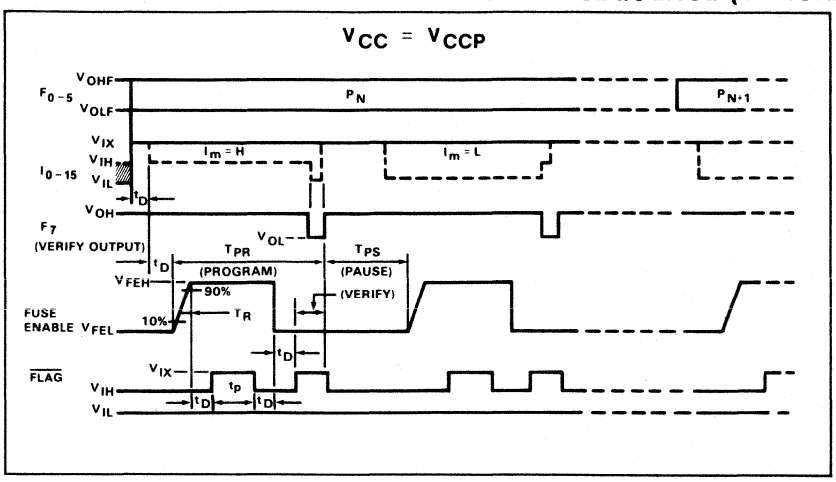
Verify Output Data

1. Set FE to V_{FEL}.
2. Disable the chip by setting $\overline{Flag}$ to V_{IH}.
3. After t_D delay, set V_{CC} to V_{CCS}, and inputs I_0 through I_{15} to V_{IH}, V_{IL}, or V_{IX}.
4. Address the P-term to be verified (No. 0 through 47) by applying the corresponding binary code to comparator inputs I_0 through I_5.
5. After t_D delay, enable the chip by setting $\overline{Flag}$ to V_{IL}.
6. To determine the status of each output link in the Storage Matrix, sense the state of outputs F_0 through F_7. The status of the link is given by the following truth table:

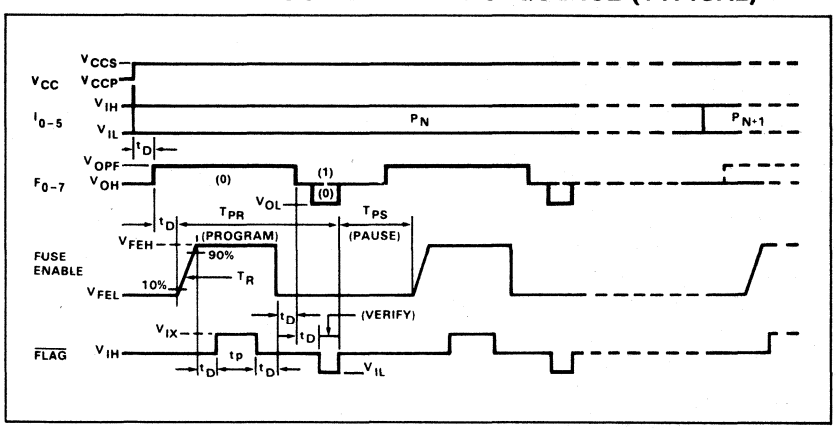
F_P	LINK
0 1	Fused Present

7. Repeat steps 4 through 6 for all other P-terms.
8. Remove V_{CCS} from V_{CC}.

ADDRESS COMPARATOR PROGRAM-VERIFY SEQUENCE (TYPICAL)



STORAGE MATRIX PROGRAM-VERIFY SEQUENCE (TYPICAL)



PROGRAMMING SYSTEM SPECIFICATIONS[1] (T_A = +25°C)

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCS}	V_{CC} supply (program/verify Storage Matrix)[2]	I_{CCS} = 550mA, min. Transient or steady state	8.25	8.5	8.75	V
I_{CCS}	I_{CC} limit	V_{CCS} = +8.50 ± .25V	550		1,000	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = 0V			-500	
	Forced output voltage					V
V_{OHF}	High		2.4		5.5	
V_{OLF}	Low		0	0.4	0.8	
	Output current					
I_{OHF}	High	V_{OHF} = +5.5V			100	μA
I_{OLF}	Low	V_{OLF} = 0V			-1	mA
V_{IX}	$\overline{\text{Flag}}$ program enable level		9.5	10	10.5	V
I_{IX1}	Input current	V_{IX} = +10V			2.5	mA
I_{IX2}	$\overline{\text{Flag}}$ input current	V_{IX} = +10V			5.0	mA
V_{FEH}	FE supply (program)[3]	I_{FEH} = 300 ± 25mA, Transient or steady state	16.0	17.0	18.0	V
V_{FEL}	FE supply (idle)	I_{FEL} = -1mA, max	1.25	1.5	1.75	V
I_{FEH}	FE supply current limit	V_{FEH} = +17 ± 1V	275	300	325	mA
V_{CCP}	V_{CC} supply (program/verify Address Comparator)	I_{CCP} = 550mA, min. Transient or steady state	4.75	5.0	5.25	V
I_{CCP}	I_{CC} limit	V_{CCP} = +5.0 ± .25V	550		1,000	mA
V_{OPF}	Forced output (program)		9.5	10	10.5	V
I_{OPF}	Output current (program)				10	mA
T_R	Output pulse rise time		10		50	μs
t_p	$\overline{\text{Flag}}$ programming pulse width		0.3	0.4	0.5	ms[5]
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time			0.6		ms
$\frac{T_{PR}}{T_{PR} + T_{PS}}$	Programming duty cycle				50	%
F_L	Fusing attempts per link				2	cycle
V_S	Verify threshold[4]		1.4	1.5	1.6	V

NOTES

1. These are specifications which a Programming System must satisfy in order to be qualified by Signetics.
2. Bypass V_{CC} to GND with a 0.01μf capacitor to reduce voltage spikes.
3. Care should be taken to ensure that the voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
4. V_S is the sensing threshold of the FPRP output voltage for a programmed link. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
5. These are new limits resulting from device improvements, and which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment.

16X48X8 FPRP PROGRAM TABLE

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) _____

CUSTOMER SYMBOLIZED PART # _____

DATE RECEIVED _____

COMMENTS _____

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____

REV_____ DATE _____

PROGRAM TABLE ENTRIES				
COMPARATOR INPUT			OUTPUT FUNCTION	
I_m	$\overline{I_m}$	Don't care	"1"	"0"
H	L	— (dash)	A	• (period)

NOTES

1. Enter (-) for unused inputs of all active P-terms.
2. Enter (A) for unused outputs of all active P-terms.
3. Unused inputs and outputs are FPRP terminals left floating.
4. Input and output fields of inactive P-terms can be left blank.

PRODUCT TERM																	ACTIVE LEVEL							
NO.	COMPARATOR INPUT																H	H	H	H	H	H	H	H
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OUTPUT FUNCTION							
																	7	6	5	4	3	2	1	0
0																								
1																								
2																								
3																								
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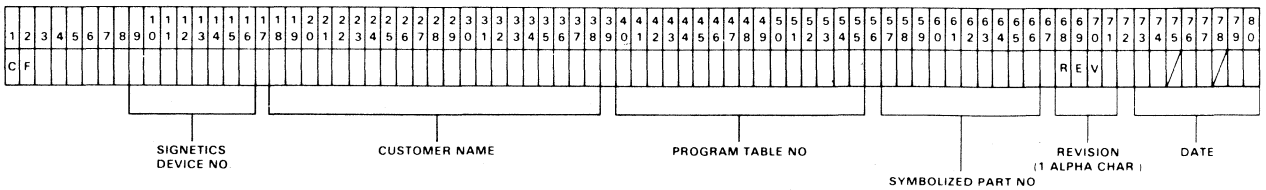
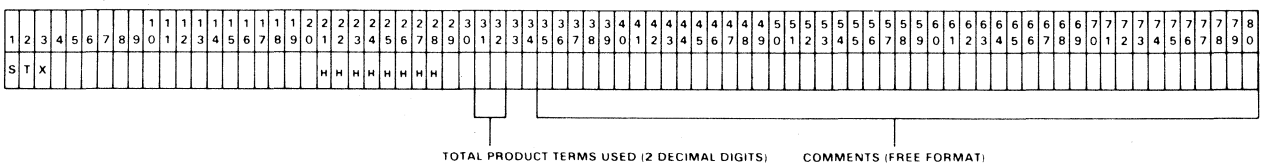
PUNCHED CARD CODING FORMAT

The FPRP Program Table can be supplied directly to Signetics in punched card form, using standard 80-column IBM cards. For each FPRP Program Table, the customer should prepare in input card deck in accordance with the following format. Product Term cards 3 through 50 can be in any order. Not all 48 Product terms need to be present. Unused Product Terms require no entry cards, and will be skipped during the actual programming sequence:

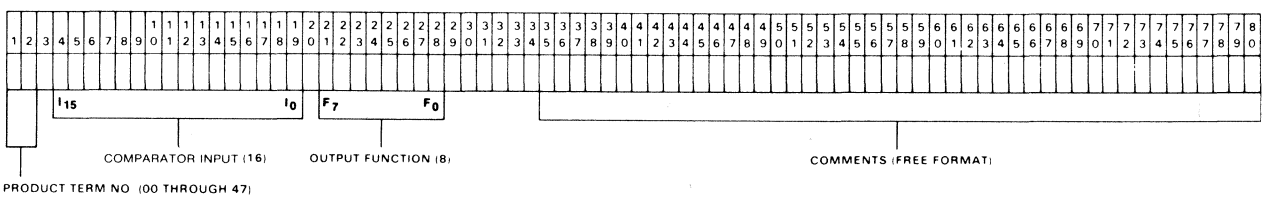
CARD NO.1—Free format within designated fields.



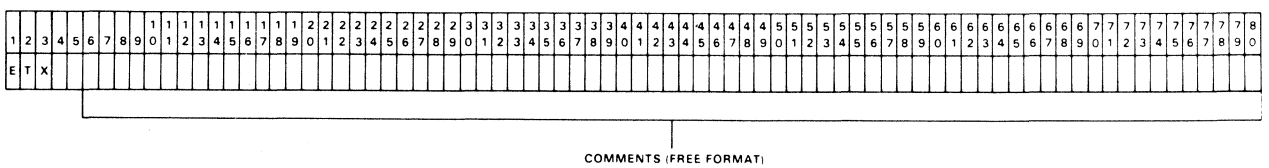
CARD NO. 2—



CARD NO. 3 through NO. 50



CARD NO. 51



Comparator input entries are determined in accordance with the following table:

COMPARATOR INPUT		
I_m	$\overline{I_m}$	Don't care
H	L	—(dash)

Output function entries are determined in accordance with the following table:

OUTPUT FUNCTION	
"1"	"0"
A	• (period)

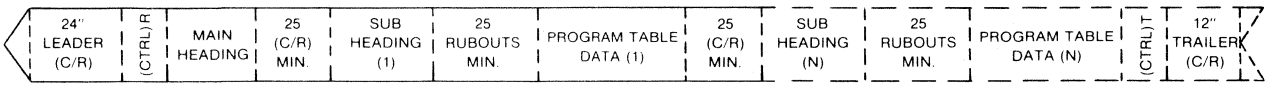
NOTES

1. Enter (-) for unused inputs of all active P-terms.
2. Enter (A) for unused outputs of all active P-terms.
3. Unused inputs and outputs are FPRP terminals left floating.
4. Input and output fields of inactive P-terms can be left blank.

TWX TAPE CODING FORMAT

The FPRP Program Table can be sent to Signetics in ASCII code format via airmail using any type of 8-level tape (paper, mylar; fanfold, etc.), or via TWX: just dial (910) 339-9283, tell the operator to turn the paper puncher on, and acknowledge. At the end of transmission instruct the operator to send tape to Signetics Order Entry.

A number of Program Tables can be sequentially assembled on a continuous tape as follows, however limit tape length to a roll of 1.75 inch inside diameter, and 4.25 inch outside diameter:



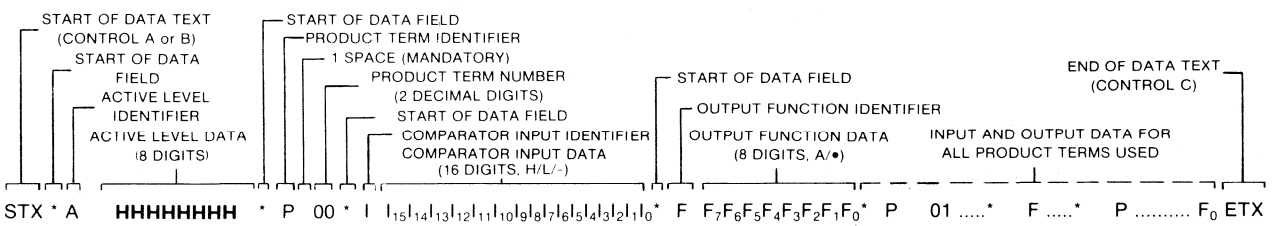
A. The MAIN HEADING at the beginning of tape includes the following information, with each entry preceded by a ($) character, whether used or not:

1. Customer Name _____
2. Customer TWX No. _____
3. Date _____
4. Purchase Order No. _____
5. Number of Program Tables _____
6. Total Number of Parts _____

B. Each SUB HEADING should contain specific information pertinent to each Program Table as follows, with each entry preceded by a ($) character, whether used or not:

1. Signetics Device No. _____
2. Program Table No. _____
3. Revision _____
4. Date _____
5. Customer Symbolized Part No. _____
6. Number of Parts _____

C. Program Table data blocks are initiated with an STX character, and terminated with an ETX character. The body of the data consists of Output Active Level, Product Term, and Output Function information separated by appropriate identifiers in accordance with the following format:



COMPARATOR INPUT		
I_m	$\overline{I_m}$	Don't care
H	L	—(dash)

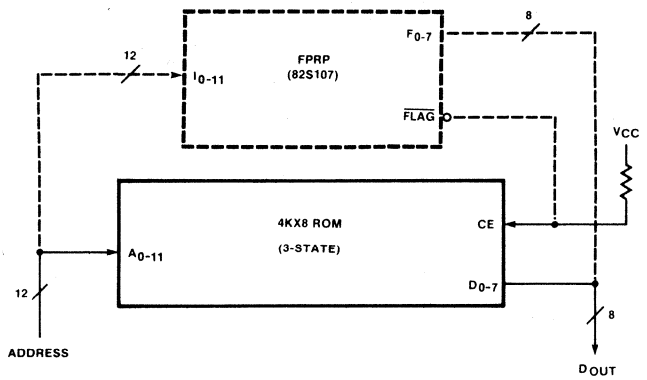
OUTPUT FUNCTION	
"1"	"0"
A	• (period)

NOTES
1. Enter (-) for unused inputs of all active P-terms.
2. Enter (A) for unused outputs of all active P-terms.
3. Unused inputs and outputs are FPRP terminals left floating.

Although the Product Term data are shown entered in sequence, this is not necessary. It is possible to input only one Product Term, if desired. Unused Product Terms require no entry. ETX signalling end of Program Table may occur with less than the maximum number of Product Terms entered.

NOTES
1. Corrections to any entry can be made by backspace and rubout. However, limit consecutive rubouts to less than 25.
2. P-Terms can be re-entered any number of times. The last entry for a particular P-Term will be interpreted as valid data.
3. Any P-Term can be deleted entirely by inserting the character (E) immediately following the P-Term number to be deleted, i.e., *P 25E deletes P-Term 25.
4. To facilitate an orderly Teletype print out, carriage returns, line feeds, spaces, etc. may be interspersed between data groups, but only preceding an asterisk (*).
5. Comments are allowed between data fields, provided that an asterisk (*) is not used in any Heading or Comment entry.

TYPICAL APPLICATION



PATCH SPECIFICATIONS

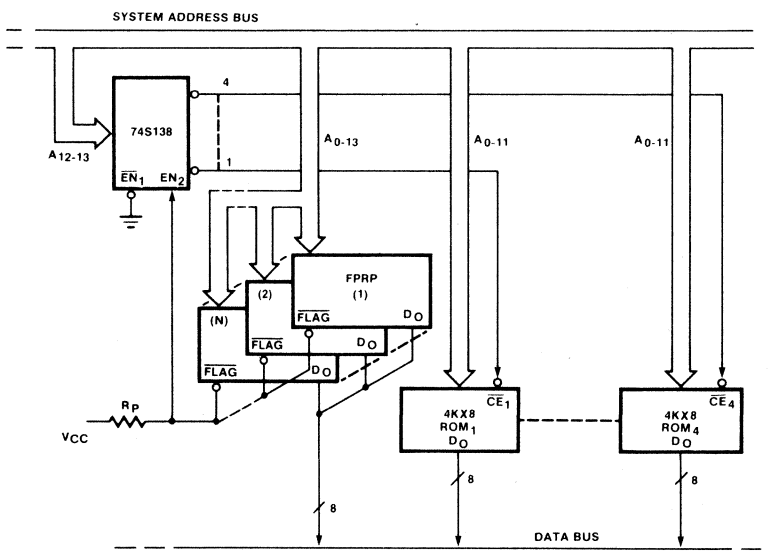
ADDRESS	NEW DATA
750	A9
5FE	7F
0A4, 0A5, 0A6, 0A7	B4

FPRP PROGRAM TABLE

INPUT ADDRESS	NO.	PRODUCT TERM: COMPARATOR INPUT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	ACTIVE LEVEL	OUTPUT FUNCTION 7	6	5	4	3	2	1	0	OUTPUT DATA
																		H	H	H	H	H	H	H	H	
750	0	–	–	–	–	L	H	H	H	L	H	L	H	L	L	L	L		A	•	A	•	A	•	•	A	A9
5FE	1	–	–	–	–	L	H	L	H	H	H	H	H	H	H	H	L		•	A	A	A	A	A	A	A	7F
OA4-OA7	2	–	–	–	–	L	L	L	L	H	L	H	L	L	H	–	–		A	•	A	A	•	A	•	•	B4
I/O ASSIGNMENT		UNUSED				A_{11}											A_0		D_7							D_0	

Since Patch inputs $I_{12\text{-}15}$ are unused, they are programmed Don't Care (–), and left open in the circuit. Note however that I_0 and I_1 are programmed as (–) in P-term 2 because they define an address block of 4 memory locations.

EXPANSION



When more than 48 memory locations need to be patched, several devices can be paralleled by wire-ANDing the $\overline{Flag}$ outputs.

MOS MEMORY DATA SPECIFICATIONS

signetics

DESCRIPTION

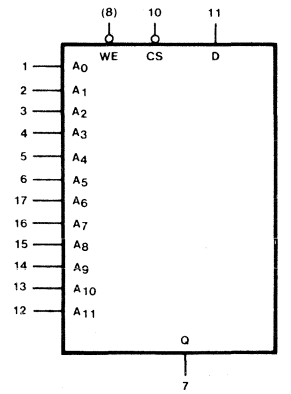
The Signetics 2613 is a high speed, 4096 bit static random access memory. Utilizing the Signetics n-channel, si-gate Mini-MOS technology to achieve high performance and high bit density, the 4096x1 organization offers a cost effective solution for designer needs.

The 2613 is fully static (access time=cycle time), all input and outputs are TTL compatible, and it has a single +5V supply. It is manufactured in the industry standard pinout 18 pin package.

FEATURES

- **Typical access time 80ns**
- **Power dissipation 0.1 mW/bit typical**
- **3-state TTL compatible output**
- **All inputs TTL compatible**
- **Fully static operation**
- **Identical access & cycle times**
- **High output impedance during write**
- **Single +5V power supply**
- **Standard 18-pin DIP**

LOGIC SYMBOL



V_{CC} = Pin 18
GND = Pin 9

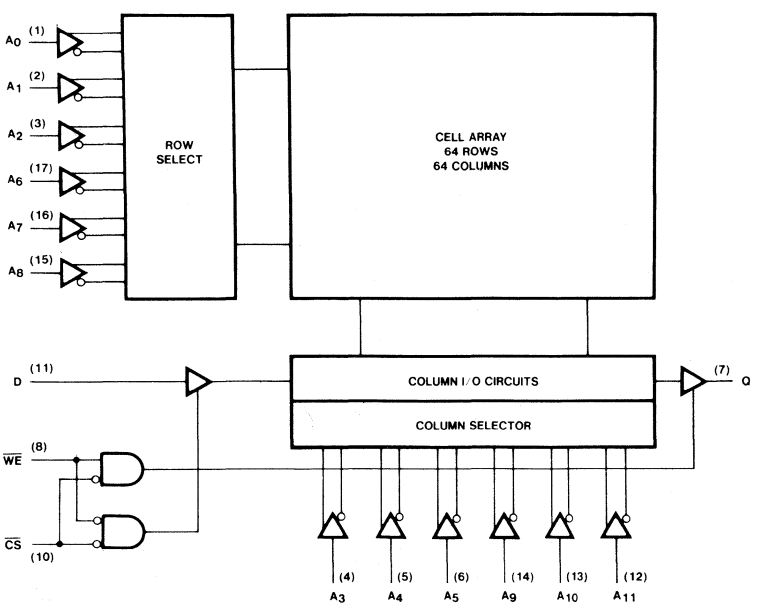
ORDERING CODE (See Packages Section for further information)

PACKAGES	ACCESS TIME			
	150ns	200ns	250ns	450ns
Ceramic DIP	2613-15I	2613-20I	2613-25I	2613-45I
Cerdip	2613-15F	2613-20F	2613-25F	2613-45F
Plastic DIP	2613-15N	2613-20N	2613-25N	2613-45N

PIN DESIGNATION

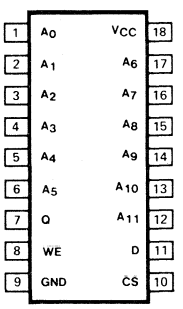
SYMBOL	DESCRIPTION
A_0-A_{11}	Address inputs
$\overline{CS}$	Chip select (active LOW) input
$\overline{WE}$	Write enable (active LOW) input
D	Data input
Q	Data output (3-State)
GND	Ground (0V)
V_{CC}	Power supply (+5V)

BLOCK DIAGRAM



V_{CC} = Pin 18
GND = Pin 9
( ) = Pin numbers

PIN CONFIGURATION



MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D	Q
Not selected	H	X	X	(Z)
Write 'O'	L	L	L	(Z)
Write 'I'	L	L	H	(Z)
Read	L	H	X	Data

X = Don't care
H = HIGH voltage level
L = LOW voltage level
(Z) = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING
Operating temperature range	0 to 70°C
Storage temperature range	−55 to 150°C
Supply voltage to ground potential	−0.5 to 7V
Short circuit output current	−20mA
Input voltage	−0.5 to 7V

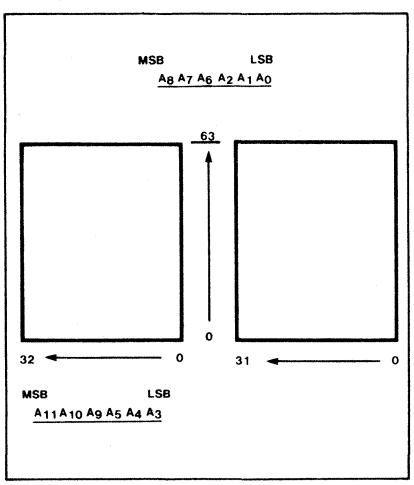
NOTE

1. Stresses above these listed as "Absolute Maximum Ratings" may damage the device. These ratings are meant for short term stress only, prolonged exposure at these ratings may affect device reliability.

DC CHARACTERISTICS : T_A = O°C to 70°C, V_{CC} = 5V ± 5%

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{IL}	Input LOW voltage range		−0.5	0.8	V
V_{IH}	Input HIGH voltage range		2.0	V_{CC}	V
I_{IL}	Input LOW current	V_{CC} = MAX, V_{IN} = OV		−10	uA
I_{IH}	Input HIGH current	V_{CC} = MAX, V_{IN} = 5.25V		10	uA
V_{OL}	Output LOW voltage	V_{CC} = MIN, I_{OL} = 2.1mA		0.45	V
V_{OH}	Output HIGH voltage	V_{CC} = MIN, I_{OH} = −1.0mA	2.4		V
I_{OZL}	Output off current LOW	V_{CC} = MAX, V_{OUT} = 0.4V, $V_{\overline{CS}}$ = 2V		−10	uA
I_{OZH}	Output off current HIGH	V_{CC} = MAX, V_{OUT} = 5.25V, $V_{\overline{CS}}$ = 2V		10	uA
I_{CC}	Supply current	V_{CC} = MAX, $V_{\overline{CS}}$ = 2V		140	mA
C_{IN}	Input capacitance	$V_{\overline{CS}}$ = 2V, V_{IN} = OV, f = 1.0MHz		5.0	pF
C_{OUT}	Output capacitance	$V_{\overline{CS}}$ = 2V, V_{OUT} = OV, f = 1.0MHz		5.0	pF

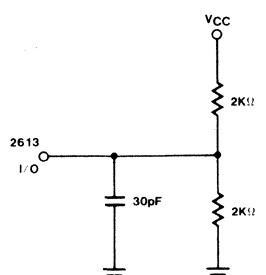
BIT MAP



ADDRESS SCRAMBLE

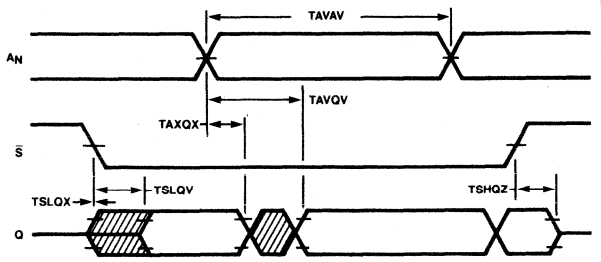
TESTER	2613	PIN
COLUMN		
A_0	A_3	4
A_1	A_4	5
A_2	A_5	6
A_3	A_9	14
A_4	A_{10}	13
A_5	A_{11}	12
ROW		
A_6	A_0	1
A_7	A_1	2
A_4	A_2	3
A_9	A_6	17
A_{10}	A_7	16
A_{11}	A_8	15

TEST LOAD CIRCUIT



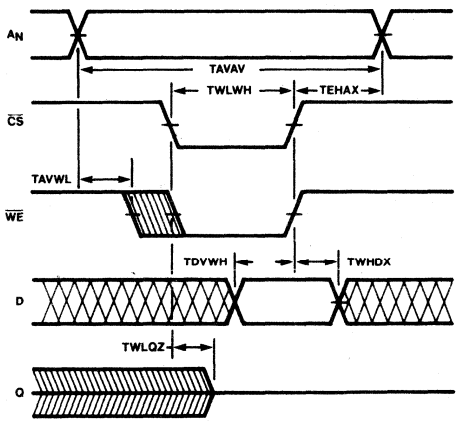
AC WAVEFORMS

READ CYCLE



Other conditions: $\overline{W}$ = HIGH, D = Don't Care, shaded areas indicate unknown output states.

WRITE CYCLE



Shaded areas indicate Don't Care input conditions or unknown output conditions.

AC CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5.0 V ± 5%

SYMBOL	PARAMETER	TEST CONDITIONS	2613-15		2613-20		2613-25		2613-45		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
	READ CYCLE										
TAVAV	Read cycle time		150		200		250		450		ns
TSLQX	Select LOW to output on		0		0		0		0		ns
TSHQZ	Select HIGH to output off		0	35	0	40	0	60	0	100	ns
TAXQX	Address to output invalid		10		10		10		20		ns
TSLQV	Chip select access time			50		70		100		120	ns
TAVQV	Address access time			150		200		250		450	ns
	WRITE CYCLE										
TAVAV	Write cycle time		150		200		250		450		ns
TAVWL	Address to write set up time		30		50		70		70		ns
TWLWH	Write LOW pulse duration		75		100		125		200		ns
TDVWH	Data set up time		50		75		100		200		ns
TWHDX	Data hold time		0		0		0		0		ns
TWLQZ	Write to output off		0	35	0	40	0	60	0	100	ns
TEHAX	Write HIGH to address invalid		20		20		20		20		ns

DESCRIPTION

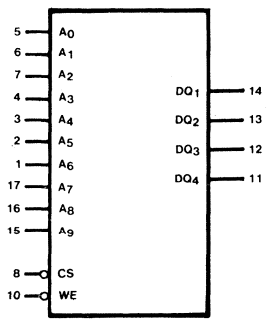
The Signetics 2614 is a high speed, 4096 bit static random access memory. Utilizing the Signetics n-channel, si-gate Mini-MOS technology to achieve high performance and high bit density, the 1024 x 4 organization offers a cost effective solution for designer needs.

The 2614 is fully static (access time = cycle time), all input and outputs are TTL compatible, and it has a single +5V supply. It is manufactured in the industry standard pinout 18 pin package.

FEATURES

- **Typical access time of 80ns**
- **Power dissipation of 0.1mW/bit typical**
- **3-state TTL compatible output**
- **All inputs TTL compatible**
- **Fully static operation**
- **Identical access & cycle time**
- **Single +5V power supply**
- **Standard 18-pin DIP**

LOGIC SYMBOL



V_{CC} = Pin 18
GND = Pin 9

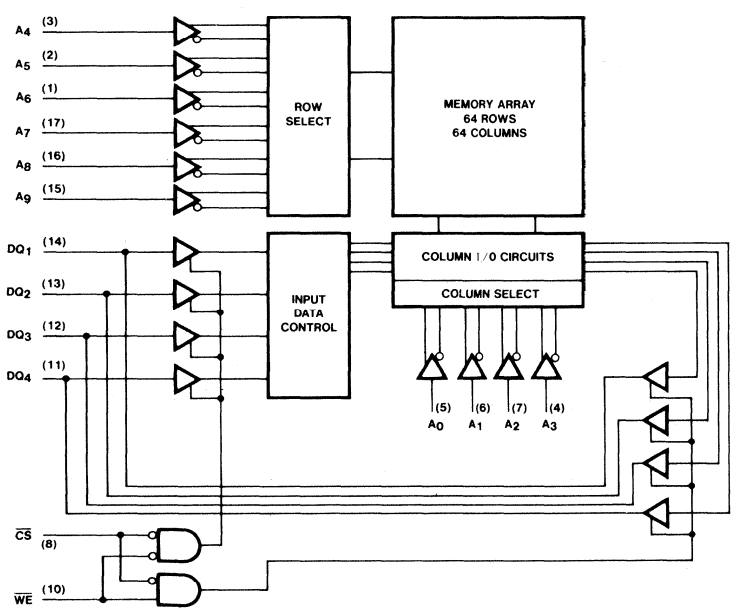
ORDERING CODE (See Packages Section for further information)

PACKAGES	ACCESS TIME			
	150ns	200ns	250ns	450ns
Ceramic DIP	2614-15I	2614-20I	2614-25I	2614-45I
Cerdip	2614-15F	2614-20F	2614-25F	2614-45F
Plastic	2614-15N	2614-20N	2614-25N	2614-45N

PIN DESIGNATION

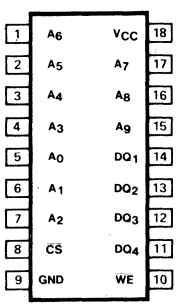
SYMBOL	NAME & FUNCTION
A_0-A_9	Address inputs
$\overline{CS}$	Chip select (active LOW) input
$\overline{WE}$	Write enable (active LOW) input
DQ_1-DQ_4	Input/Output port (3-State)
GND	Ground (0V)
V	Power supply (+5V)

BLOCK DIAGRAM



V_{CC} = Pin 18
GND = Pin 9
( ) = Pin numbers

PIN CONFIGURATION



MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS $\overline{CS}$	INPUTS $\overline{WE}$	INPUTS DQ_{IN}	OUTPUT DQ_{OUT}
Not selected	H	X	X	(Z)
Read	L	H	(Z)	Data
Not allowed (bus contention)	L	H	H/L	Data
Write	L	L	Data	(Z)

NOTES
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1]

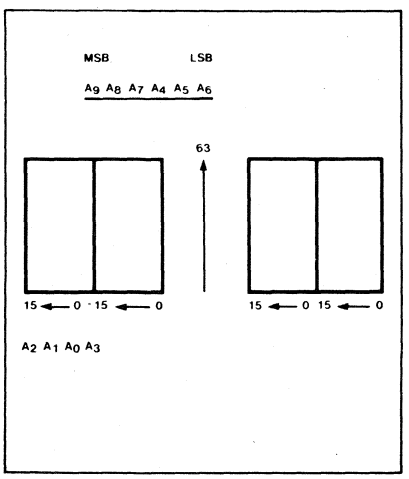
PARAMETER	RATING
Operating temperature range	−10 to 80°C
Storage temperature range	−55 to 150°C
Supply voltage to ground potential	−0.5 to 7V
Short circuit output current	−20mA
Input voltage	−0.5 to 7V

NOTE
1. Stresses above these listed as "Absolute Maximum Ratings" may damage the device. These ratings are meant for short term stress only, prolonged exposure at these ratings may affect device reliability.

DC CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ± 5%

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Max	UNIT
V_{IL}	Input LOW voltage range		−0.5	0.8	V
V_{IH}	Input HIGH voltage range		2.0	V_{CC}	V
I_{IL}	Input LOW current	V_{CC} = MAX, V_{IN} = 0V		−10	μA
I_{IH}	Input HIGH current	V_{CC} = MAX, V_{IN} = 5.25V		10	μA
V_{OL}	Output LOW voltage	V_{CC} = MIN, I_{OL} = 2.1mA		0.45	V
V_{OH}	Output HIGH voltage	V_{CC} = MIN, I_{OH} = −1.0mA	2.4		V
I_{OZL}	Output off current LOW	V_{CC} = MAX, V_{OUT} = 0.4V, $V_{\overline{CS}}$ = 2V		−10	μA
I_{OZH}	Output off current HIGH	V_{CC} = MAX, V_{OUT} = 5.25V, $V_{\overline{CS}}$ = 2V		10	μA
I_{CC}	Supply current	V_{CC} = MAX, $V_{\overline{CS}}$ = 2V		140	mA
C_{IN}	Input capacitance	$V_{\overline{CS}}$ = 2V, V_{IN} = 0V, f = 1.0MHz		5.0	pF
C_{OUT}	Output capacitance	$V_{\overline{CS}}$ = 2V, V_{OUT} = 0V, f = 1.0MHz		5.0	pF

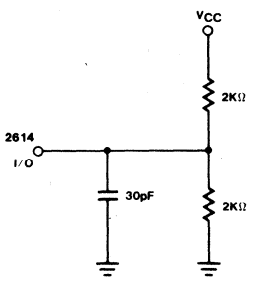
BIT MAP



ADDRESS SCRAMBLE

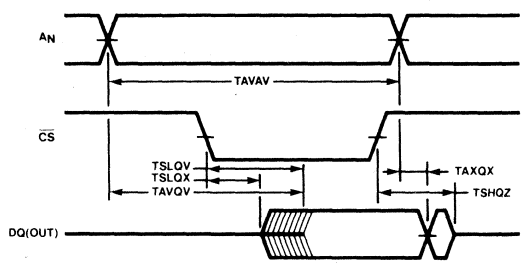
TESTER	2614	PIN
ROW		
A_0	A_3	4
A_1	A_0	5
A_2	A_1	6
A_3	A_2	7
COLUMN		
A_4	A_6	1
A_5	A_5	2
A_6	A_4	3
A_7	A_7	17
A_8	A_8	16
A_9	A_9	15

TEST LOAD CIRCUIT

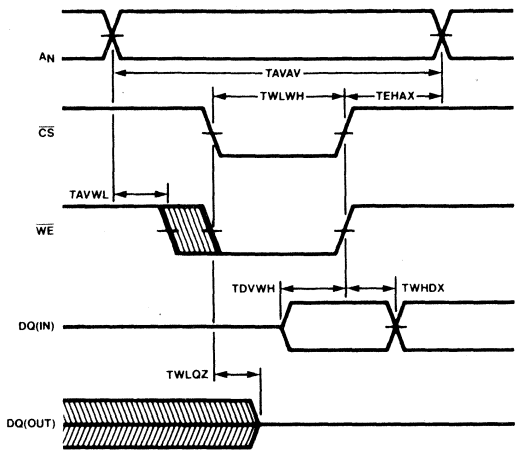


AC WAVEFORMS

READ CYCLE



WRITE CYCLE



AC CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} −5.0V ± 5%

SYMBOL	PARAMETER	TEST CONDITIONS	2614-15		2614-20		2614-25		2614-45		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
	READ CYCLE										
TAVAV	Read cycle time		150		200		250		450		ns
TSLQX	Select LOW to output on		0		0		0		0		ns
TSHQZ	Select HIGH to output off		0	35	0	40	0	60	0	100	ns
TAXQX	Address to output invalid		10		10		10		20		ns
TSLQV	Chip select access time			50		70		100		120	ns
TAVQV	Address access time			150		200		250		450	ns
	WRITE CYCLE										
TAVAV	Write cycle time		150		200		250		450		ns
TAVWL	Address to write set up time		30		50		70		70		ns
TWLWH	Write LOW pulse duration		75		100		125		200		ns
TDVWH	Data set up time		50		75		100		200		ns
TWHDX	Data hold time		0		0		0		0		ns
TWLQZ	Write to output off		0	35	0	40	0	60	0	100	ns
TEHAX	Write HIGH to address invalid		20		20		20		20		ns

OBJECTIVE SPECIFICATION

2690-2—F,I,N • 2690-3—F,I,N • 2690-4—F,I,N

DESCRIPTION

The 2690 is fabricated with double-poly n-channel silicon gate technology for high performance and high functional density. It uses a single transistor dynamic storage cell and dynamic circuitry to achieve high speed and low power dissipation.

The unique design of the 2690 allows it to be packaged in the industry standard 16-pin in-line package, which provides the highest system bit densities and is compatible with widely available automated handling equipment.

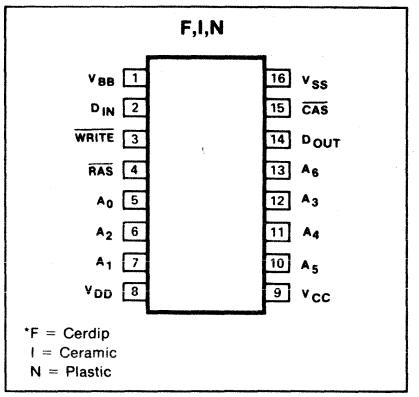
The use of the 16-pin package is made possible by multiplexing the 14 address bits (required to address one of 16,384 bits) into the 2690 on 7 address input pins. The two 7-bit address words are latched into the device by the 2 TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

The memory cell requires refreshing for data retention. This is most easily accomplished by performing a $\overline{RAS}$ only cycle at each of 128 row addresses every 2ms.

FEATURES

- **Access time:**
  2690-2: 150ns
  2690-3: 200ns
  2690-4: 250ns
- **Read and write cycle time:**
  2690-2: 375ns
  2690-3: 375ns
  2690-4: 410ns
- **Low power:**
  Operating: 462mW (max)
  Standby: 20mW (max)
- **±10% power supply margins**
- **On-chip latches for address and data in**
- **Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow 2-dimensional chip selection and extended page boundary**
- **Page mode addressing**
- **$\overline{RAS}$ only refresh**
- **Common I/O capability using "early write" operation**
- **All inputs TTL compatible**
- **3-state TTL compatible output**

PIN CONFIGURATION

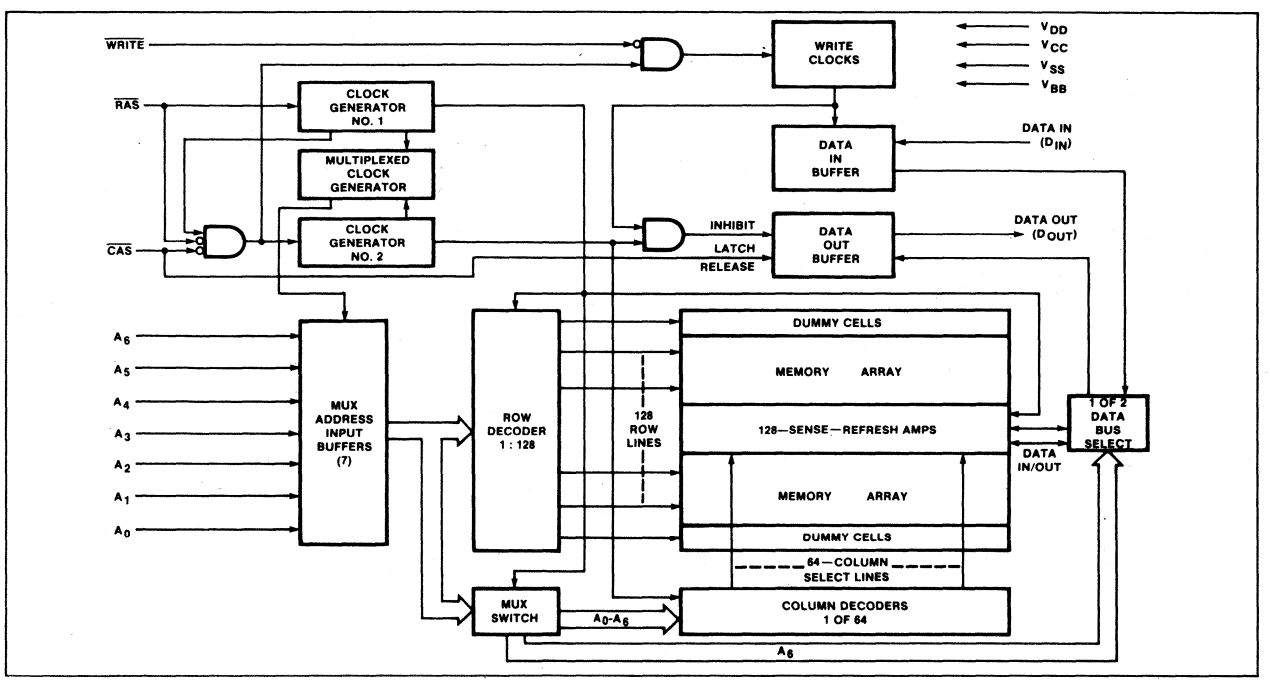


*F = Cerdip
I = Ceramic
N = Plastic

PIN DESIGNATION

PIN NO.	SYMBOL	NAME & FUNCTION
5-7, 10-13	A_0-A_6	Address inputs
15	$\overline{CAS}$	Column address strobe
2	D_{IN}	Data in
14	D_{OUT}	Data out
4	$\overline{RAS}$	Row address strobe
3	$\overline{WRITE}$	Read/write input
1	V_{BB}	Power (-5V)
9	V_{CC}	Power (+5V)
8	V_{DD}	Power (+12V)
16	V_{SS}	Ground

BLOCK DIAGRAM



AC CHARACTERISTICS[7,8,9]

T_A = 0°C to +70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V unless otherwise specified.

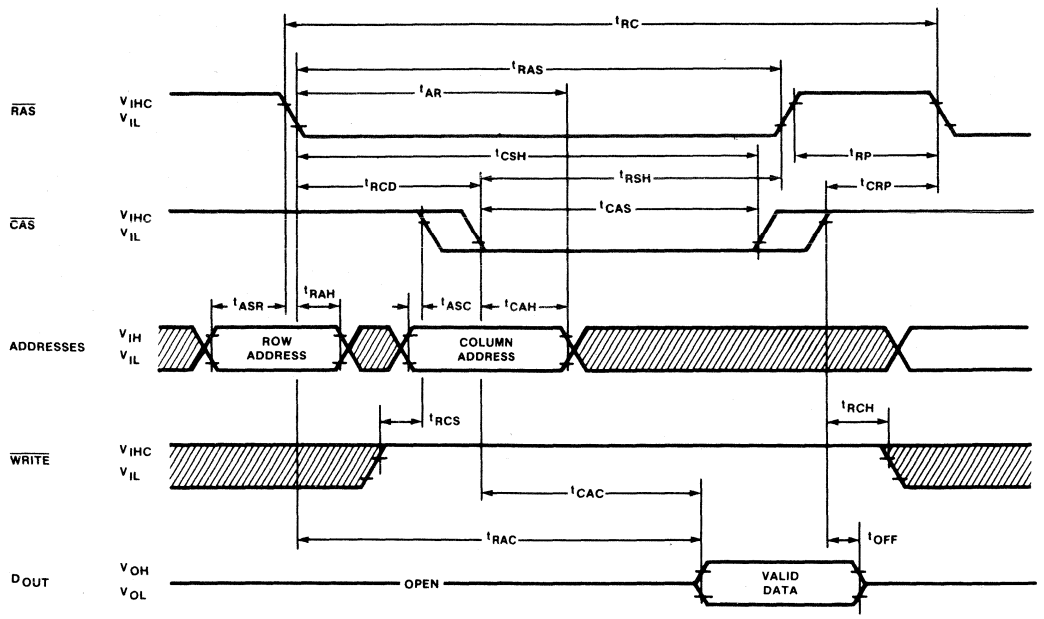
SYMBOL	PARAMETER	TEST CONDITIONS	2690-2		2690-3		2690-4		UNIT
			Min	Max	Min	Max	Min	Max	
	READ OR WRITE (EARLY) CYCLE								
t_{REF}	Refresh			2		2		2	ms
t_T[9]	Transition		3	35	3	50	3	50	ns
t_{RC}[15]	Random cycle		320		375		410		ns
t_{RAS}	$\overline{RAS}$ duration		150	10000	200	10000	250	10000	ns
t_{RP}	$\overline{RAS}$ precharge		100		120		150		ns
t_{RCD}[10]	Strobe delay		20	50	25	65	35	85	ns
t_{CAS}	$\overline{CAS}$ duration		100	10000	135	10000	165	10000	ns
t_{CRP}	$\overline{CAS}$ precharge		−20		−20		−20		ns
t_{RSH}	$\overline{RAS}$ hold		100		135		165		ns
t_{CSH}	$\overline{CAS}$ hold		150		200		250		ns
t_{ASR}	Row address set up		0		0		0		ns
t_{RAH}	Row address hold		20		25		35		ns
t_{ASC}	Column address set up		−10		−10		−10		ns
t_{CAH}	Column address hold		45		55		75		ns
t_{AR}	Address hold		95		120		160		ns
	READ CYCLE								
t_{RCS}	Read set up		0		0		0		ns
t_{RCH}	Read hold		0		0		0		ns
t_{OFF}[14]	Output turn off delay		0	40	0	50	0	60	ns
t_{RAC}[12,13]	Row access			150		200		250	ns
t_{CAC}[11,12]	Column access			100		135		165	ns
	WRITE (EARLY) CYCLE								
t_{WCS}[17]	Write set up		−20		−20		−20		ns
t_{WCH}	Write hold		45		55		75		ns
t_{WP}	Write duration		45		55		75		ns
t_{RWL}	Write to $\overline{RAS}$ lead		50		70		85		ns
t_{CWL}	Write to $\overline{CAS}$ lead		50		70		85		ns
t_{WCR}	Write to $\overline{RAS}$ hold		95		120		160		ns
t_{DS}[16]	Data set up		0		0		0		ns
t_{DH}[16]	Data hold		45		55		75		ns
t_{DHR}	Data to $\overline{RAS}$ hold		95		120		160		ns

NOTES

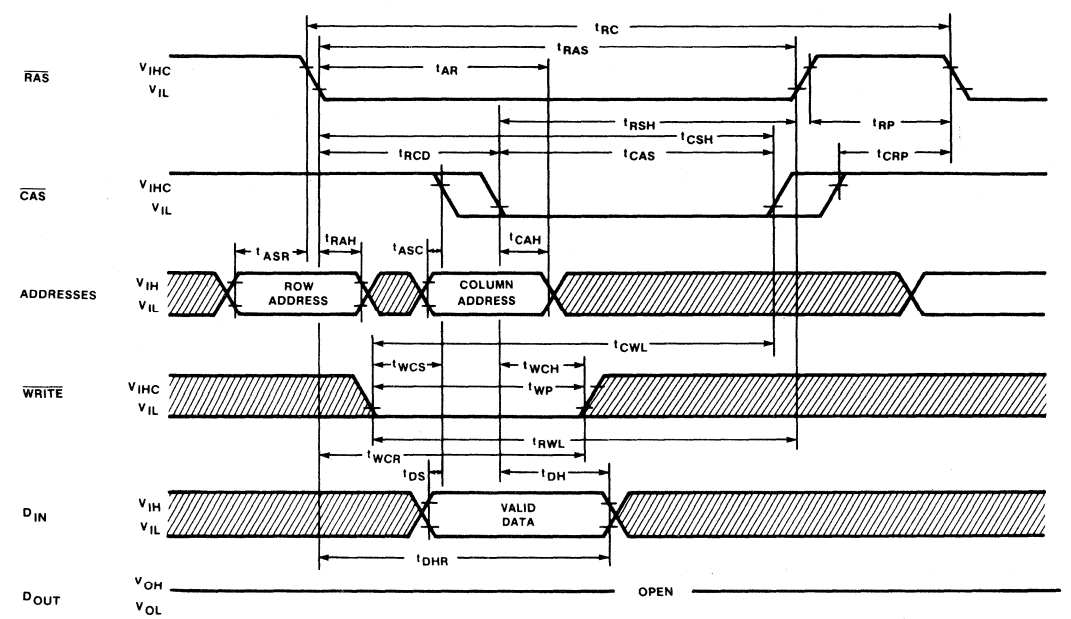
7. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
8. Ac measurements assume t_T = 5ns.
9. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
10. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
12. Measured with a load equivalent to 2 TTL loads and 100pF.
13. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value specified, t_{RAC} will increase by the amount that t_{RCD} exceeds the value specified.
14. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
15. The specifications for t_{RMW} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
16. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read/modify/write cycles.
17. t_{WCS} t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read/write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE (EARLY WRITE)



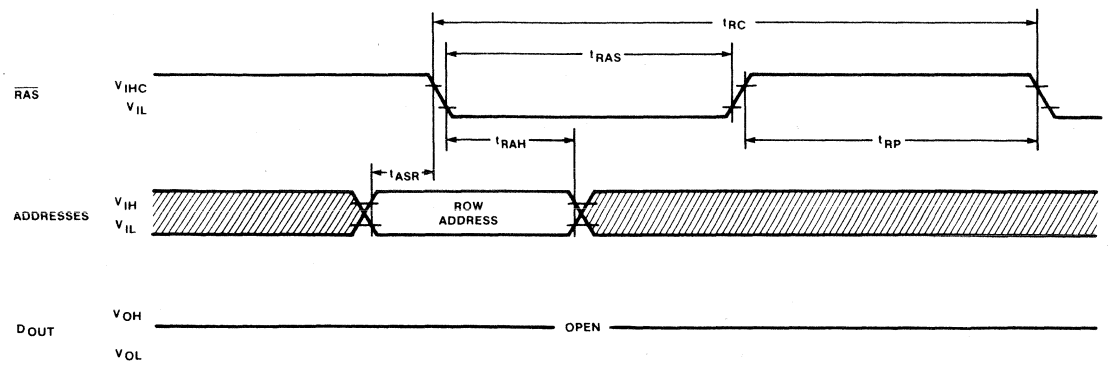
AC CHARACTERISTICS[7,8,9]

T_A = 0°C to +70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	2690-2		2690-3		2690-4		UNIT
			Min	Max	Min	Max	Min	Max	
	$\overline{RAS}$ ONLY REFRESH CYCLE								
t_{REF}	Refresh			2		2		2	ms
t_T[9]	Transition		3	35	3	50	3	50	ns
t_{RC}[15]	Random cycle		320		375		410		ns
t_{RAS}	$\overline{RAS}$ duration		150	10000	200	10000	250	10000	ns
t_{RP}	$\overline{RAS}$ precharge		100		120		150		ns
t_{ASR}	Row address set up		0		0		0		ns
t_{RAH}	Row address hold		20		25		35		ns
	READ/WRITE OR READ/MODIFY/WRITE								
t_{REF}	Refresh			2		2		2	ms
t_T[9]	Transition		3	35	3	50	3	50	ns
t_{RWC}	Read/write cycle		320		375		515		ns
t_{RMW}	Read/modify/write cycle		320		405		515		ns
t_{RRAS}	R/W $\overline{RAS}$ duration		185	10000	245	10000	305	10000	ns
t_{MRAS}	RMW $\overline{RAS}$ duration		215	10000	285	10000	355	10000	ns
t_{RP}	$\overline{RAS}$ precharge		100		120		150		ns
t_{RCD}[10]	Strobe delay		20	50	25	65	35	85	ns
t_{RCAS}	R/W $\overline{CAS}$ duration		135	10000	180	10000	230	10000	ns
t_{MCAS}	RMW $\overline{CAS}$ duration		165	10000	220	10000	270	10000	ns
t_{CRP}	$\overline{CAS}$ precharge		−20		−20		−20		ns
t_{RSH}	$\overline{RAS}$ hold		100		135		165		ns
t_{CSH}	$\overline{CAS}$ hold		150		200		250		ns
t_{ASR}	Row address set up		0		0		0		ns
t_{RAH}	Row address hold		20		25		35		ns
t_{ASC}	Column address set up		−10		−10		−10		ns
t_{CAH}	Column address hold		45		55		75		ns
t_{AR}	Address hold		95		120		160		ns
t_{RCS}	Read set up		0		0		0		ns
t_{RWD}	$\overline{RAS}$ to write delay		120		160		200		ns
t_{CWD}	$\overline{CAS}$ to write delay		70		95		125		ns
t_{RWL}	Write to $\overline{RAS}$ lead		50		70		85		ns
t_{CWL}	Write to $\overline{CAS}$ lead		50		70		85		ns
t_{WP}	Write duration		45		55		75		ns
t_{MOD}	Modify		0	9785	0	9715	0	9645	ns
t_{DS}[16]	Data set up		0		0		0		ns
t_{DH}[16]	Data hold		45		55		75		ns
t_{OFF}[14]	Output turn off delay		0	40	0	50	0	60	ns
t_{RAC}[12,13]	Row access		150		200		250		ns
t_{CAC}[11,12]	Column access		100		135		165		ns

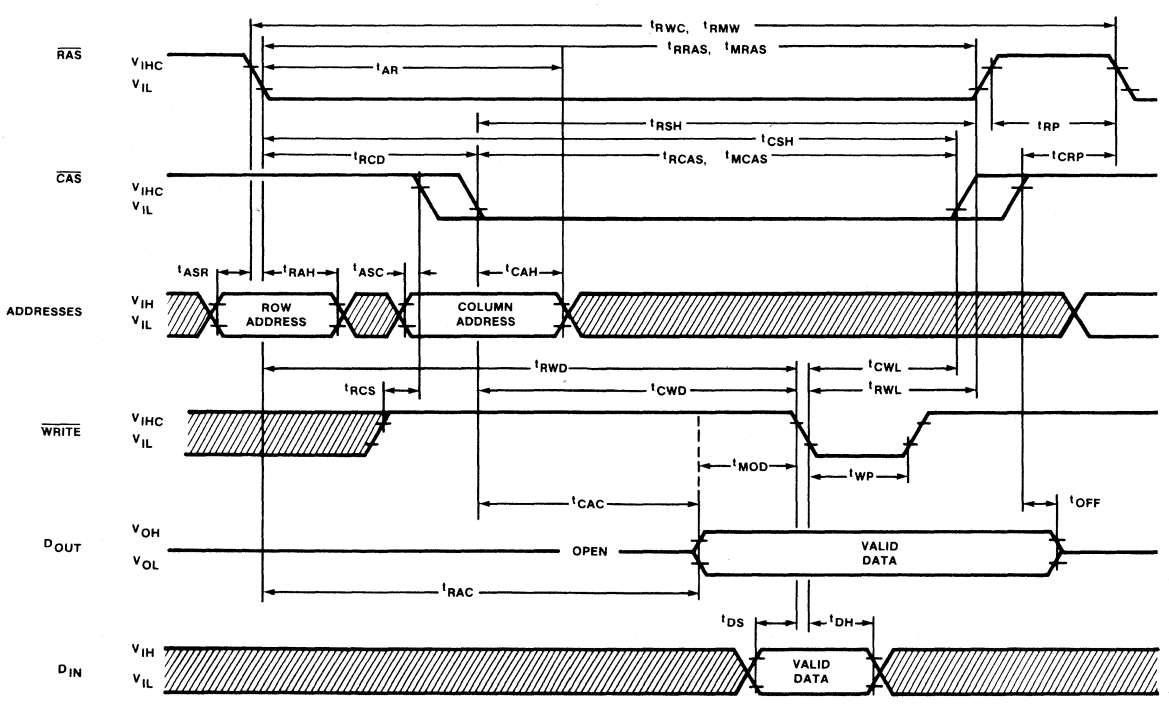
TIMING DIAGRAMS (Cont'd)

$\overline{RAS}$ ONLY REFRESH CYCLE



1. $\overline{CAS}$ = V_{IHC}
2. $\overline{WRITE}$ = Don't care

READ/WRITE, READ/MODIFY/WRITE CYCLE



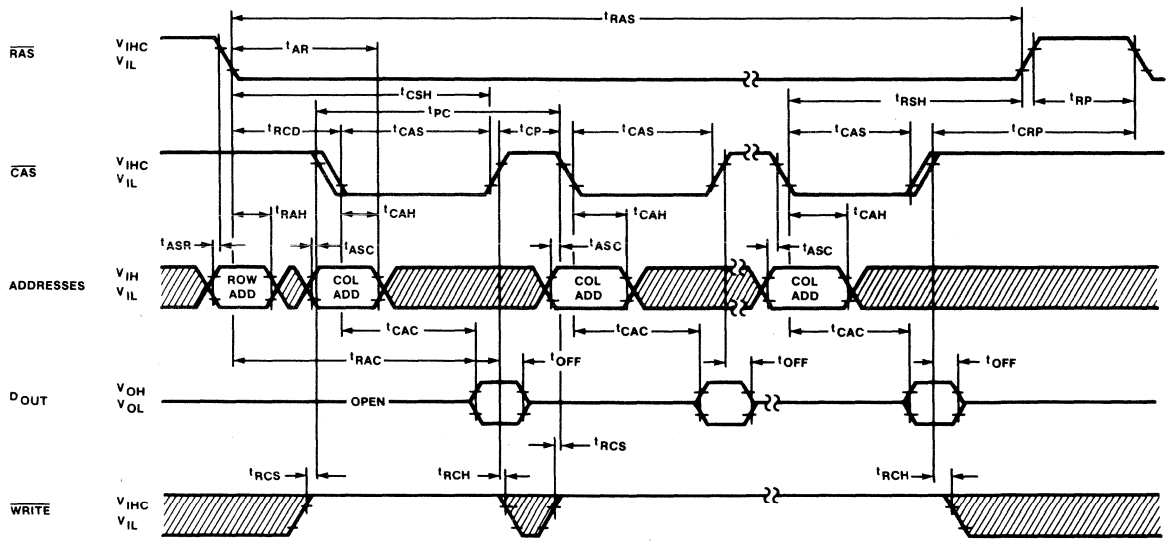
AC CHARACTERISTICS[7,8,9]

T_A = 0°C to +70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V unless otherwise specified.

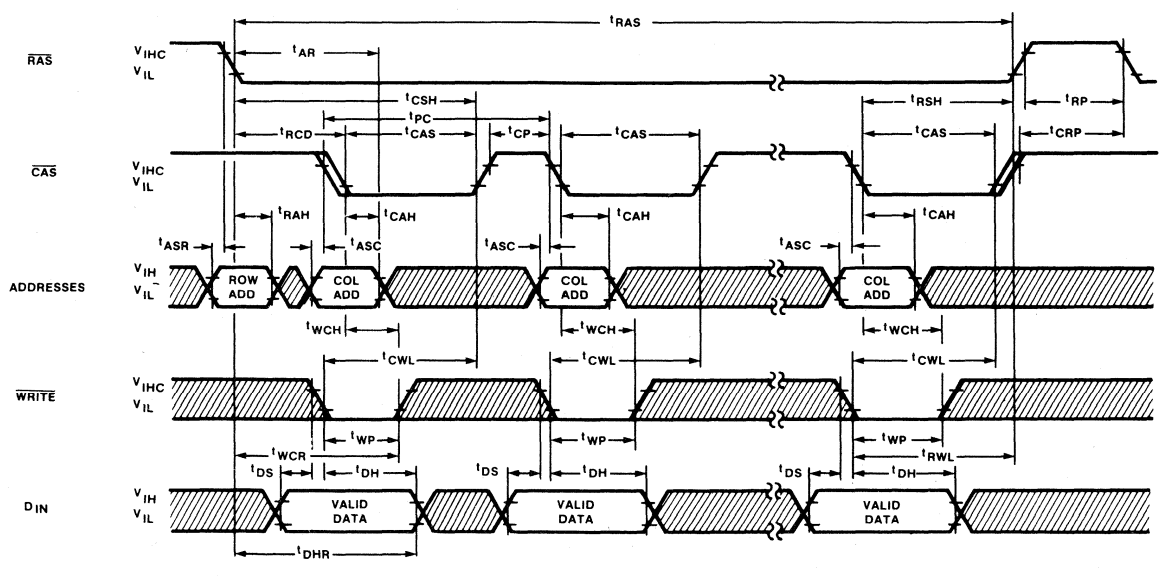
SYMBOL	PARAMETER	TEST CONDITIONS	2690-2		2690-3		2690-4		UNIT
			Min	Max	Min	Max	Min	Max	
	PAGE MODE CYCLES								
t_{REF}	Refresh			2		2		2	ms
t_T[9]	Transition		3	35	3	50	3	50	ns
t_{RAS}	$\overline{RAS}$ duration		150	10000	200	10000	250	10000	ns
t_{RP}	$\overline{RAS}$ precharge		100		120		150		ns
t_{RCD}[10]	Strobe delay		20	50	25	65	35	85	ns
t_{CAS}	$\overline{CAS}$ duration		100	10000	135	10000	165	10000	ns
t_{CP}	$\overline{CAS}$ HIGH duration		60		80		100		ns
t_{CSH}	$\overline{CAS}$ hold		150		200		250		ns
t_{PC}	Page mode cycle		170		225		275		ns
t_{RSH}	$\overline{RAS}$ hold		100		135		165		ns
t_{CRP}	$\overline{CAS}$ precharge		−20		−20		−20		ns
t_{ASR}	Row address set up		0		0		0		ns
t_{RAH}	Row address hold		20		25		35		ns
t_{ASC}	Column address set up		−10		−10		−10		ns
t_{CAH}	Column address hold		45		55		75		ns
t_{AR}	Address hold		95		120		160		ns
	PAGE MODE READ CYCLE								
t_{RCS}	Read set up		0		0		0		ns
t_{RCH}	Read hold		0		0		0		ns
t_{OFF}[14]	Output turn off delay		0	40	0	50	0	60	ns
t_{RAC}[12,13]	Row access		150		200		250		ns
t_{CAC}[11,12]	Column access		100		135		165		ns
t_{WCH}	Write hold		45		55		75		ns
t_{WP}	Write duration		45		55		75		ns
t_{CWL}	Write to $\overline{CAS}$ lead		50		70		85		ns
t_{RWL}	Write to $\overline{RAS}$ lead		50		70		85		ns
t_{WCR}	Write to $\overline{RAS}$ hold		95		120		160		ns
t_{DS}[16]	Data set up		0		0		0		ns
t_{DH}[16]	Data hold		45		55		75		ns
t_{DHR}	Data to $\overline{RAS}$ hold		95		120		160		ns

TIMING DIAGRAMS (Cont'd)

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



OBJECTIVE SPECIFICATION

2690-2—F,I,N • 2690-3—F,I,N • 2690-4—F,I,N

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING Min	RATING Max	UNIT
V_M	Voltage on any pin with respect to V_{BB}	-0.5	20	V
V_{PM}	Voltage on V_{DD}, V_{CC} pins with respect to V_{SS}	-1.0	15	V
	V_{BB} - V_{SS} (V_{DD} > V_{SS})		0	V
	Temperature range			°C
T_A	Operating	0	+70	
T_{STG}	Storage	-55	+150	
I_{SSC}	Output current			mA
	Short circuit		50	
P_D	Power dissipation		1	W

DC ELECTRICAL CHARACTERISTICS[2]

T_A[3] = 0°C to +70°C, V_{DD} = 12V ±10%, V_{CC}[4] = 5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
	Input voltage					V
V_{IL}	Low	Any input	-1.0		0.8	
V_{IH}	High	All inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7.0	
V_{IHC}	High	$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7		7.0	
	Output voltage[4]					V
V_{OL}	Low	I_{OL} = 4.2mA	0		0.4	
V_{OH}	High	I_{OH} = -5.0mA	2.4		V_{CC}	
	Leakage current					µA
I_{IL}	Input	Any input, V_{BB} = -5V, 0V < V_{IN} < 7V, All other pins not under test = 0V	-10		10	
I_{OL}	Output	D_{OUT} is disabled, 0V < V_{OUT} < 5.5V	-10		10	
	V_{DD} current[5]					mA
I_{DD1}	Operating	$\overline{RAS}$, $\overline{CAS}$ cycling			35	
I_{DD2}	Standby	$\overline{RAS}$ at V_{IHC}			1.5	
I_{DD3}	Refresh	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}			27	
I_{DD4}	Page mode	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling			27	
	Supply current					µA
I_{CC}	V_{CC}[6]					
I_{BB1}	Average V_{BB}	$\overline{RAS}$ and $\overline{CAS}$ cycling			200	
I_{BB2}	V_{BB}	$\overline{RAS}$ = V_{IHC}			100	
	Capacitance	Calculated from the equation C = $\frac{\Delta Q}{\Delta V}$ with ΔV = 3V				pF
C_{AD}	Address, D_{IN}				5	
C_C	$\overline{CAS}$, $\overline{RAS}$, $\overline{WRITE}$				10	
C_{OUT}	Output	$\overline{CAS}$ = V_{IHC} to disable D_{OUT}			7	

NOTES

1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages referenced to V_{SS}.
3. T_A is specified here for operation at frequencies to $t_{RC} \leq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible provided ac operating parameters are met, according to the following equation: T_A (max) °C = 70 - 9 X {cycle rate (MHz) - 2.66}.
4. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
5. I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. I_{DD} limits at cycle rates other than those specified are determined by the following equations:

   For the 2690-2/2690-3:
   I_{DD1} (max) mA = 10 + 9.4 X cycle rate (MHz)
   I_{DD3} (max) mA = 10 + 6.5 X cycle rate (MHz)
   I_{DD4} (max) mA = 10 + 3.75 X cycle rate (MHz)

   For the 2690-4:
   I_{DD1} (max) mA = 10 + 10.25 X cycle rate (MHz)
   I_{DD3} (max) mA = 10 + 7 X cycle rate (MHz)
   I_{DD4} (max) mA = 10 + 4.7 X cycle rate (MHz)
6. I_{CC} depends upon output loading. During readout of high level data, V_{CC} is connected through a low impedance (135Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

4027-2/4027-3/4027-4-F,I,N

DESCRIPTION

The 4027 is fabricated with n-channel silicon gate technology for high performance and high functional density, and uses a single transistor dynamic storage cell and dynamic circuitry to achieve high speed and low power dissipation.

The unique design of the 4027 allows it to be packaged in the industry standard 16-pin dual inline package, which provides the highest system bit densities and is compatible with widely available automated handling equipment.

The use of the 16-pin package is made possible by multiplexing the 12 address bits (required to address 1 of 4096 bits) into the 4027 on 6 address input pins. The two 6-bit address words are latched into the device by the 2TTL clocks, Row Address Strobe ($\overline{RAS}$), and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

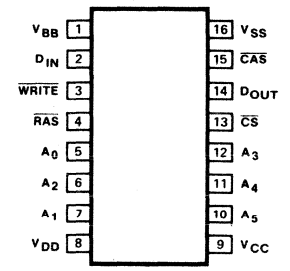
The single transistor dynamic storage cell provides high speed along with low power dissipation. The memory cell requires refreshing for data retention, and this is most easily accomplished by performing a read cycle at each of the 64 row addresses every 2ms, or by performing a $\overline{RAS}$ only cycle.

FEATURES

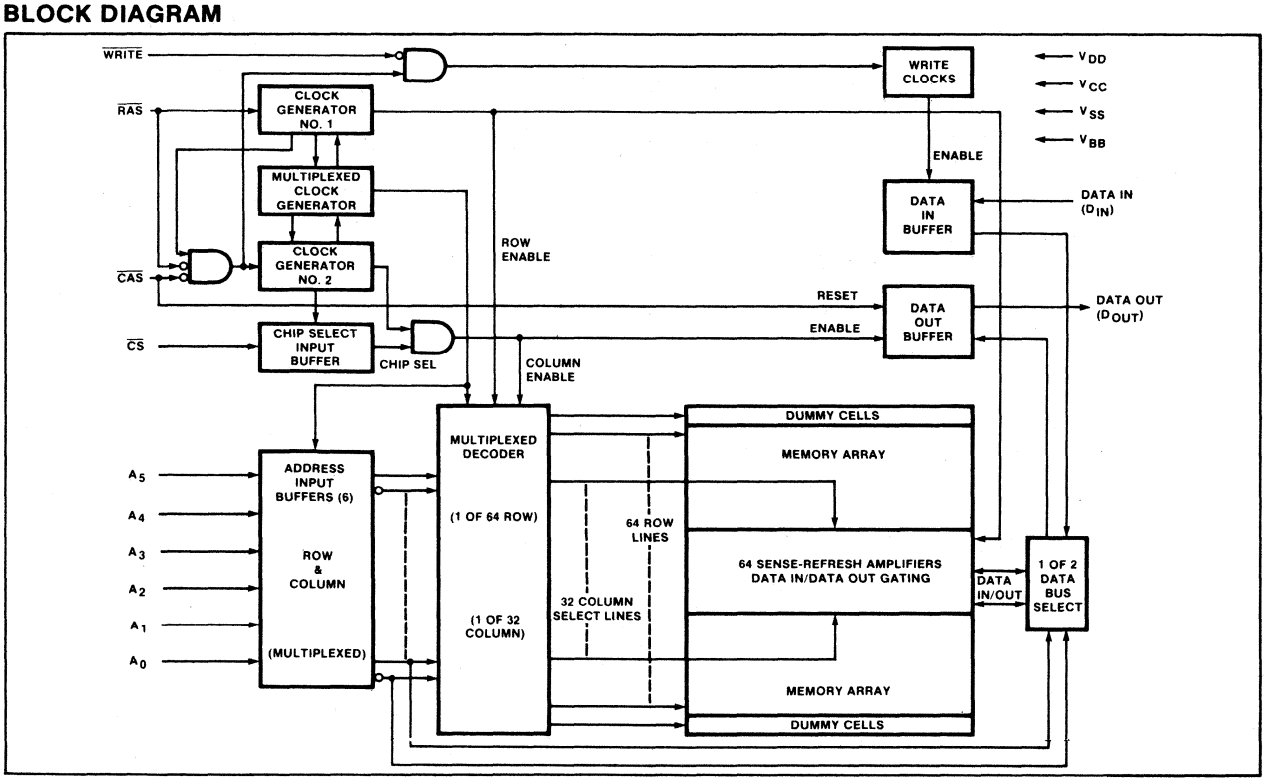
- **All inputs including clock TTL compatible**
- **On chip latches for address, chip select and data in**
- **3-state TTL compatible output**
- **Output data is latched and valid into next cycle**
- **Access time:**
  - **4027-2: 150ns**
  - **4027-3: 200ns**
  - **4027-4: 250ns**
- **Read and write cycle time:**
  - **4027-2: 320ns**
  - **4027-3: 375ns**
  - **4027-4: 375ns**
- **Low power:**
  - **Operating: 462mW**
  - **Standby: 27mW**
- **RAS only refresh (no dummy cycles required)**
- **Page mode addressing**
- **±10% power supply margins**

PIN CONFIGURATION

F,I,N PACKAGE



BLOCK DIAGRAM

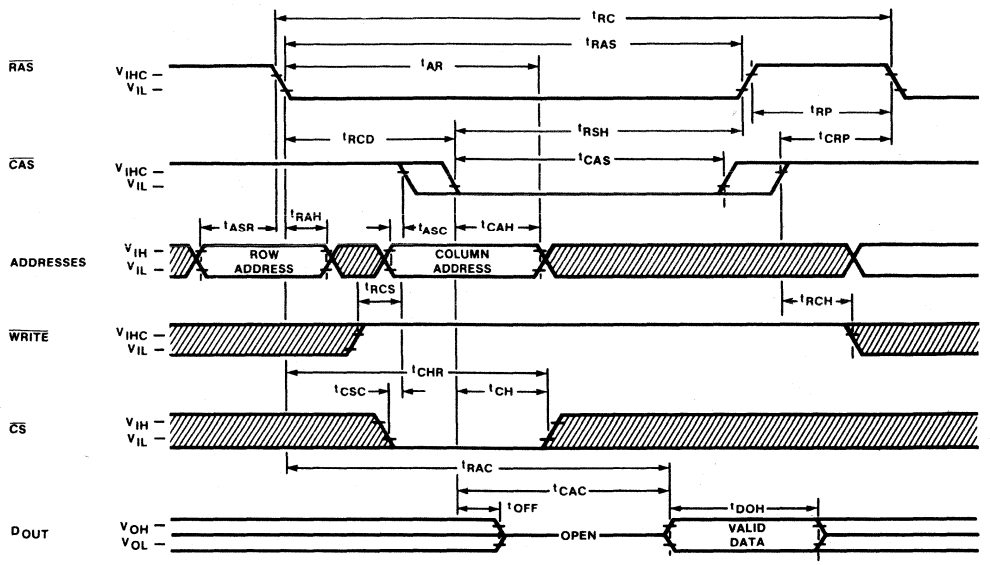


AC CHARACTERISTICS [3,11,12] T_A = 0°C to +70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V unless otherwise specified.

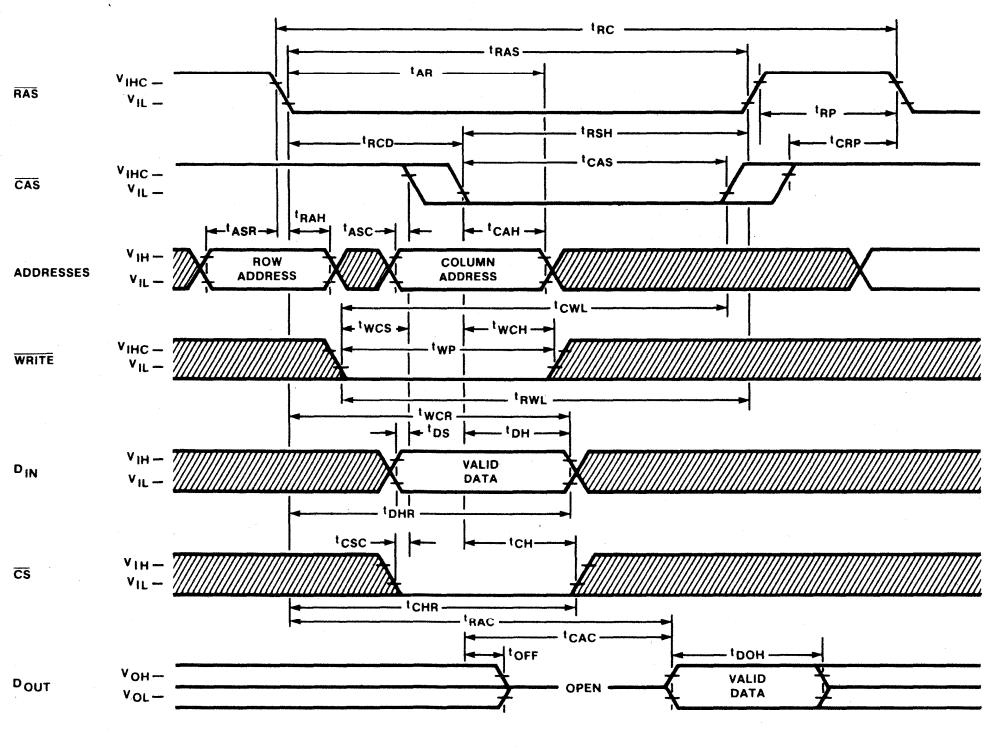
SYMBOL	PARAMETER	TEST CONDITIONS	4027-2		4027-3		4027-4		UNIT
			Min	Max	Min	Max	Min	Max	
	READ OR WRITE (EARLY) CYCLE								
t_{REF}	Refresh			2		2		2	ms
t_T[12]	Transition		3	35	3	50	3	50	ns
t_{RC}[17]	Random cycle		320		375		375		ns
t_{RAS}	$\overline{RAS}$ duration		150	10000	200	10000	250	10000	ns
t_{RP}	$\overline{RAS}$ precharge		100		120		120		ns
t_{RCD}[16]	Strobe delay		20	50	25	65	35	85	ns
t_{CAS}	$\overline{CAS}$ duration		100		135		165		ns
t_{CRP}	$\overline{CAS}$ precharge		0		0		0		ns
t_{RSH}	$\overline{RAS}$ hold		100		135		165		ns
t_{ASR}	Row address set up		0		0		0		ns
t_{RAH}	Row address hold		20		25		35		ns
t_{ASC}	Column address set up		−10		−10		−10		ns
t_{CSC}	Chip select address set up		−10		−10		−10		ns
t_{CAH}	Column address hold		45		55		75		ns
t_{CH}	Chip select hold		45		55		75		ns
t_{AR}	Address hold		95		120		160		ns
t_{CHR}	Chip select to $\overline{RAS}$ hold		95		120		160		ns
t_{OFF}	Output turn off delay		0	40	0	50	0	60	ns
t_{RAC}[14,15]	Row access			150		200		250	ns
t_{CAC}[13,14]	Column access			100		135		165	ns
t_{DOH}	Data out hold			10		10		10	μs
	READ CYCLE								
t_{RCS}	Read set up		0		0		0		ns
t_{RCH}	Read hold		0		0		0		ns
	WRITE (EARLY) CYCLE								
t_{WCS}	Write set up		0		0		0		ns
t_{WCH}	Write hold		45		55		75		ns
t_{WP}	Write duration		45		55		75		ns
t_{RWL}	Write to $\overline{RAS}$ lead		50		70		85		ns
t_{CWL}	Write to $\overline{CAS}$ lead		50		70		85		ns
t_{WCR}	Write to $\overline{RAS}$ hold		95		120		160		ns
t_{DS}[18]	Data set up		0		0		0		ns
t_{DH}[18]	Data hold		45		55		75		ns
t_{DHR}	Data to $\overline{RAS}$ hold		95		120		160		ns

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE

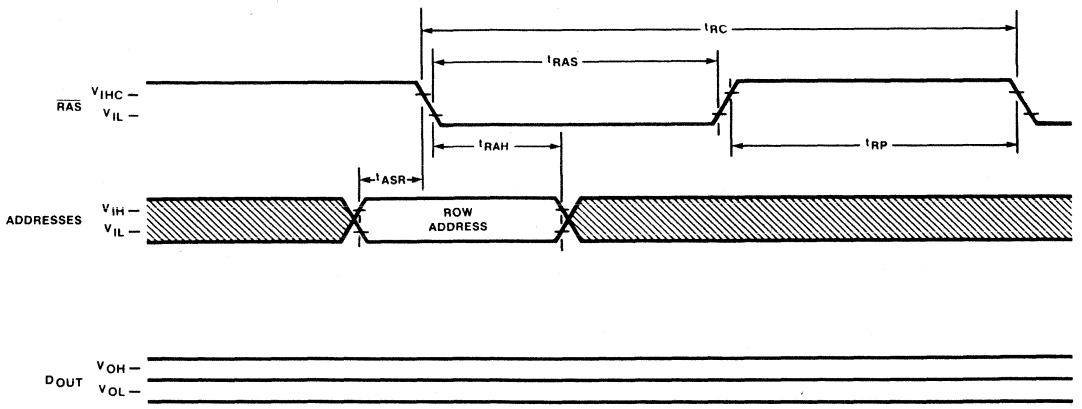


AC CHARACTERISTICS [3,11,12] T_A = 0°C to +70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	4027-2		4027-3		4027-4		UNIT
			Min	Max	Min	Max	Min	Max	
	$\overline{RAS}$ ONLY REFRESH CYCLE								
t_{REF}	Refresh			2		2		2	ms
t_T[12]	Transition		3	35	3	50	3	50	ns
t_{RC}[17]	Random cycle		320		375		375		ns
t_{RAS}	$\overline{RAS}$ duration		150	10000	200	10000	250	10000	ns
t_{RP}	$\overline{RAS}$ precharge		100		120		120		ns
t_{ASR}	Row address set up		0		0		0		ns
t_{RAH}	Row address hold		20		25		35		ns
	READ/WRITE OR READ/MODIFY/WRITE								
t_{REF}	Refresh			2		2		2	ms
t_T[12]	Transition		3	35	3	50	3	50	ns
t_{RWC}[17,20]	Read/write cycle		330		420		480		ns
t_{RMW}[17,20]	Read/modify/write cycle		380		470		530		ns
t_{RRAS}	R/W $\overline{RAS}$ duration		215	10000	300	10000	380	10000	ns
t_{MRAS}	RMW $\overline{RAS}$ duration		265	10000	350	10000	430	10000	ns
t_{RP}	$\overline{RAS}$ precharge		100		120		150		ns
t_{RCD}[16]	Strobe delay		20	50	25	65	35	85	ns
t_{RCAS}	R/W $\overline{CAS}$ duration		165		235		295		ns
t_{MCAS}	RMW $\overline{CAS}$ duration		215		285		345		ns
t_{CRP}	$\overline{CAS}$ precharge		0		0		0		ns
t_{RSH}	$\overline{RAS}$ hold		100		135		165		ns
t_{ASR}	Row address set up		0		0		0		ns
t_{RAH}	Row address hold		20		25		35		ns
t_{ASC}	Column address set up		−10		−10		−10		ns
t_{CSC}	Chip select set up		−10		−10		−10		ns
t_{CAH}	Column address hold		45		55		75		ns
t_{CH}	Chip select hold		45		55		75		ns
t_{AR}	Address hold		95		120		160		ns
t_{CHR}	Chip select to $\overline{RAS}$ hold		95		120		160		ns
t_{RCS}	Read set up		0		0		0		ns
t_{RWD}[19]	$\overline{RAS}$ to write delay		110		145		175		ns
t_{CWD}[19]	$\overline{CAS}$ to write delay		60		80		90		ns
t_{RWL}	Write to $\overline{RAS}$ lead		50		70		85		ns
t_{CWL}	Write to $\overline{CAS}$ lead		50		70		85		ns
t_{WP}	Write duration		45		55		75		ns
t_{MOD}	Modify		0	9735	0	9650	0	9570	ns
t_{DS}	Data set up		0		0		0		ns
t_{DH}	Data hold		45		55		75		ns
t_{OFF}	Output turn off delay		0	40	0	50	0	60	ns
t_{RAC}[14,15]	Row access		150		200		250		ns
t_{CAC}[13,14]	Column access		100		135		165		ns
t_{DOH}	Data out hold			10		10		10	μs

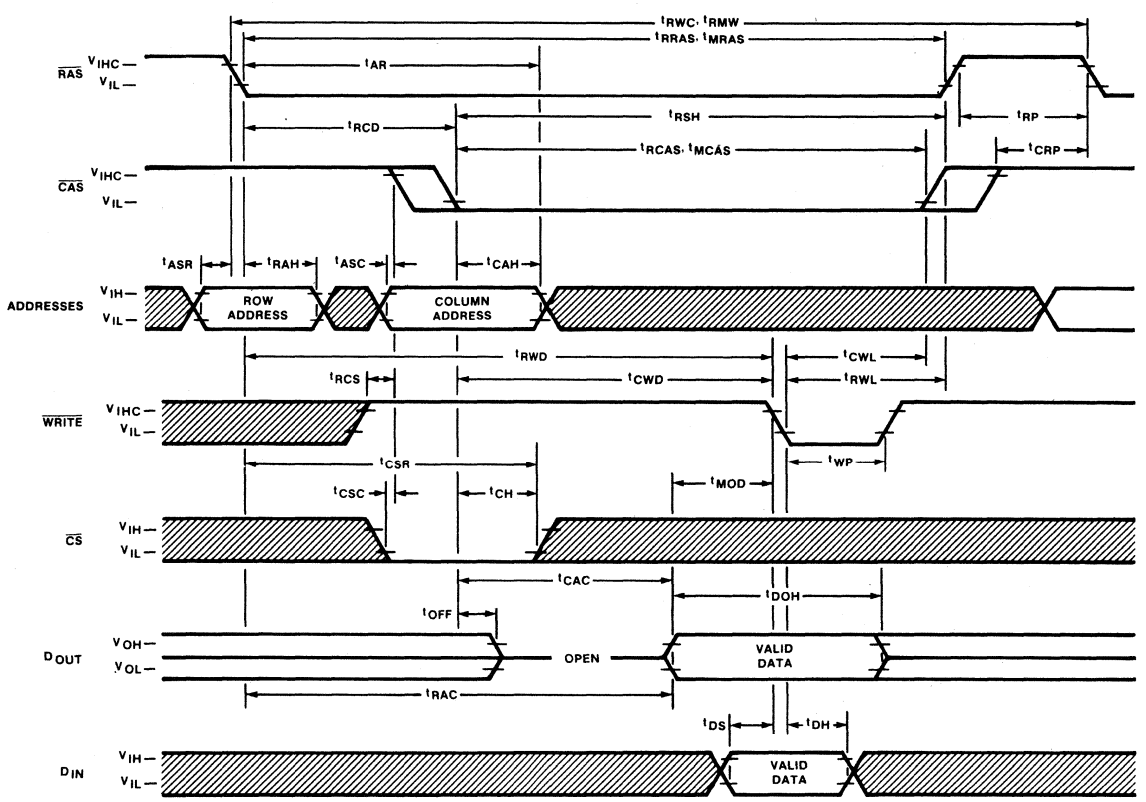
TIMING DIAGRAMS (Cont'd)

"$\overline{RAS}$ ONLY" REFRESH CYCLE



DOUT remains unchanged from previous cycle.

READ/WRITE, READ/MODIFY WRITE CYCLE

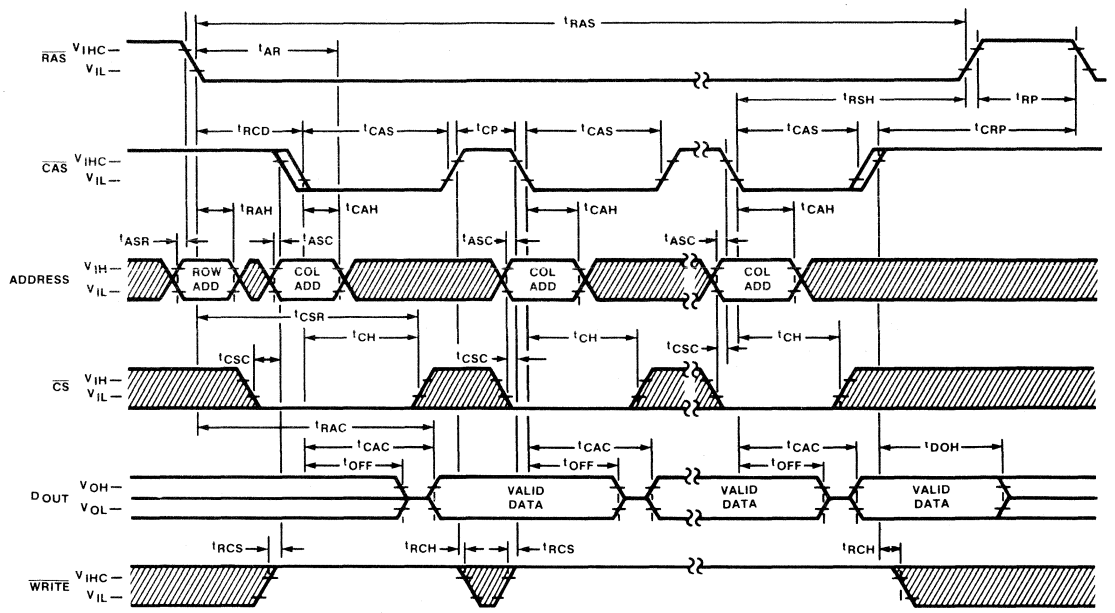


AC CHARACTERISTICS [3,11,12] T_A = 0°C to +70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = OV unless otherwise specified.

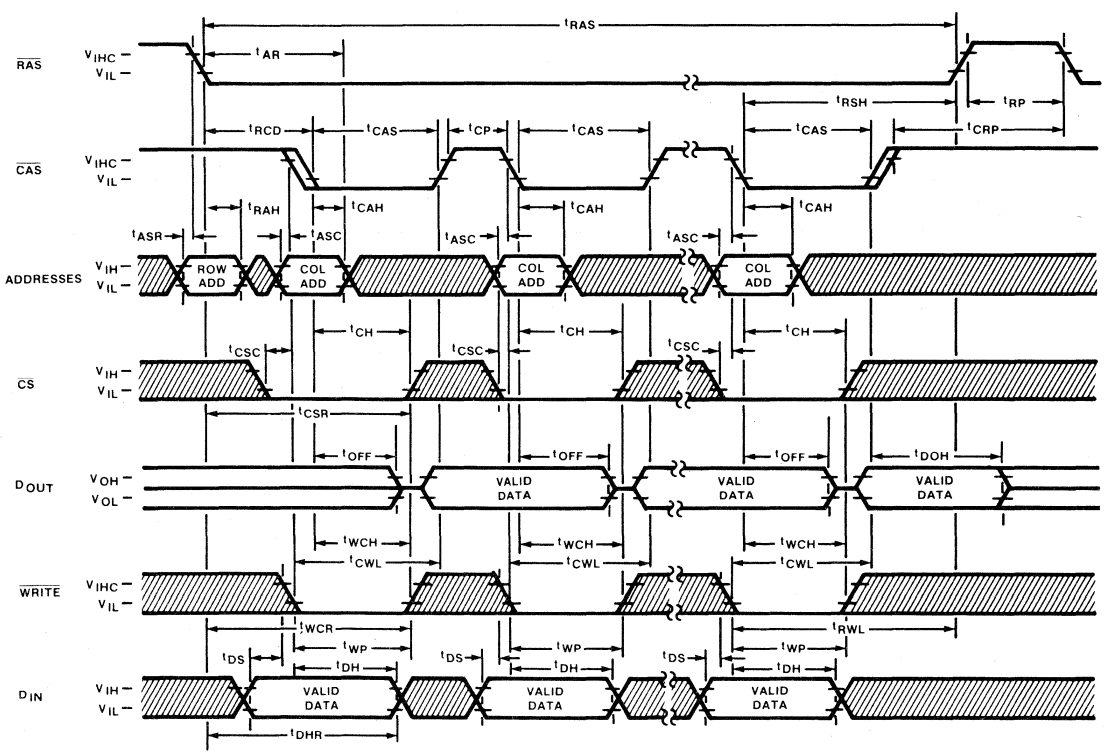
SYMBOL	PARAMETER	TEST CONDITIONS	4027-2		4027-3		4027-4		UNIT
			Min	Max	Min	Max	Min	Max	
	PAGE MODE CYCLES								
t_{REF}	Refresh			2		2		2	ms
t_T[12]	Transition		3	35	3	50	3	50	ns
t_{RAS}	$\overline{RAS}$ duration		150	10000	200	10000	250	10000	ns
t_{RP}	$\overline{RAS}$ precharge		100		120		150		ns
t_{RCD}[16]	Strobe delay		20	50	25	65	35	85	ns
t_{CAS}	$\overline{CAS}$ duration		100		135		165		ns
t_{CP}	$\overline{CAS}$ HIGH duration		60		80		110		ns
t_{PC}	Page mode cycle		170		225		275		ns
t_{RSH}	$\overline{RAS}$ hold		100		135		165		ns
t_{CRP}	$\overline{CAS}$ precharge		0		0		0		ns
t_{ASR}	Row address set up		0		0		0		ns
t_{RAH}	Row address hold		20		25		35		ns
t_{ASC}	Column address set up		−10		−10		−10		ns
t_{CSC}	Chip select set up		−10		−10		−10		ns
t_{CAH}	Column address hold		45		55		75		ns
t_{CH}	Chip select hold		45		55		75		ns
t_{AR}	Address hold		95		120		160		ns
t_{CSR}	Chip select to $\overline{RAS}$ hold		95		120		160		ns
	PAGE MODE READ CYCLE								
t_{RCS}	Read set up		0		0		0		ns
t_{RCH}	Read hold		0		0		0		ns
t_{OFF}	Output turn off delay		0	40	0	50	0	60	ns
t_{RAC}[14,15]	Row access		150		200		250		ns
t_{CAC}[13,14]	Column access		100		135		165		ns
t_{DOH}	Data out hold			10		10		10	μs
	PAGE MODE WRITE CYCLE								
t_{WCH}	Write hold		45		55		75		ns
t_{WP}	Write duration		45		55		75		ns
t_{CWL}	Write lead		50		70		85		ns
t_{RWL}	Write to $\overline{RAS}$ lead		50		70		85		ns
t_{WCR}	Write to $\overline{RAS}$ hold		95		120		160		ns
t_{DS}	Data set up		0		0		0		ns
t_{DH}	Data hold		45		55		75		ns
t_{DHR}	Data to $\overline{RAS}$ hold		95		120		160		ns

TIMING DIAGRAMS (Cont'd)

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_{STG}	Storage	-55 to 150	
	All input or output voltages with respect to the most negative supply voltage V_{BB}	+20 to -.5	V
	Supply voltage V_{DD}, V_{CC} and V_{SS} with respect to V_{BB}	+20 to -1	V
	$V_{BB} - V_{SS}$ with $V_{DD} - V_{SS} > 0$	0	V

DC ELECTRICAL CHARACTERISTICS[2,3] T_A = 0°C to 70°C, V_{DD} + 12V ± 10%, V_{CC}[4] = 5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage	Any input				V
V_{IL}	Low		-1.0		0.8	
V_{IH}	High		2.4		7.0	
	Output voltage					V
V_{OL}	Low	I_{OL} = 3.2mA	0.0		0.4	
V_{OH}	High	I_{OH} = -5.0mA	2.4		V_{CC}	
	Leakage current	Any input				µA
I_{IL}	Input[5]				10	
I_{OL}	Output[6,7]				10	
	V_{DD} current					mA
I_{DD1}	Average[8]				35	
I_{DD2}	Standby[6]	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}		1	2	
I_{DD3}	Average	$\overline{RAS}$ only cycles			25	
I_{CC}	V_{CC} supply current[9]					mA
I_{BB}	Average V_{BB} current				150	µA
	Capacitance					pF
C_{AD}	Address, D_{IN}, $\overline{CS}$[10]				5	
C_C	$\overline{CAS}$, $\overline{RAS}$,[10] $\overline{WRITE}$				10	
C_{OUT}	Output[6,10]				7	

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages referenced to V_{SS}.
3. Several cycles are required after power up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
4. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
5. All device pins at 0 volts except V_{BB} which is at -5 volts and the pin under test which is at +10 volts.
6. Output is disabled (high impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilizations is required prior to measurement of this parameter.
7. $0V \leq V_{OUT} \leq +10V$.
8. Current is proportioned to cycle rate, I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min). See Figure 1 for I_{DD1} limits at other cycle rates.
9. I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to Data Out. At all other times I_{CC} consists of leakage currents only.
10. Effective capacitance is calculated from the equation: $C = \frac{\Delta Q}{\Delta v}$ with Δv = 3 volts.
11. A.C. measurements assume t_T = 5ns.
12. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
13. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
14. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
15. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
16. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
17. The specifications for t_{RC} (min), t_{RWC} (min), and t_{RMW} (max) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
18. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read/modify write cycles.
19. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read/write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.
20. For t_{RWC} (min), t_{MOD} is -40ns. For t_{RMW} (min), t_{MOD} time available is at least +10ns. There is no restriciton on t_{RMW} (min) but t_{MOD} time available is naturally then affected. For $t_{RMW} < t_{RMW}$ (min) +10ns, cycle then becomes t_{RWC} where $t_{MOD} <$ 0ns.

2600-F,I,N • 2600-1 - F,I,N

DESCRIPTION

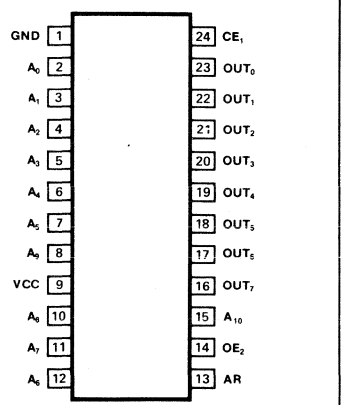
The 2600 outputs appear and remain in a steady state condition until a new address is read. The 16,384 bits are organized as 2048 addresses with 8 output lines. Full address decoding is performed on chip. The 2600's size enhances its usage in any high density, fixed memory application such as logic function generation or microprogramming. Programming of the device is accomplished via the use of one custom mask during device fabrication.

FEATURES

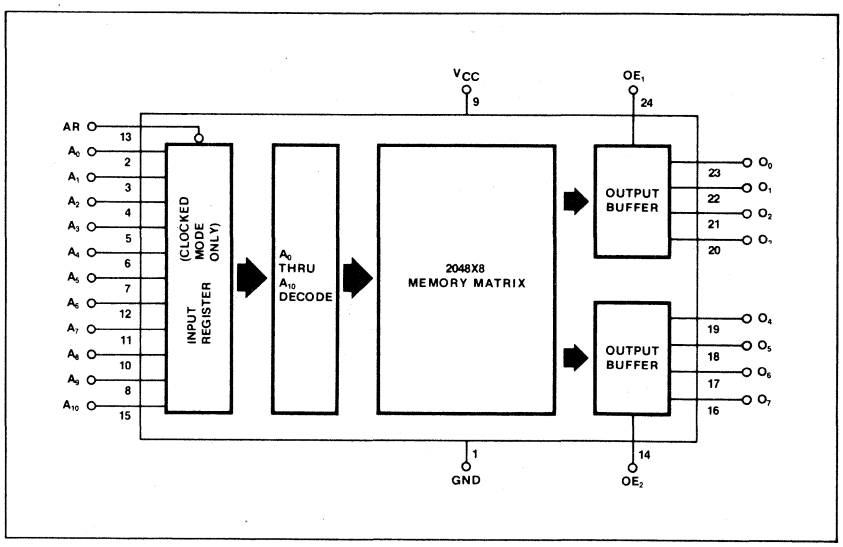
- **Completely static**
- **Utilizes MOS n-channel si-gate technology**
- **Clocked or unclocked operation**
- **Access time: 300/550ns max**
- **Single +5V power supply**
- **2 output enable controls allow:**
  Wire OR'D three-state outputs for expanded memories
  2048X8 or 4096X4 organization
- **All inputs and outputs directly TTL compatible**
- **Pin compatible with EA4600 and EA4900**

PIN CONFIGURATION

F,I,N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to +150	
P_D	Power dissipation	Hermetic 1.25	W
	Voltages on all inputs and supply pins	-0.5 to +7.0	V

ELECTRICAL DRIVE REQUIREMENTS $0°C \leq T_A \leq +70°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS[2,3]	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage	Address read, address input and output enable				V
V_{IL}	Low		-0.5		0.8	
V_{IH}	High		2.2		V_{CC}	
	Output voltage	TTL interface				V
V_{OL}	Low data	I_O = 1.6mA		0.2	0.4	
V_{OH}	High data	I_O = -100μA	2.4	3.5	V_{CC}	
I_{LI}	Input leakage current	Test pin at V = V_{CC} max, Other pins at ground			10	μA
I_{CC}	Supply current	V_{CC} = V_{CC} max 25°C		80	115	mA
	Capacitance	0V bias, f = 1MHz				pF
C_{IN}	Address input			5	7.5	
C_{AR}	AR input			5	7.5	
C_{OUT}	Output			7	10	

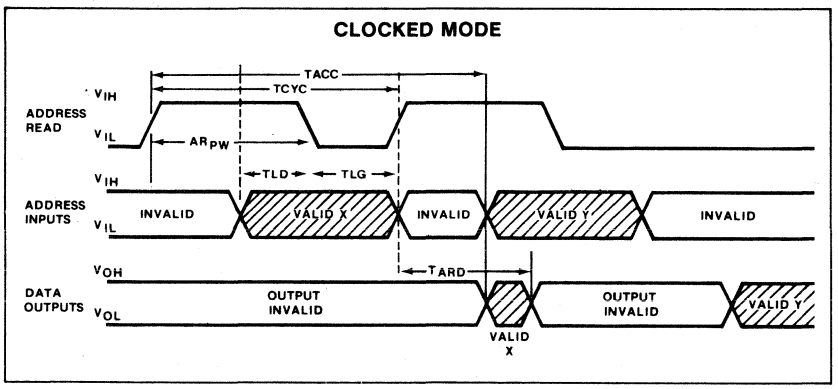
TIMING SPECIFICATIONS $0°C \leq T_A \leq +70°C$, $4.75V \leq V_{CC} \leq 5.25V$

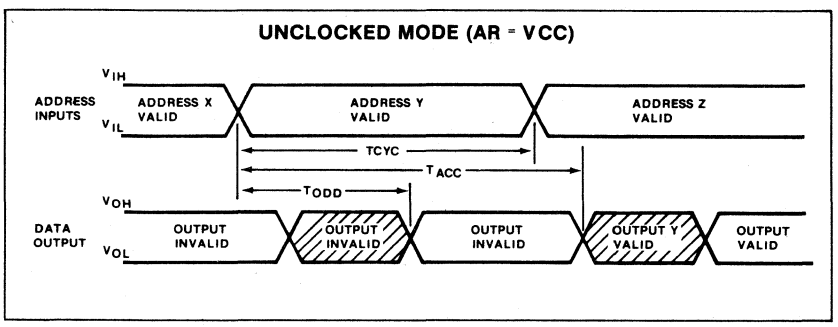
PARAMETER		TO	FROM	TEST CONDITIONS[2,3]	2600			2600-1			UNIT
					Min	Typ	Max	Min	Typ	Max	
CLOCKED MODE											
T_{CYC}	Cycle time				500			300			ns
	Pulse width										ns
AR_{PW}	Address read				300	150		100	50		
	Delay time										ns
T_{ACC}		Output	Address			450	550		200	300	
T_{ARD}		Output disturb	Address read		75	140		0	30		
T_{LD}	Address lead time				100	30		50	0		ns
T_{LG}	Address lag time				150	70		100	50		ns
UNCLOCKED MODE											
T_{CYC}	Cycle time			Standard	500			300			ns
	Delay time										ns
t_{ACC}		Output	Address			450	500		200	300	
T_{ODD}		Output disturb			0	50		0	30		
OUTPUT ENABLE (CLOCKED OR UNCLOCKED MODE)											
	Delay time										ns
T_{CO}		Output on	Output enable			100	300		(50)	150	
T_{DO}		Output off	Output enable			150	400		100	200	

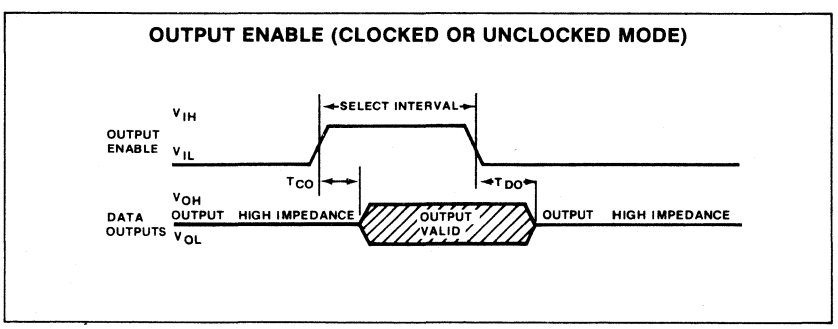
NOTES

1. Stresses more severe than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and operation of the device at any condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are referenced to V_{SS}. Positive current flows into the referenced pin.
3. Output load = 50pF plus 1 standard TTL input.

TIMING DIAGRAMS







DEFINITIONS

Clocked Mode

1. T_{CYC}, Cycle Time is the time between successive address read pulses.
2. T_{LD}, Address Lead Time is the minimum time required for the address to be valid prior to the falling edge of the AR pulse.
3. T_{LG}, Address Lag Time is the minimum amount of the time required for the address to remain valid after the falling edge of the AR pulse.
4. T_{ARD}, Address Read to Output Disturb Delay is the minimum time between the AR pulse and the first output transition when a new address is present.

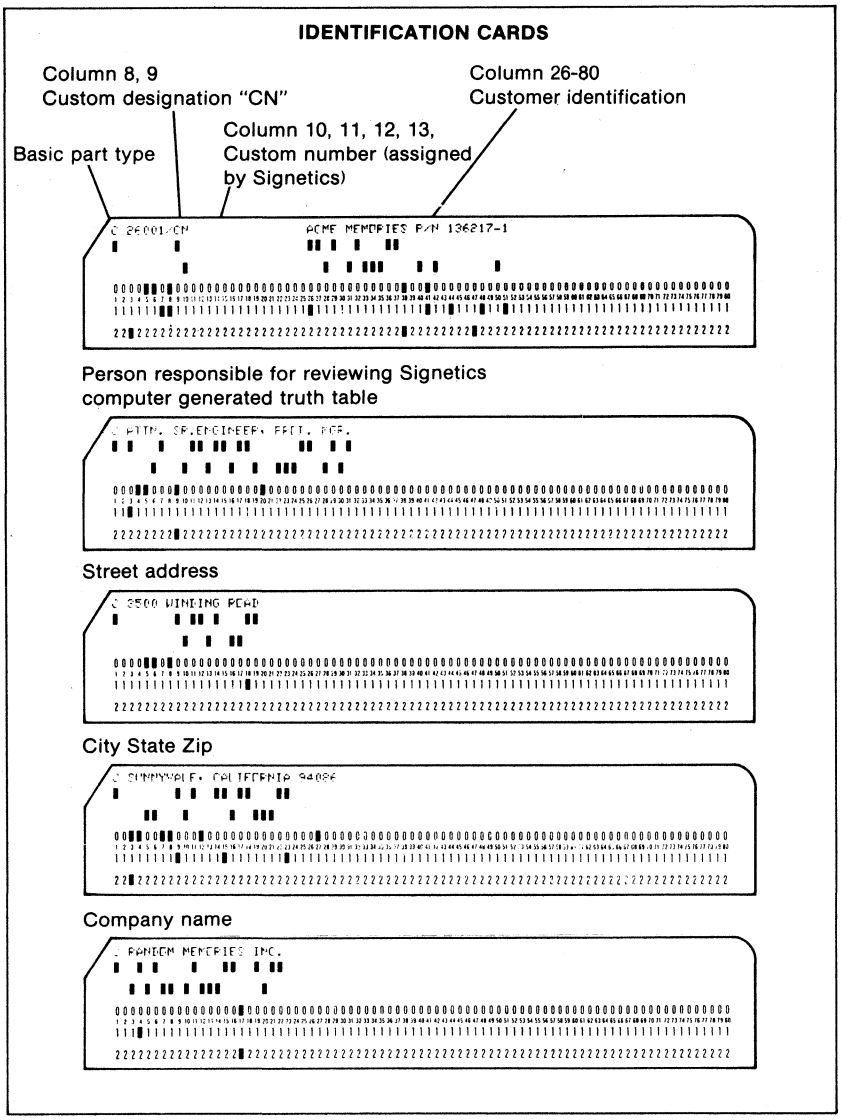
Unclocked Mode

1. T_{CYC}, Cycle Time is the time between application of successive addresses.
2. T_{ACC}, Address to Output Delay Time is the maximum time between a new valid address and the corresponding valid output.
3. T_{ODD}, Output Disturb Delay is the minimum time between the address change and the first output transition.

Output Enable

1. T_{CO}, Output Enable to Output ON Delay Time is the minimum time required for the output, in high impedance state, to become valid after rising edge of the output enable pulse.
2. T_{DO}, Output Enable to Output ON Delay Time is the minimum time required for the output to become high impedance after the falling edge of the output enable pulse.

CARD FORMAT



CUSTOM PATTERN PROGRAMMING INSTRUCTIONS

For the very large MOS ROM now produced by Signetics, a computer aided technique utilizing punched computer cards is employed. This technique requires that the customer supply Signetics with a deck of standard 80 column computer cards describing the data to be stored in the ROM array.

The required punching format is described below. All addresses must be included with their outputs defined. That is, no assumptions are made regarding the bit configuration of undefined outputs. Therefore the customer must submit cards defining the entire ROM contents, even though part or portions of the ROM may be unused (zeros).

Data Card Format for Custom ROMs

Each card is to be punched as follows. Note that for the Signetics 2600, a 3-digit octal number is used for representing the 8 ROM outputs.

Column

1-4 Punch a 4-digit octal number representing the input address for the first of the 16 output words appearing on this card. (This is the initial address)

5-7 Punch a 3-digit octal number representing the outputs for the initial input address.

8-10 Punch a 3-digit octal number representing the outputs for the initial input address +1.

11-13 Punch a 3-digit octal number representing the outputs for the initial input address +2.

50-52 Punch a 3-digit octal number representing the outputs for the initial input address +15.

69-80 The unique number assigned to this ROM pattern by Signetics must be punched in this field enclosed by blank spaces. This number can be obtained by contacting your local Signetics salesman, representative, or the marketing department at the factory directly.

Each card, therefore, carries (in octal) the initial input address for the 16 output words contained on that card, the 16 output words themselves (in octal) and the unique ROM number. The card must be provided for all possible sequential address locations (in blocks of 16). A 2048 word ROM, therefore, requires 128 cards, with all 16 output words defined on each card.

2607-F,I,N

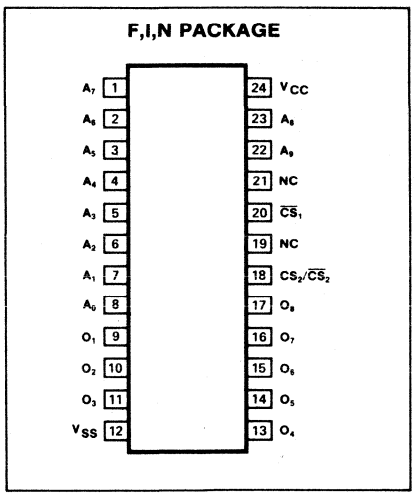
FEATURES

- Static operation—no clocks
- Access time: 450ns max
- Single 5V power supply
- TTL compatible inputs and outputs
- Power dissipation: 525mW
- Tri-state outputs
- Mask programmable chip select for easy word expansion
- N-channel silicon gate technology
- Standard 24-pin package
- Designed for system applications requiring high performance, large bit storage and simple interfacing
- 2 chip selects ($\overline{CS}1$, negative true; CS2/$\overline{CS}2$, either negative true or positive true at mask level)
- Pin for pin compatible with Intel 2708 electrically programmed erasable ROM and Intel 2308/8308 ROM, except only requiring +5V supply
- All inputs capacitive and do not sink or source current

PIN DESIGNATION

PIN NO.	FUNCTION
A_0-A_9	Address inputs
O_1-O_8	Data outputs
CS_1, CS_2	Chip select inputs
NC	No connect

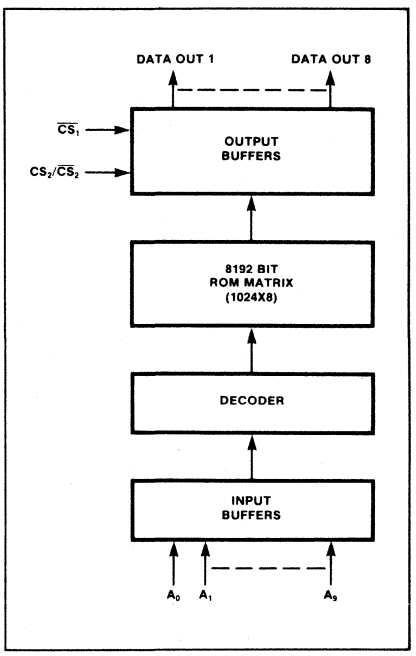
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to +150	
	All input, output, and supply voltages with respect to ground pin	-0.5 to +7	V

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{SS} = OV unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low				0.65	
V_{IH}	High		2.2		V_{CC}+1.0	
	Output voltage					V
V_{OL}	Low	I_{OL} = 2mA			0.45	
V_{OH1}	High	I_{OH} = 1mA	2.4			
I_{LI}	Input load current	V_{IN} = 0 to 5.25V			10	μA
I_{LO}	Output leakage current	Chip deselected			10	μA
I_{CC}	Supply current			80	100	mA
P_D	Power dissipation			400	525	mW
	Capacitance	T_A = 25°C, f = 1MHz, V_{CC} and all other pins tied to V_{SS}				pF
C_{IN}	Input				7.5	
C_{OUT}	Output				15	

AC ELECTRICAL CHARACTERISTICS

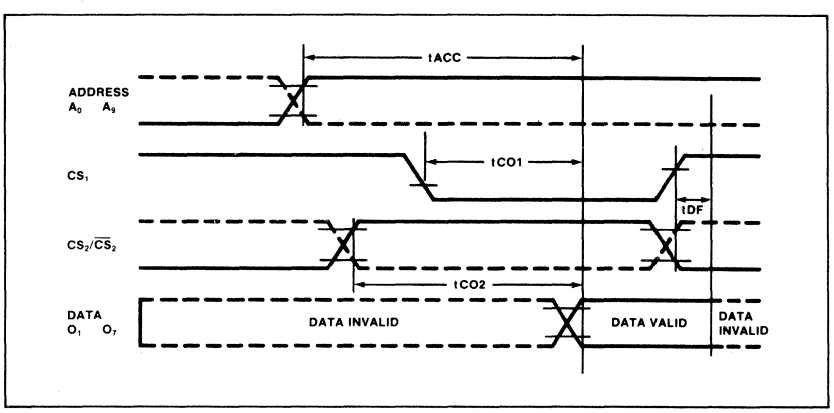
T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{SS} = OV unless otherwise specified, Output load = 1 TTL gate, Input pulse levels = .65V to 2.2V, Input pulse rise and fall times = 20ns, Timing measurement reference level: V_{IH} = 2.0V, V_{OH} = 0.8V, V_{IL} = V_{OL}

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
	Delay time						ns
t_{ACC}		Output	Address		200	450	
t_{CO1}		Output	Chip select 1		85	160	
t_{CO2}		Output	Chip select 2		85	160	
t_{DF}	Float time	Output data	Chip deselect		70	160	ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values for T_A = 25°C and typical supply voltages.

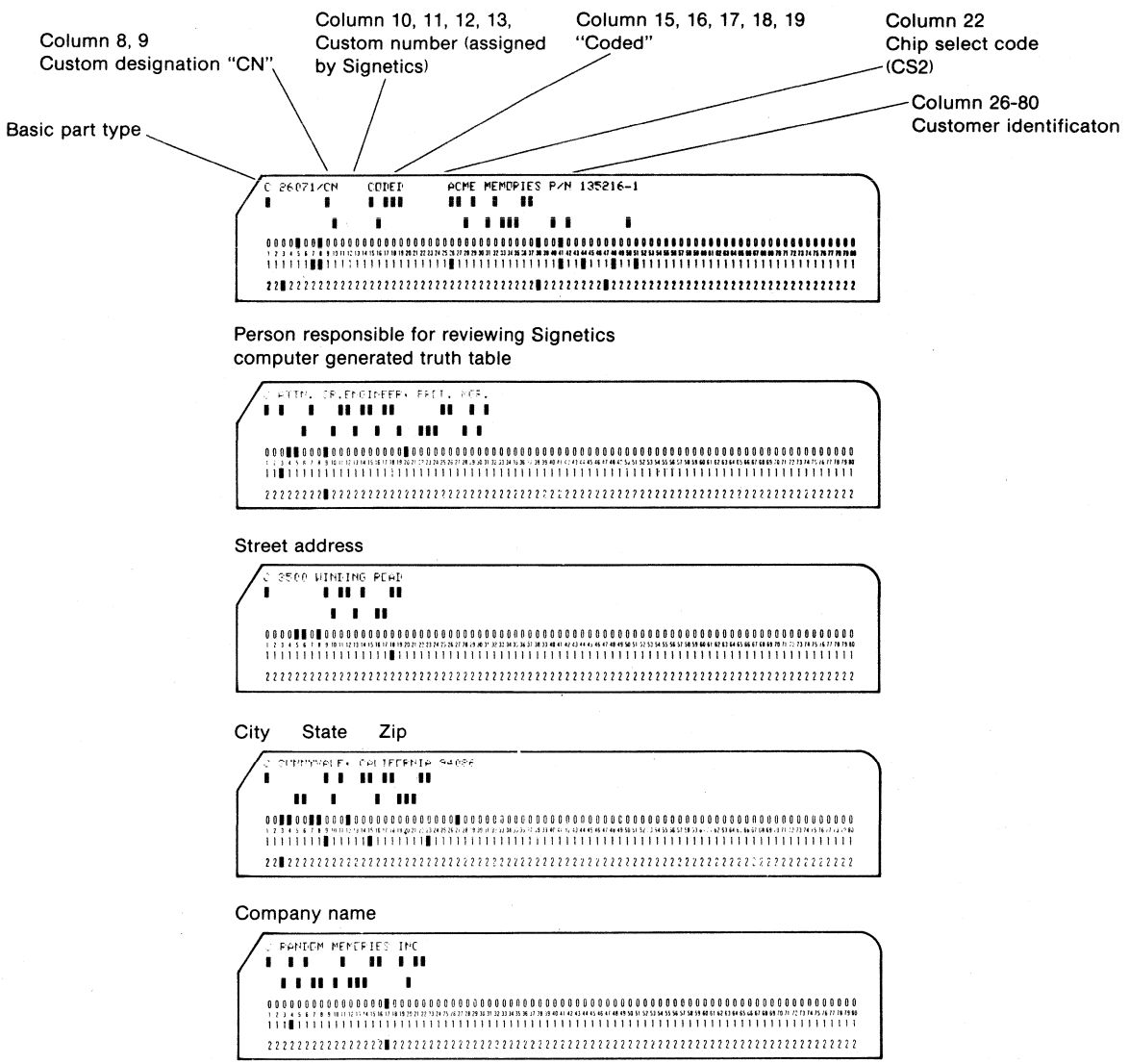
TIMING DIAGRAM



2607-F,I,N

CARD FORMAT

IDENTIFICATION CARDS



INPUT FORMAT

A. For a N words X 8-bit organization only, cards 2 and the following cards should be punched as shown. Each card specifies the 8-bit output of 8 words.

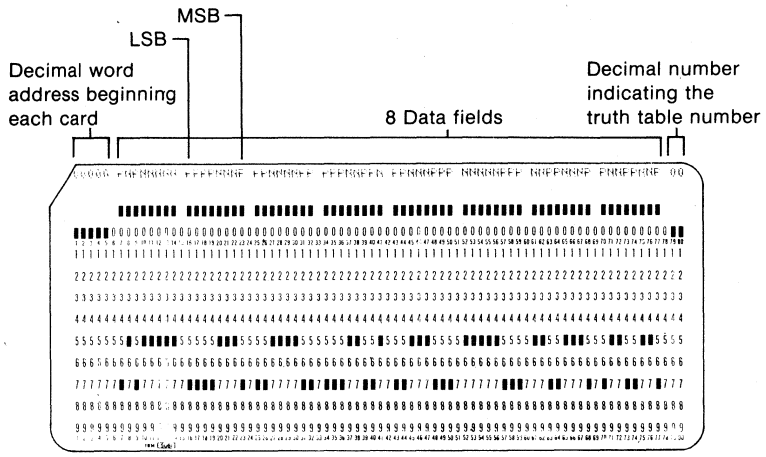
B. Paper Tape Format
The paper tapes which should be used are the:

1. 1" wide paper tape using 7 or 8-bit ASCII code, such as a model 33 ASR teletype produces:

The format requirements are as follows:

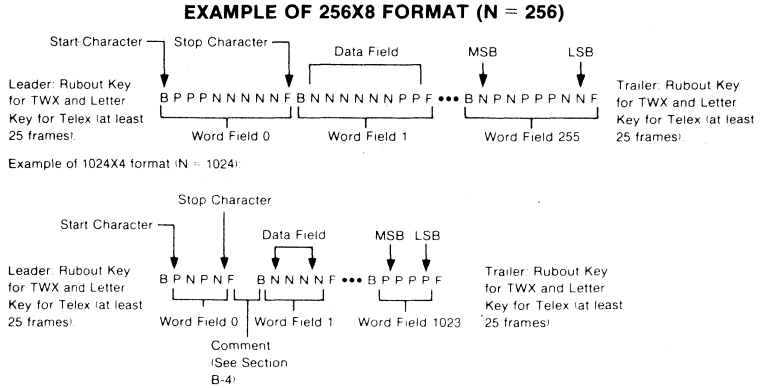
1. All word fields are to be punched in consecutive order, starting with word field 0 (all addresses low). There must be exactly N word fields for the NX8 organization.
2. Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 or 4 data characters between the B and F for the NX8 organization.

   NO OTHER CHARACTERS, SUCH AS RUBOUTS, ARE ALLOWED ANYWHERE IN A WORLD FIELD. If in preparing a tape, an error is made, the entire word field, including the B and F must be rubbed out. Within the word field, a P results in a high level output, and an N results in a low level output.
3. Preceding the first word field and following the last word field, there must be a leader/trailer length of at least 25 characters. This should consist of rubout punches (letter key for Telex tapes).
4. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every 4 word fields). When these carriage returns, etc. are inserted, the tape may be easily listed on the teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every 4 word fields.
5. Included in the tape before the leader should be the customer's complete Telex or TWX number and if more than one pattern is being transmitted, the ROM pattern number.
6. MSB and LSB are the most and least significant bit of the device outputs. Refer to the data sheet for the pin numbers.



COLUMN	DATA
1-5	Punch the 5 digit decimal equivalent of the binary coded location which begins each card. The address is right justified, i.e., 00000, 00008, 00016, etc.
6	Blank
7-14	Data field
15	Blank
16-23	Data field
24	Blank
25-32	Data field
33	Blank
34-41	Data field
42	Blank
43-50	Data field
51	Blank
52-59	Data field
60	Blank
61-68	Data field
69	Blank
70-77	Data field
78	Blank
79-80	Punch same 2 digit decimal number as in title card.

EXAMPLE OF 256X8 FORMAT (N = 256)



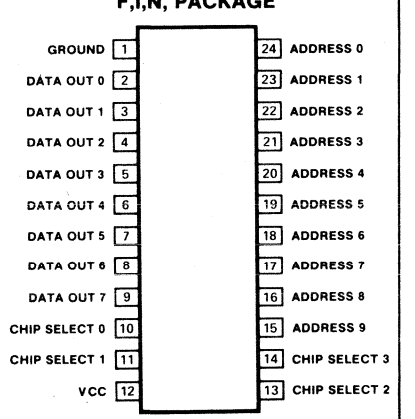
2608-F,I,N • 2608-1-F,I,N

FEATURES

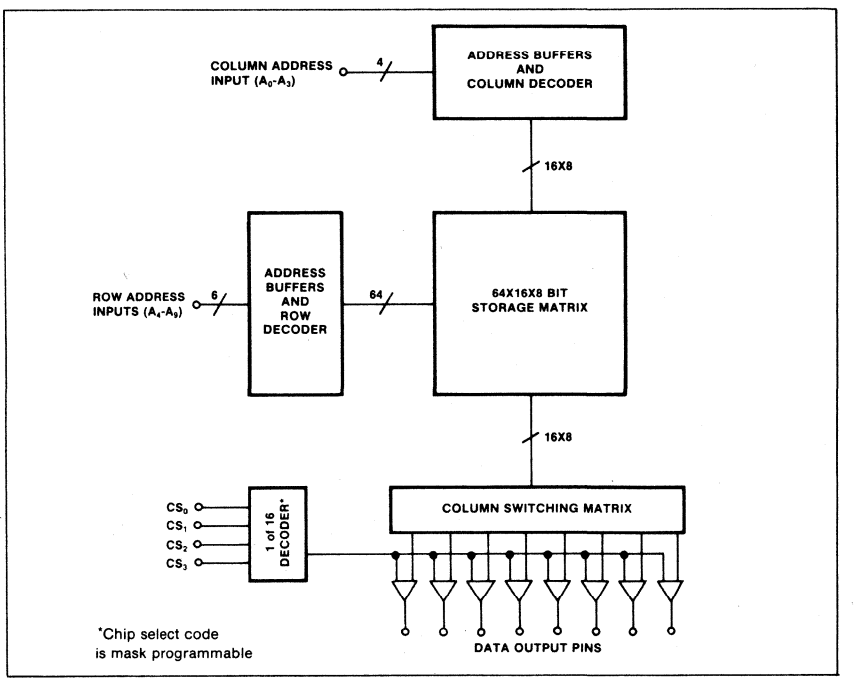
- Static operation—no clocks
- Access time:
  - 2608: 550ns
  - 2608-1: 450ns
- Single 5V power supply and ground power connections
- TTL compatible inputs and outputs
- Power dissipation: 400mW max
- Tri-state outputs
- 4 mask programmable chip selects for easy word expansion
- Low threshold n-channel silicon gate technology which allows ease of use with low voltage logic families such as transistor-transistor logic
- Standard 24-pin package
- Fully decoded

PIN CONFIGURATION

F,I,N, PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1,2]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
	All input, output and supply voltages with respect to ground pin	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$ (unless otherwise noted)[3,4,5,6,7]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low		-0.5		0.65	
V_{IH}	High		2.2			
	Output voltage					V
V_{OL}	Low	$I_{OL} = 1.6mA$			0.45	
V_{OH}	High	$I_{OH} = 100\mu A$	2.4			
I_{IN}	Input load current	$0 \le V_{IN} \le 5.25V$			10	μA
	Output leakage current	Device deselected				μA
I_{LOH}		$V_O = 2.4V$			10	
I_{LOL}		$V_O = 0.4V$			10	
I_{CC}	Supply current	$V_{CC} = 5.25V$, $T_A = 0°C$			80	mA
	Capacitance					pF
C_{IN}	Input	$V_{IN} = OV$			7.5	
C_{OUT}	Output	$V_{OUT} = OV$			15	

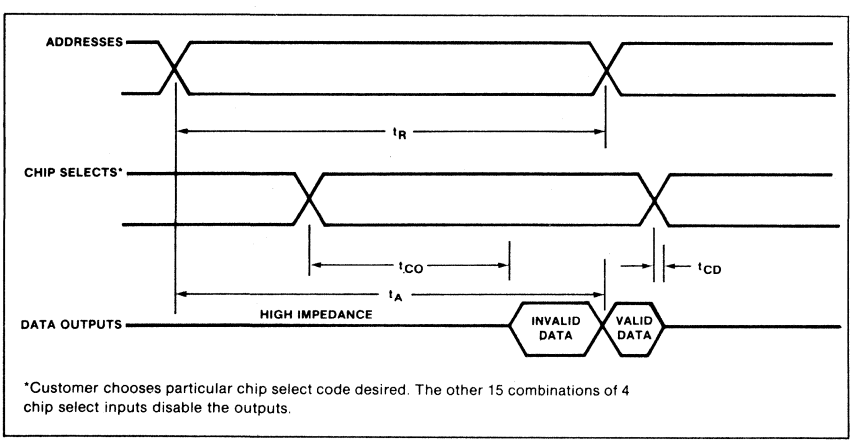
AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$[8,9,10]

PARAMETER		TO	FROM	2608			2608-1			UNIT
				Min	Typ	Max	Min	Typ	Max	
t_R	Read cycle time			550			450			ns
t_{CO}	Enable time[11]	Output	Chip select			300			300	ns
t_{CD}	Disable time[11]	Output	Chip select	10		150	10		150	ns
t_A	Access time[11]	Output	Address	100		550	100		450	ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 50° C/W junction to ambient.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameter valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process improvements.
7. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
8. Input levels swing between 0.65V and 2.2V.
9. Input signal transition times are 20ns.
10. Timing reference level is 1.5V.
11. Output load is one standard TTL load plus 130pF.

TIMING DIAGRAM



*Customer chooses particular chip select code desired. The other 15 combinations of 4 chip select inputs disable the outputs.

PIN DESCRIPTION

Addresses

These 10 TTL-compatible inputs are decoded on-chip to select one of 1024 8-bit bytes. Since the 2608 utilizes static logic throughout, a change in addresses results in a change in data as long as the chip is selected. Access time is measured from the point where the last address input became stable. Cycle time and access time are equal in a static ROM design.

Chip Selects

There are 4 TTL-compatible chip select inputs for the 2608. Only 1 combination of these 4 signals enables the chip. The other 15 disable the chip. The particular enabling combination is chosen by the customer and specified on the first punched card of the customer card deck. A positive logic convention is assumed.

Data Outputs

The 8 data outputs are push-pull buffers capable of driving one standard TTL load plus a 130pF load capacitance. These outputs are placed in the high impedance state when any one of the disabling combinations of the chip select inputs is present.

CODING FORMAT

Coding data for the 2608 may be sent to Signetics via punched cards or via a written truth table. Cards are preferred since errors are essentially eliminated.

On receipt of a card deck, Signetics will translate the card deck to a truth table using the Signetics Computer Aided Design (CAD) facility. The truth table will then be sent to the customer for final approval. On receipt of final approval, Signetics will produce masks and proceed with manufacturing.

DATA CARDS

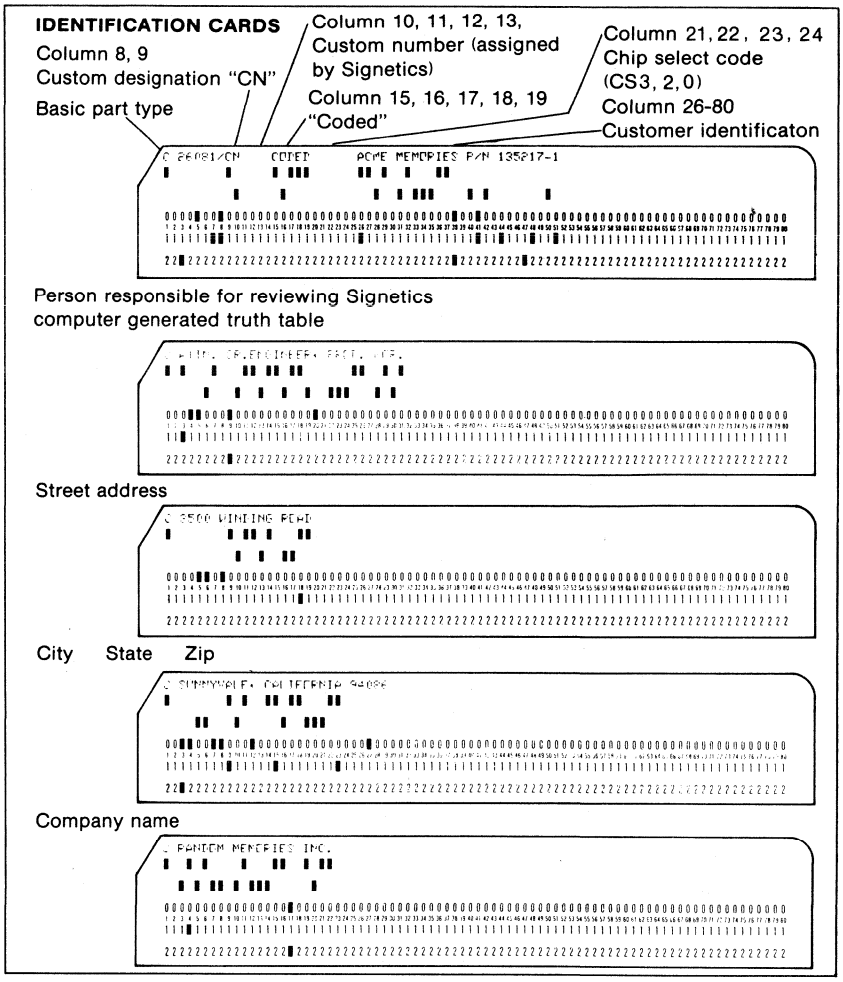
Columns

12—75	Hexadecimal data coding
77—78	Card number (starting 01)
79—80	Total number of cards (32)

Column 12 on the first card contains the hexadecimal equivalent of bits D7 thru D4 of byte 0, while column 13 contains the hexadecimal equivalent of bits D3 thru D0. Columns 14 and 15 contain byte 1, columns 16 and 17 byte 2, and so on.

The first card contains the first 32 bytes. Columns 12 and 13 on the second card will contain byte 32 (the 33rd byte). A total of 32 cards will contain 1024 bytes of 8 bit.

CARD FORMAT



BINARY TO HEXADECIMAL CONVERSION

BINARY COMBINATION D0-D3 or Dr-D7				HEXA-DECIMAL CHARACTER
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

OBJECTIVE SPECIFICATION

2609-F,I,N

DESCRIPTION

The 2609 is a mask-programmable 8192-bit row select character generator. It contains 128 characters in a 7X9 matrix, and has the capability of shifting certain characters that normally extend below the baseline, such as j, y, g, p and q. Circuitry is supplied internally to effectively lower the whole matrix for this type of character, a feature previously requiring external circuitry.

A 7-bit address code is used to select 1 of the 128 available characters. Each character is defined as a specific combination of logic "1"s and "0"s stored in a 7X9 matrix. When a specific 4-bit binary row select code is applied, a word of 7 parallel bits appears at the output. The rows can be sequentially selected, providing a 9-word sequence of 7 parallel bits per word for each character selected by the address inputs. As the row select inputs are sequentially addressed, the devices will automatically place the 7X9 character in 1 of 2 pre-programmed positions on the 16-row matrix, with the positions defined by the 4 row select inputs.

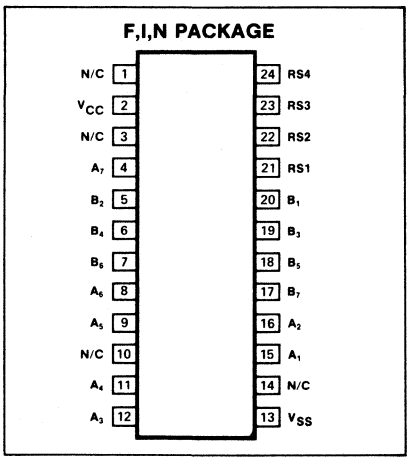
Complete TTL compatibility is provided, as well as direct interfacing with other NMOS devices, and with CMOS when using a +5V power supply. Maximum access time is 500ns; however, if a device is programmed without shifted characters, the access time is reduced.

FEATURES

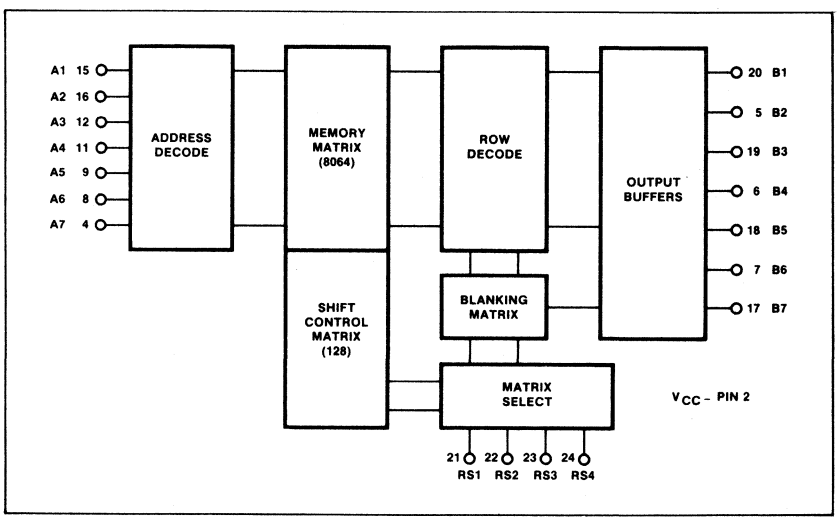
- **Static operation—no clocks**
- **Access time: 500ns max**
- **Single 5V power supply**
- **TTL compatible inputs and outputs**
- **Power dissipation: 525mW**
- **N-channel silicon gate technology**
- **Standard 24-pin package**
- **All inputs are capacitive and do not sink or source current**

PIN CONFIGURATION

F,I,N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to +150	
	All input, output and supply voltages with respect to ground pin	-0.5 to +7	V

OBJECTIVE SPECIFICATION 2609-F,I,N

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low		0		0.65	
V_{IH}	High[1]	Driven by TTL	2.2		V_{CC}	
	Output voltage					V
V_{OB}	Low (Blank)	I_{OL} = 1.6mA	0	0.4		
V_{OD}	High (Dot)	I_{OH} = -40μA	2.4			
I_{IH}	Leakage current	V_{IH} = 5.25V, V_{CC} = 4.75V			10	μA
I_{CC}	Supply current			80	100	mA
	Capacitance[2]	f = 1.0MHz, T_A = 25°C				pF
C_{IN}	Input				7.5	
C_{OUT}	Output			4.0	15	

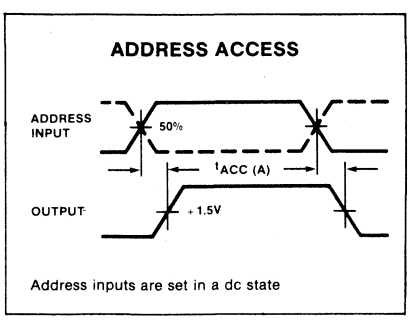
AC ELECTRICAL CHARACTERISTICS

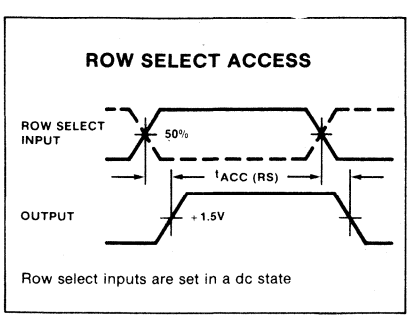
T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified,
V_{IN} levels = 0.65V and 2.2V or driven by TTL, Input t_r and t_f < 20ns,
Measurement reference level = 1.5V, Output loading = 1 TTL gate +130pF

PARAMETER		TO	FROM	LIMITS		UNIT
				Min	Max	
	Access time					ns
$t_{ACC(A)}$	Address	Output	Address		500	
$t_{ACC(RS)}$	Row select	Output	Row select		500	
$t_{ACC(S)}$	Shifted character	Output	Address		750	
P_D	Power dissipation				525	mW

NOTES
1. No pullup resistors are required.
2. Capacitances are periodically sampled rather than 100% tested.
3. This is advance information and specifications are subject to change without notice.

TIMING DIAGRAMS





MEMORY OPERATION USING POSITIVE LOGIC

(Most positive level = 1, most negative level = 0)

Address

To select 1 of the 128 characters, apply the appropriate binary code to the address inputs (A1-A7).

Row Select

To select 1 of the rows of the addressed character to appear at the 7 output lines, apply the appropriate binary code to the row select inputs (RS1-RS4).

Shifted Characters

These devices have the capability of displaying characters that descend below the bottom line (such as lower case letters j, y, g, p and q). Internal circuitry effectively drops the whole matrix for this type of character. Any character can be programmed to occupy either of the 2 positions in a 7X16 matrix.

Output

For these devices, an output dot is defined as a logic "1" level, and an output blank is defined as a logic "0" level.

MEMORY TIMING DEFINITIONS

$t_{ACC(A)}$ Address Access Time:
The time delay between a change in the address inputs and a corresponding change at the output lines with all other inputs held stable, and with the recommended load.

$t_{ACC(RS)}$ Row Select Access Time:
The time delay between a change in the row select inputs and the appearance of valid information at the output lines, with all other inputs held stable.

DISPLAY FORMAT

Figure 1 shows the relationship between the logic levels at the row select inputs and the character row at the outputs. The 2609 allows the user to locate the basic 7X9 font anywhere in 7X16 array. In addition, a shift-

ed font can be placed anywhere in the same 7X16 array. For example, the basic CN6571 font is established in rows R14-R6. All other rows are automatically blanked. The shifted font is established in rows R11-R3. Thus, while any one character is contained in a 7X9 array, the CN6571 requires a 7X12 array on the CRT screen to contain both normal and descending characters. Other uses of the shift option may require as much as the full 7X16 array, or as little as the basic 7X9 array.

The 2609 can be programmed to be scanned either from bottom to top or from top to bottom. This is achieved through the option of assigning row numbers in ascending or descending count, as long as both the basic font and the shifted font are the same. For example, an up counter will scan the CN6571 from bottom to top.

CUSTOM PROGRAMMING FOR 2609

By programming of a single photomask, the customer may specify the content of this memory. Encoding of the photomask is done with the aid of a computer. Use of the computer provides a quick and efficient way to implement a custom bit pattern, while reducing the cost of implementation.

Information on the general options of the 2609 should be submitted on an Organizational Data Form.

Programming of the memory content should be transmitted to Signetics as completed data encoding sheets. The Data Encoding Sheet Format illustration details the requirements for proper completion of the data encoding sheets.

Three examples are shown to indicate proper character encoding. The following rules apply:

1. Enter the character number in the space provided above each dot matrix. Address 0000000 is used for character number 1, with other character numbers following in the normal binary progression.
2. Indicate the rows to be used in the space provided to the left of each dot matrix. Note that characters may be positioned in either of two 7X9 locations on a 7X16 matrix; however, only 2 positions are allowed per mask option. The character for a given address may occupy only 1 of these positions
3. Column zero is added to the dot matrix on the format sheet for use in indicating shifted characters. If a character is to be shifted, a dot should be entered into the first row of the first (zero) column (see the third example, j).
4. The desired character should be entered in the matrix, using only columns B1-B7.

FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
SIGNETICS 2609 MOS ROM

Customer _____

Customer part no. _____ Rev. _____

Row number for top row of non-shifted characters _____

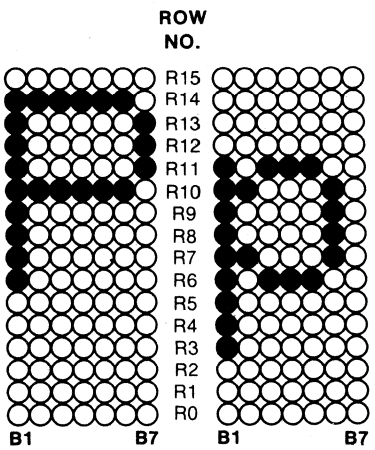
Row number for top row of shifted characters _____

Count down Count up

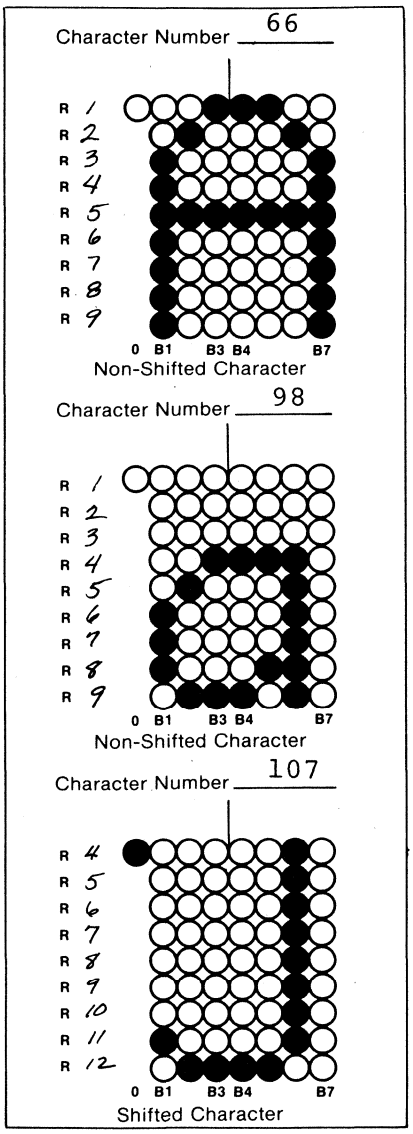
ROW SELECT INPUT CODE AND SAMPLE CHARACTERS FOR CN6571

TRUTH TABLE

RS4	RS3	RS2	RS1	OUTPUT
0	0	0	0	R0
0	0	0	1	R1
0	0	1	0	R2
0	0	1	1	R3
0	1	0	0	R4
0	1	0	1	R5
0	1	1	0	R6
0	1	1	1	R7
1	0	0	0	R8
1	0	0	1	R9
1	0	1	0	R10
1	0	1	1	R11
1	1	0	0	R12
1	1	0	1	R13
1	1	1	0	R14
1	1	1	1	R15



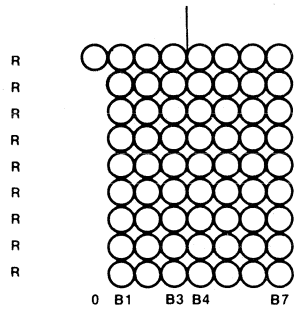
DATA ENCODING SHEET FORMAT



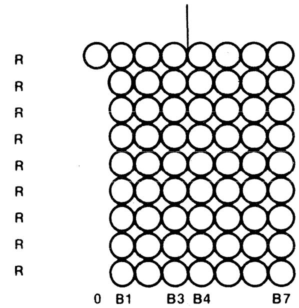
DATA ENCODING SHEET FOR 2609

Customer ______________ Customer Part No. ______________ Rev. ______ Page ______ of ______ Pages

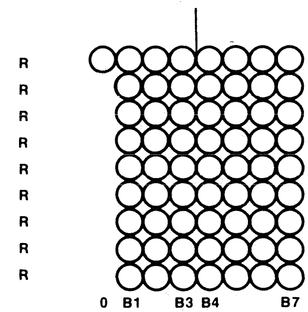
Character Number ________



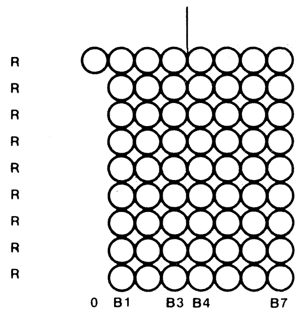
Character Number ________



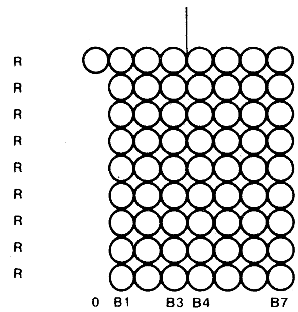
Character Number ________



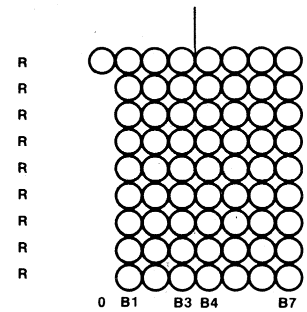
Character Number ________



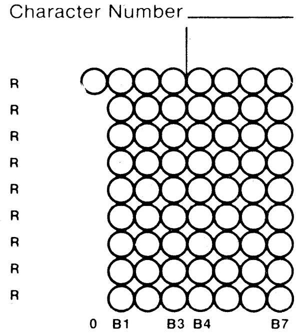
Character Number ________



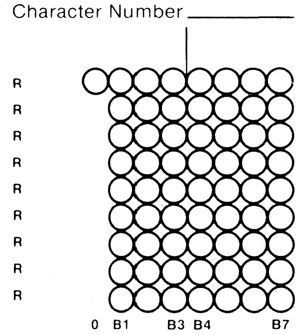
Character Number ________



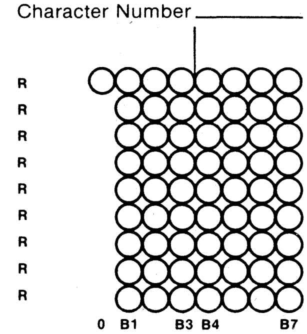
Character Number ________



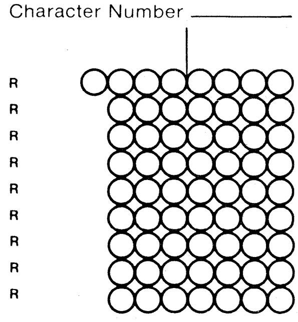
Character Number ________



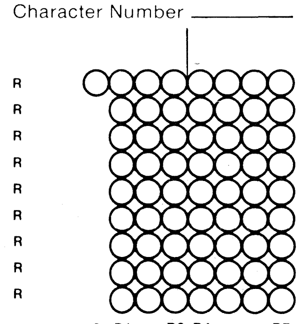
Character Number ________



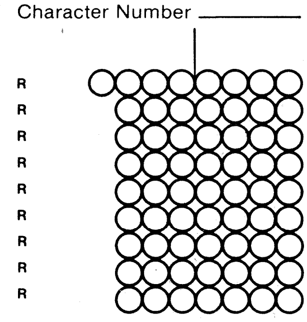
Character Number ________



Character Number ________



Character Number ________



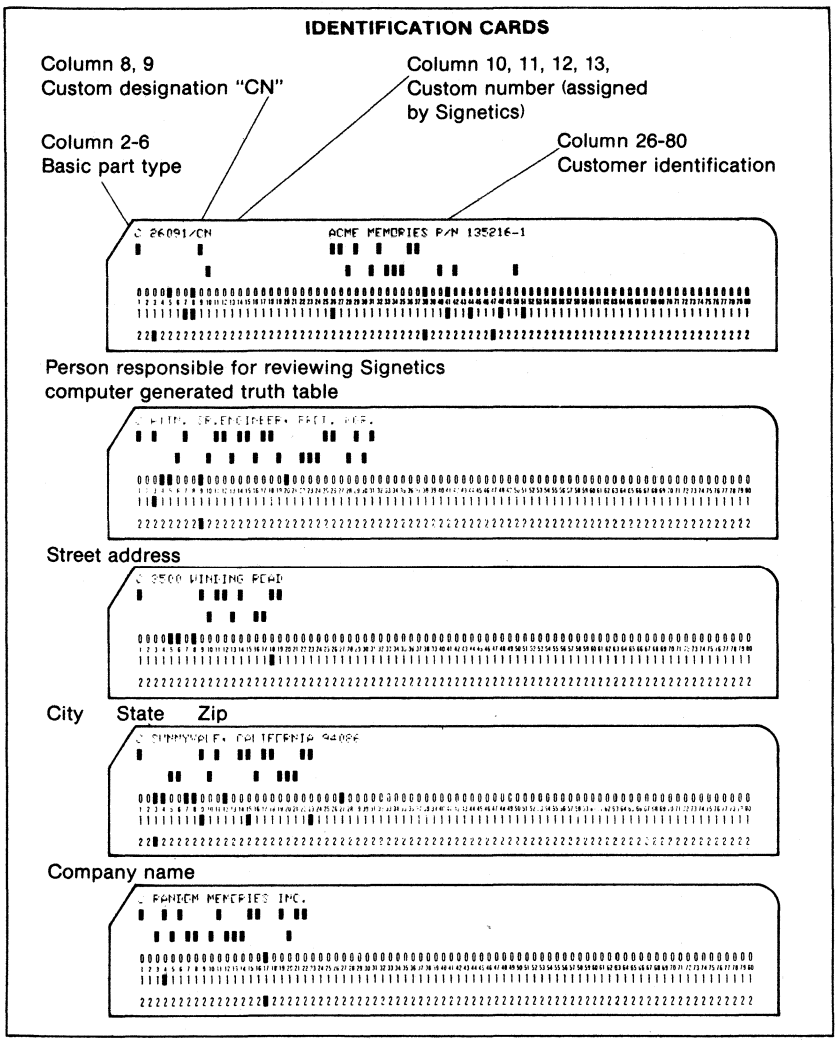
USASCII CHARACTER GENERATOR CODE

The CN6571 has been programmed with the characters shown. No attempt has been made on this figure to indicate columns and rows actually used on the display for each character.

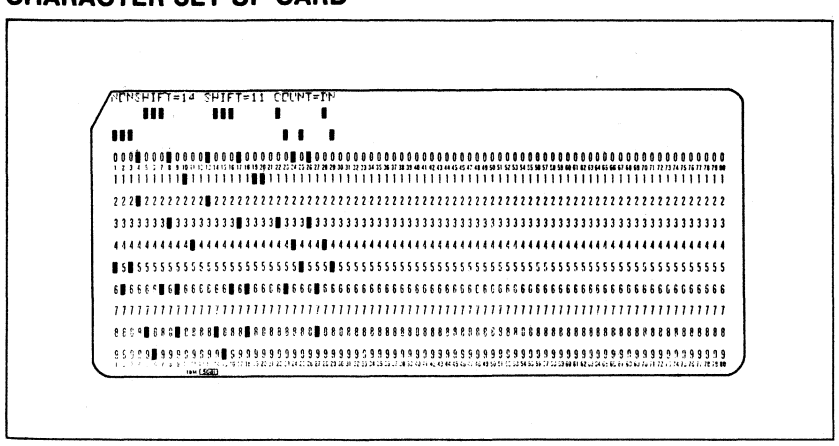
ADDRESS (A)							DISPLAYED CHARACTER	SHIFTED
7	6	5	4	3	2	1		
0	0	0	0	0	0	0	α	
0	0	0	0	0	0	1	β	yes
0	0	0	0	0	1	0	γ	yes
0	0	0	0	0	1	1	δ	
0	0	0	0	1	0	0	ε	
0	0	0	0	1	0	1	ζ	
0	0	0	0	1	1	0	η	yes
0	0	0	0	1	1	1	θ	
0	0	0	1	0	0	0	ι	
0	0	0	1	0	0	1	κ	
0	0	0	1	0	1	0	λ	
0	0	0	1	0	1	1	μ	yes
0	0	0	1	1	0	0	ν	
0	0	0	1	1	0	1	ξ	
0	0	0	1	1	1	0	ο	
0	0	0	1	1	1	1	π	
0	0	1	0	0	0	0	ρ	yes
0	0	1	0	0	0	1	σ	
0	0	1	0	0	1	0	τ	
0	0	1	0	0	1	1	υ	
0	0	1	0	1	0	0	φ	
0	0	1	0	1	0	1	χ	
0	0	1	0	1	1	0	ψ	yes
0	0	1	0	1	1	1	ω	
0	0	1	1	0	0	0	Ω	
0	0	1	1	0	0	1	√	
0	0	1	1	0	1	0	¯	
0	0	1	1	0	1	1	←	
0	0	1	1	1	0	0	!	
0	0	1	1	1	0	1	÷	
0	0	1	1	1	1	0	Σ	
0	0	1	1	1	1	1	≈	
0	1	0	0	0	0	0	Blank	
0	1	0	0	0	0	1	!	
0	1	0	0	0	1	0	"	
0	1	0	0	0	1	1	#	
0	1	0	0	1	0	0	$	
0	1	0	0	1	0	1	%	
0	1	0	0	1	1	0	&	
0	1	0	0	1	1	1	'	
0	1	0	1	0	0	0	(	
0	1	0	1	0	0	1	)	
0	1	0	1	0	1	0	*	
0	1	0	1	0	1	1	+	
0	1	0	1	1	0	0	,	yes
0	1	0	1	1	0	1	—	
0	1	0	1	1	1	0	.	
0	1	0	1	1	1	1	/	
0	1	1	0	0	0	0	0	
0	1	1	0	0	0	1	1	
0	1	1	0	0	1	0	2	
0	1	1	0	0	1	1	3	
0	1	1	0	1	0	0	4	
0	1	1	0	1	0	1	5	
0	1	1	0	1	1	0	6	
0	1	1	0	1	1	1	7	
0	1	1	1	0	0	0	8	
0	1	1	1	0	0	1	9	
0	1	1	1	0	1	0	:	
0	1	1	1	0	1	1	;	
0	1	1	1	1	0	0	<	
0	1	1	1	1	0	1	=	
0	1	1	1	1	1	0	>	
0	1	1	1	1	1	1	?	

ADDRESS (A)							DISPLAYED CHARACTER	SHIFTED
7	6	5	4	3	2	1		
1	0	0	0	0	0	0	@	
1	0	0	0	0	0	1	A	
1	0	0	0	0	1	0	B	
1	0	0	0	0	1	1	C	
1	0	0	0	1	0	0	D	
1	0	0	0	1	0	1	E	
1	0	0	0	1	1	0	F	
1	0	0	0	1	1	1	G	
1	0	0	1	0	0	0	H	
1	0	0	1	0	0	1	I	
1	0	0	1	0	1	0	J	
1	0	0	1	0	1	1	K	
1	0	0	1	1	0	0	L	
1	0	0	1	1	0	1	M	
1	0	0	1	1	1	0	N	
1	0	0	1	1	1	1	O	
1	0	1	0	0	0	0	P	
1	0	1	0	0	0	1	Q	
1	0	1	0	0	1	0	R	
1	0	1	0	0	1	1	S	
1	0	1	0	1	0	0	T	
1	0	1	0	1	0	1	U	
1	0	1	0	1	1	0	V	
1	0	1	0	1	1	1	W	
1	0	1	1	0	0	0	X	
1	0	1	1	0	0	1	Y	
1	0	1	1	0	1	0	Z	
1	0	1	1	0	1	1		
1	0	1	1	1	0	0	—	
1	0	1	1	1	0	1	|	
1	0	1	1	1	1	0	—	
1	0	1	1	1	1	1	—	
1	1	0	0	0	0	0	`	
1	1	0	0	0	0	1	a	
1	1	0	0	0	1	0	b	
1	1	0	0	0	1	1	c	
1	1	0	0	1	0	0	d	
1	1	0	0	1	0	1	e	
1	1	0	0	1	1	0	f	
1	1	0	0	1	1	1	g	yes
1	1	0	1	0	0	0	h	
1	1	0	1	0	0	1	i	
1	1	0	1	0	1	0	j	yes
1	1	0	1	0	1	1	k	
1	1	0	1	1	0	0	l	
1	1	0	1	1	0	1	m	
1	1	0	1	1	1	0	n	
1	1	0	1	1	1	1	o	
1	1	1	0	0	0	0	p	yes
1	1	1	0	0	0	1	q	yes
1	1	1	0	0	1	0	r	
1	1	1	0	0	1	1	s	
1	1	1	0	1	0	0	t	
1	1	1	0	1	0	1	u	
1	1	1	0	1	1	0	v	
1	1	1	0	1	1	1	w	
1	1	1	1	0	0	0	x	
1	1	1	1	0	0	1	y	yes
1	1	1	1	0	1	0	z	
1	1	1	1	0	1	1	{	
1	1	1	1	1	0	0	¦	
1	1	1	1	1	0	1	}	
1	1	1	1	1	1	0	~	
1	1	1	1	1	1	1	Solid	

CARD FORMAT HEADER CARDS



CHARACTER SET UP CARD



CHARACTER SET UP CARD

Card #6

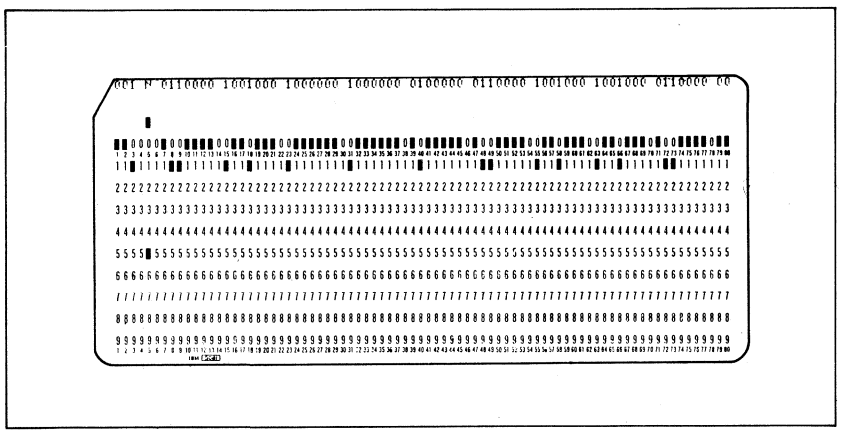
Columns	
1	Type in —, NONSHIFT =
10 & 11	Enter decimal number that corresponds to TOP row of the nonshifted characters
13-18	Type in —, SHIFT =
19 & 20	Enter decimal number that corresponds to TOP row of shifted characters
22-27	Type in —, COUNT =
28 & 29	These columns are used to identify the direction of the numerical count for the subsequent row numbers. When "DN" is punched this adds -1 to the number of top row of character to get the second row; third row is -2; etc.
30-78	Leave blank
79 & 80	Enter truth table number

CHARACTER CARDS

This format identifies characters by numerical sequence beginning with 001 (the first character of the set) and ending with 128 (the last character of the set). Address 0000000 is used for character #1, with other characters following in normal binary progression with A_1 the LSB and A_7 the MSB.

Columns	
1-3	Enter decimal character number
4	Leave blank
5	Enter character position: S for shifted, N for nonshifted
6	Leave blank
7-13	Enter contents of the top row of character beginning with the least significant bit (B_1) and ending with the most significant bit (B_7)[A,B]
14	Leave blank
15-21	Enter contents of second row of character (LSB to MSB)
22	Leave blank
23-29	Enter third row
30	Leave blank
31-77	Continue until contents of all 9 rows have been entered
78	Leave blank
79 & 80	Enter truth table number

CHARACTER CARD



NOTES

A. An entered dot corresponds to a high voltage output
B. A complete card deck consists of 5 header cards, 1 set up card and 128 character cards

DESCRIPTION

The Signetics 2616 is a 16,384-bit static MOS read-only memory organized as 2048 words by 8 bits. This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The inputs and outputs are fully TTL compatible. This device operates with a single 5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined by the designer and the desired chip select logic level is fixed during the masking process. These three programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

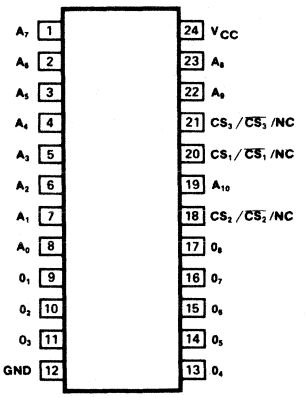
The 2616 read-only memory is fabricated with n-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits. Only a single 5V power supply is needed and all devices are directly TTL compatible.

FEATURES

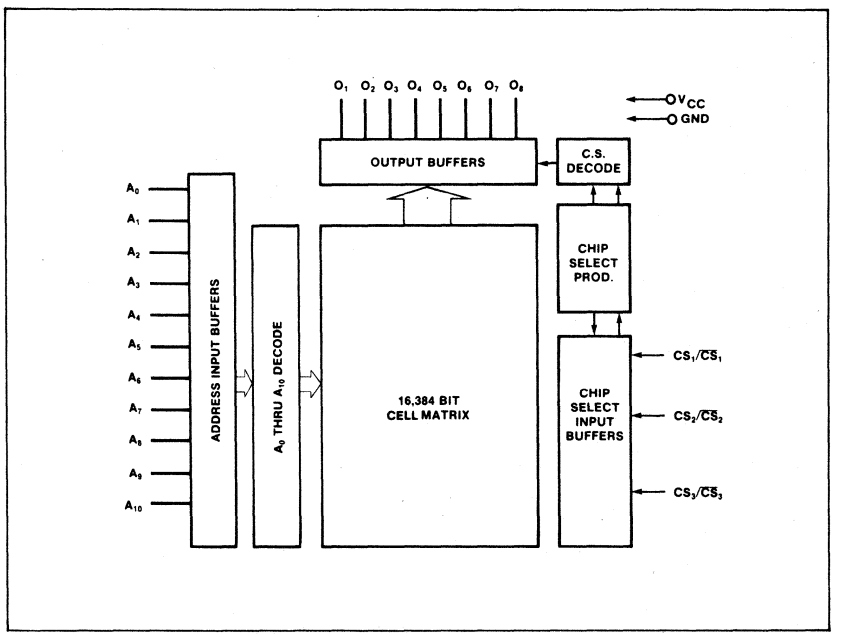
- **Single 5V power supply**
- **Guaranteed 350/450ns access time**
- **Directly TTL compatible—all inputs and outputs**
- **Three programmable chip select inputs for easy memory expansion or no connection option**
- **Three-state output—OR-tie capability**
- **Fully decoded—on chip address decode**
- **Inputs protected—all inputs have protection against static charge**

PIN CONFIGURATION

F,I,N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
	Supply voltage to ground potential	-0.5 to 7	V
	Applied voltage		V
	Input	-0.5 to 7	
	Output	-0.5 to 7	
P_D	Power dissipation	1	W

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% unless otherwise specified

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[2]					V
V_{IL}	Low		-0.5		0.8	
V_{IH}	High		2.2		V_{CC}	
	Output voltage	V_{CC} = 4.75V				V
V_{OL}	Low	I_{OL} = 1.6mA			0.4	
V_{OH}	High	I_{OH} = -100μA	2.4		V_{CC}	
I_{LI}	Input load current	V_{CC} = 5.25V, OV ≤ V_{IN} ≤ 5.25V			10	μA
I_{LO}	Output leakage current	Chip deselected, V_{OUT} = 0.4V to V_{CC}			10	μA
I_{CC}	Supply current	Output unloaded, T_A = 25°C, V_{CC} = 5.25V, V_{IN} = V_{CC}			115	mA
	Capacitance[3]	T_A = 25°C, f = 1.0MHz, all pins except pin under test tied to ac ground				pF
C_{IN}	Input				7	
C_O	Output				10	

AC ELECTRICAL CHARACTERISTICS

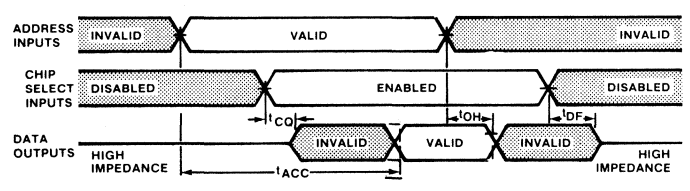
T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%, Output load = 1 TTL load and 100pF, Input transition time = 20ns, Timing reference levels: Input = 0.8V and 2.2V, Output = 0.4V and 2.4V unless otherwise specified.

PARAMETER		2616			2616-1			UNIT
		Min	Typ	Max	Min	Typ	Max	
t_{ACC}	Address access time			450			350	ns
t_{CO}	Chip select delay			200			150	ns
t_{DF}	Chip deselect delay			200			150	ns
t_{OH}	Previous data valid after address change delay	20			20			ns

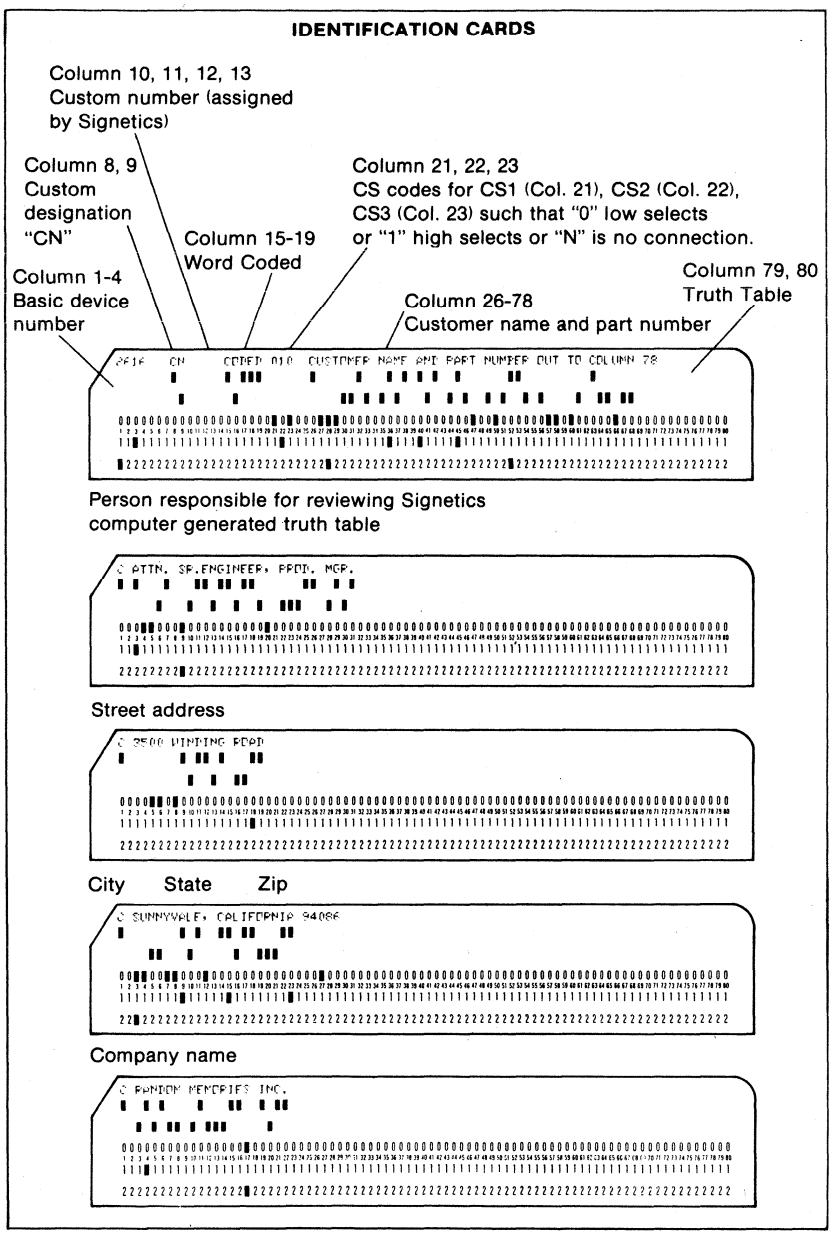
NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Input levels that swing more negative than -0.5V will be clamped and may cause damage to the device.
3. This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



CARD FORMAT



PROGRAMMING INSTRUCTIONS

2616

All Signetics Read Only Memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern is supplied on standard 80 column computer cards in the format described below.

All address and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of:

A. Title card
B. Comment cards
C. Data cards

For the user's convenience the data cards consisting of address and bit patterns can be specified in any one of three formats:

1. The hexadecimal format, where each data card carries (in hexadecimal) the initial input address for the 32 output words contained on that card, the 32 output words themselves (in hexadecimal) and the ROM truth table number. An N word ROM, therefore, requires n/32 cards, with all 32 output words defined on each card.
2. The octal format, where each data card carries (in octal) the initial input address for the 16 output words contained on that card, the 16 output words themselves (in octal) and the ROM truth table number. An N word ROM, therefore, requires N/16 cards, with all 16 output words defined on each card.
3. The binary format, where each data card carries (in decimal) the initial input address for the 8 output words contained on that card, the 8 output words themselves (in binary) and the ROM truth table number. An N word ROM, therefore, requires N/8 cards, with all 8 output words defined on each card.

Positive logic is used on all input cards; a logic "1" is the most positive voltage level and a logic "0" is the most negative level

Title Card

COLUMN	INFORMATION
1-4	Signetics Part Number, that is, 2600, 2616, 2620, etc.
7-13	Leave blank ——— Pattern Number to be assigned by Signetics.
15-19	Punch the letters "CODED"
21	CS1/CS1/NC Chip Select Logic Level (If low selects chip, punch "0"; if high selects chip, punch "1"; if no connection, punch "N".)

PROGRAMMING INSTRUCTIONS

2616 (Cont'd)

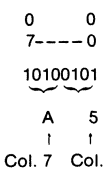
22	CS2/$\overline{CS2}$/NC Chip Select Logic Level
23	CS3/$\overline{CS3}$/NC Chip Select Logic Level
26-78	Customer Identification
79-80	ROM Truth Table Number (may be left blank)

Comment Cards

Any number of comment cards may be used for specifying the user's name, telephone number, address, any special instructions, etc. On these cards the letter "C" must be punched in column 1 and comments can be punched in columns 2-80.

Hexadecimal Format Data Cards

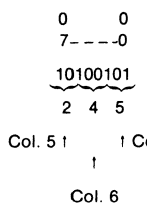
COLUMN	INFORMATION
1-5	Hexadecimal equivalent of the binary input address (A_0 = LSB). This is the initial input address and is punched right justified, that is, 00000, 00020, 00040, etc.
7-8	Hexadecimal equivalent of the binary output data (O_0 = LSB) for initial input address. EXAMPLE: Column 7 is upper 4 bits.



9-10	Output data for initial input address +1.
11-12	Output data for initial input address +2.
⋮	⋮
67-68	Output data for initial input address +30.
69-70	Output data for initial input address +31.
79-80	ROM truth table number (may be left blank)

Octal Format Data Cards

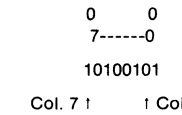
COLUMN	INFORMATION
1-4	Octal equivalent of the binary input address (A_0 = LSB). This is the initial input address and is punched right justified, that is, 0000, 0020, 0040, etc.
5-7	Octal equivalent of the binary output data (O_0 = LSB) for initial input address. EXAMPLE:



8-10	Output data for initial input address +1.
11-13	Output data for initial input address +2.
⋮	⋮
47-49	Output data for initial input address +14.
50-52	Output data for initial input address +15.
79-80	ROM truth table number (may be left blank).

Binary Format Data Cards

COLUMN	INFORMATION
1-5	Decimal equivalent of the binary input address (A_0 = LSB). This is the initial input address and is punched right justified, that is, 00000, 00008, 00016, etc.
7-14	Binary output data (O_0 = LSB) for initial input address. Output data can also be punched with a "P" or an "N" instead of a "1" or a "0," respectively.



16-23	Output data for initial input address +1.
25-32	Output data for initial input address +2.
34-41	Output data for initial input address +3.
43-50	Output data for initial input address +4.
52-59	Output data for initial input address +5.
61-68	Output data for initial input address +6.
70-77	Output data for initial input address +7.
79-80	ROM truth table number (may be left blank).

2617-F,I,N • 2617-1 - F,I,N

DESCRIPTION

The Signetics 2617 is a 16,384-bit static MOS read-only memory organized as 2048 words by 8 bits. This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The inputs and outputs are fully TTL compatible. This device operates with a single 5V power supply. The two chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined by the designer and the desired chip select logic level is fixed during the masking process. These two programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitate easy memory expansion.

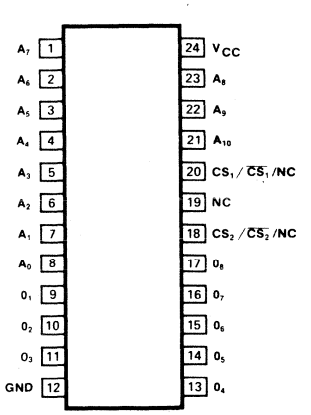
The 2617 read-only memory is fabricated with n-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits. Only a single 5V power supply is needed and all devices are directly TTL compatible.

FEATURES

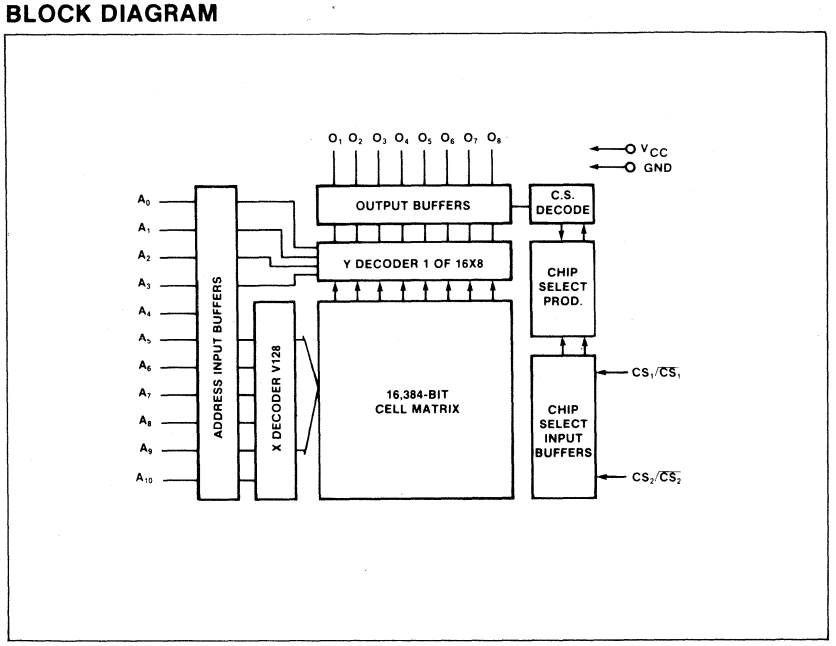
- **Single 5V power supply**
- **Guaranteed 350/450ns access time**
- **Directly TTL compatible—all inputs and outputs**
- **Two programmable chip select inputs for easy memory expansion or no connection option**
- **Three-state output—OR-tie capability**
- **Fully decoded—on chip address decode**
- **Inputs protected—all inputs have protection against static charge**

PIN CONFIGURATION

F,I,N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
	Supply voltage to ground potential	-0.5 to 7	V
	Applied voltage		V
	Input	-0.5 to 7	
	Output	-0.5 to 7	
P_D	Power dissipation	1	W

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% unless otherwise specified

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[2]					V
V_{IL}	Low		-0.5		0.8	
V_{IH}	High		2.2		V_{CC}	
	Output voltage	V_{CC} = 4.75V				V
V_{OL}	Low	I_{OL} = 1.6mA			0.4	
V_{OH}	High	I_{OH} = -100μA	2.4		V_{CC}	
I_{LI}	Input load current	V_{CC} = 5.25V, OV ≤ V_{IN} ≤ 5.25V			10	μA
I_{LO}	Output leakage current	Chip deselected, V_{OUT} = 0.4V to V_{CC}			10	μA
I_{CC}	Supply current	Output unloaded, T_A = 25°C, V_{CC} = 5.25V, V_{IN} = V_{CC}			115	mA
	Capacitance[3]	T_A = 25°C, f = 1.0MHz, all pins except pin under test tied to ac ground				pF
C_{IN}	Input				7	
C_O	Output				10	

AC ELECTRICAL CHARACTERISTICS

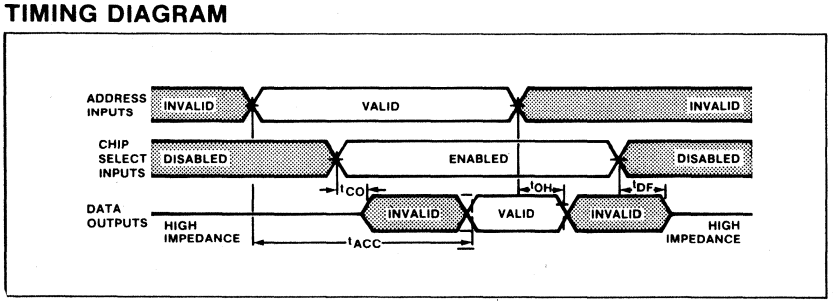
T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%, Output load = 1 TTL load and 100pF, Input transition time = 20ns, Timing reference levels: Input = 0.8V and 2.2V, Output = 0.4V and 2.4V unless otherwise specified.

PARAMETER		2617			2617-1			UNIT
		Min	Typ	Max	Min	Typ	Max	
t_{ACC}	Address access time			450			350	ns
t_{CO}	Chip select delay			200			150	ns
t_{DF}	Chip deselect delay			200			150	ns
t_{OH}	Previous data valid after address change delay	20			20			ns

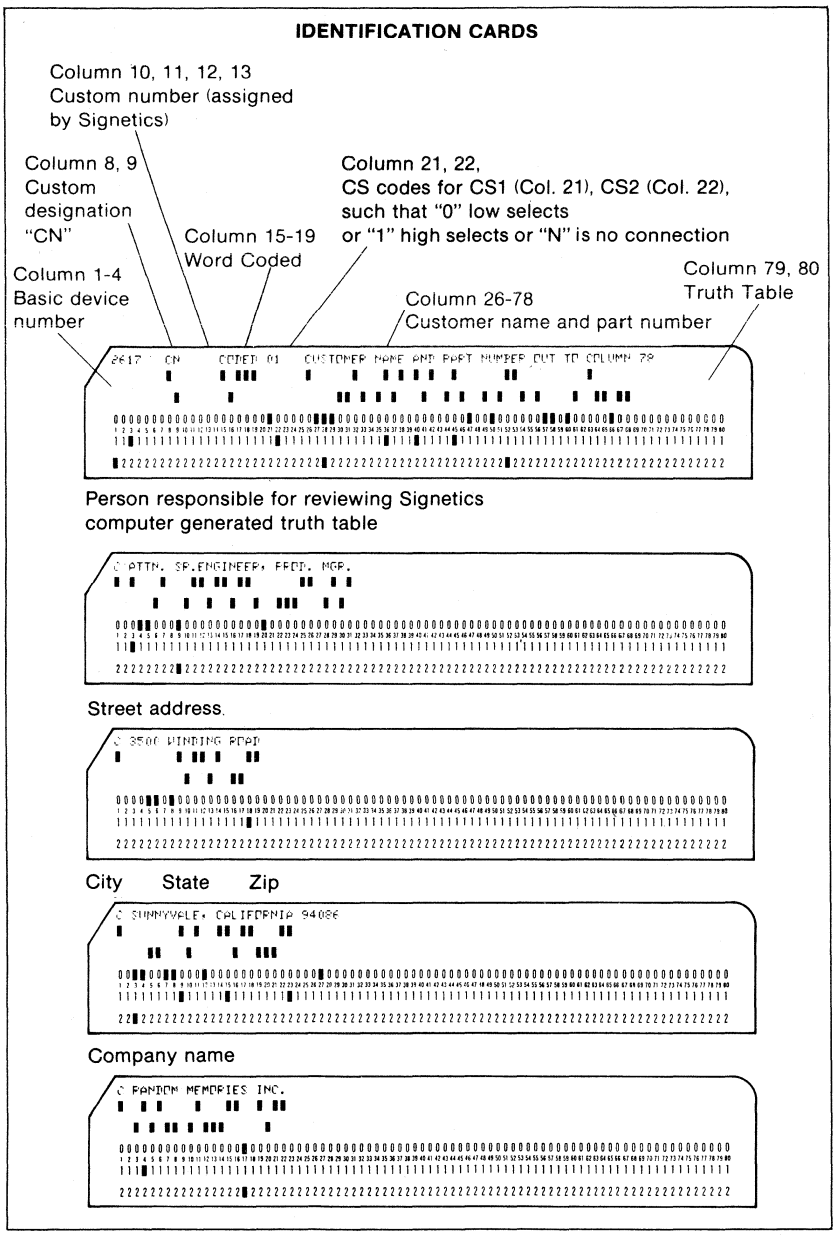
NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Input levels that swing more negative than -0.5V will be clamped and may cause damage to the device.
3. This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



CARD FORMAT



PROGRAMMING INSTRUCTIONS

2617

All Signetics Read Only Memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern is supplied on standard 80 column computer cards in the format described below.

All address and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of:

A. Title card
B. Comment cards
C. Data cards

For the user's convenience the data cards consisting of address and bit patterns can be specified in any one of three formats:

1. The hexadecimal format, where each data card carries (in hexadecimal) the initial input address for the 32 output words contained on that card, the 32 output words themselves (in hexadecimal) and the ROM truth table number. An N word ROM, therefore, requires N/32 cards, with all 32 output words defined on each card.
2. The octal format, where each data card carries (in octal) the initial input address for the 16 output words contained on that card, the 16 output words themselves (in octal) and the ROM truth table number. An N word ROM, therefore, requires N/16 cards, with all 16 output words defined on each card.
3. The binary format, where each data card carries (in decimal) the initial input address for the 8 output words contained on that card, the 8 output words themselves (in binary) and the ROM truth table number. An N word ROM, therefore, requires N/8 cards, with all 8 output words defined on each card.

Positive logic is used on all input cards; a logic "1" is the most positive voltage level and a logic "0" is the most negative level.

Title Card

COLUMN	INFORMATION
1-4	Signetics Part Number, that is, 2600, 2616, 2620, etc.
7-13	Leave blank ____ Pattern Number to be assigned by Signetics.
15-19	Punch the letters "CODED"
21	CS1/$\overline{CS1}$/NC Chip Select Logic Level (If low selects chip, punch "0"; if high selects chip, punch "1"; if no connection, punch "N".)

PROGRAMMING INSTRUCTIONS

2617 (Cont'd)

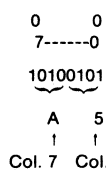
22	CS2/$\overline{CS2}$/NC Chip Select Logic Level
26-78	Customer Identification
79-80	ROM Truth Table Number (may be left bank)

Comment Cards

Any number of comment cards may be used for specifying the user's name, telephone number, address, any special instructions, etc. On these cards the letter "C" must be punched in column 1 and comments can be punched in columns 2-80.

Hexadecimal Format Data Cards

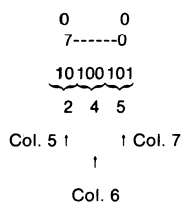
COLUMN	INFORMATION
1-5	Hexadecimal equivalent of the binary input address (A_0 = LSB). This is the initial input address and is punched right justified, that is, 00000, 00020, 00040, etc.
7-8	Hexadecimal equivalent of the binary output data (O_0 = LSB) for initial input address. EXAMPLE: Column 7 is upper 4 bits.



9-10	Output data for initial input address +1.
11-12	Output data for initial input address +2.
67-68	Output data for initial input address +30.
69-70	Output data for initial input address +31.
79-80	ROM truth table number (may be left blank)

Octal Format Data Cards

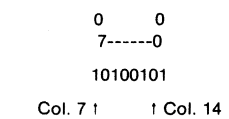
COLUMN	INFORMATION
1-4	Octal equivalent of the binary input address (A_0 = LSB). This is the initial input address and is punched right justified, that is, 0000, 0020, 0040, etc.
5-7	Octal equivalent of the binary output data (O_0 = LSB) for initial input address. EXAMPLE:



8-10	Output data for initial input address +1.
11-13	Output data for initial input address +2.
47-49	Output data for initial input address +14.
50-52	Output data for initial input address +15.
79-80	ROM truth table number (may be left blank).

Binary Format Data Cards

COLUMN	INFORMATION
1-5	Decimal equivalent of the binary input address (A_0 = LSB). This is the initial input address and is punched right justified, that is, 00000, 00008, 00016, etc.
7-14	Binary output data (O_0 = LSB) for initial input address. Output data can also be punched with a "P" or an "N" instead of a "1" or a "0", respectively.



16-23	Output data for initial input address +1.
25-32	Output data for initial input uddress +2.
34-41	Output data for initial input address +3.
43-50	Output data for initial input address +4.
52-59	Output data for initial input address +5.
61-68	Output data for initial input address +6.
70-77	Output data for initial input address +7.
79-80	ROM truth table number (may be left blank).

2620-F

DESCRIPTION

This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

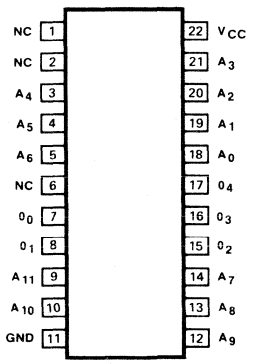
The 2620 Read Only Memory is fabricated with n-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits.

FEATURES

- **Guaranteed 450ns access time**
- **Power dissipation: 525mW max**
- **Completely TTL compatible**
- **Single +5V power supply**
- **Standard 22-pin package**

PIN CONFIGURATION

F PACKAGE



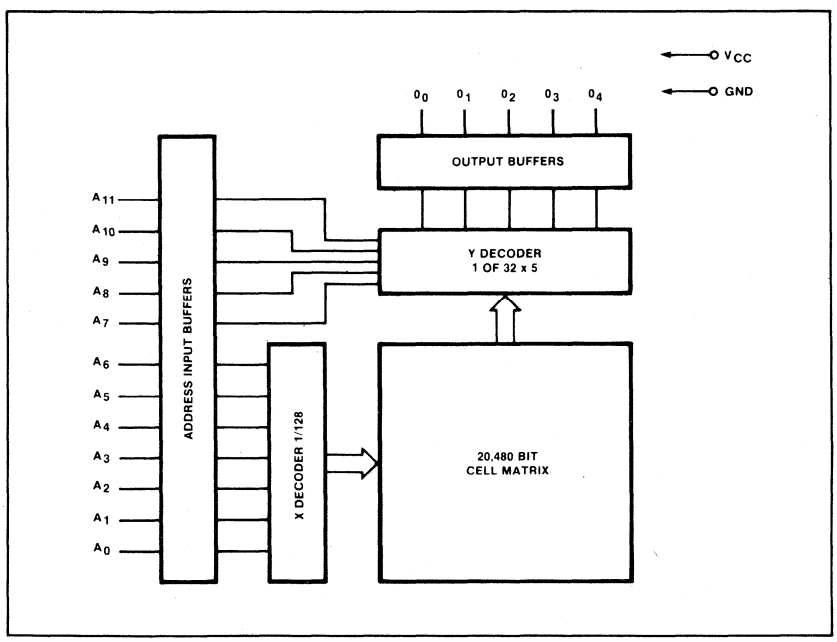
ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating	0° to +70	
T_{STG}	Storage	-65° to +150	
P_D	Power dissipation	1.2	W
	Applied voltage		V
	Input	-0.5 to +7	
	Output	-0.5 to +7	
	Supply voltage to ground potential	-0.5 to +7	V

NOTE

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



2620-F

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%, unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low		-0.5		0.8	
V_{IH}	High		2.2		V_{CC}	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA			0.4	
V_{OH}	High	I_{OH} = -100μA	2.4		V_{CC}	
I_{LI}	Input load current	0V ≤ V_{IN} ≤ 5.25V			10	μA
I_{CC}	Supply current	Output unloaded, V_{IN} = V_{CC}			100	mA
	Capacitance[2]	T_A = 25°C, f = 1MHz, all pins except pins under test tied to ground				pF
C_{IN}	Input				7	
C_{OUT}	Output				10	

NOTE

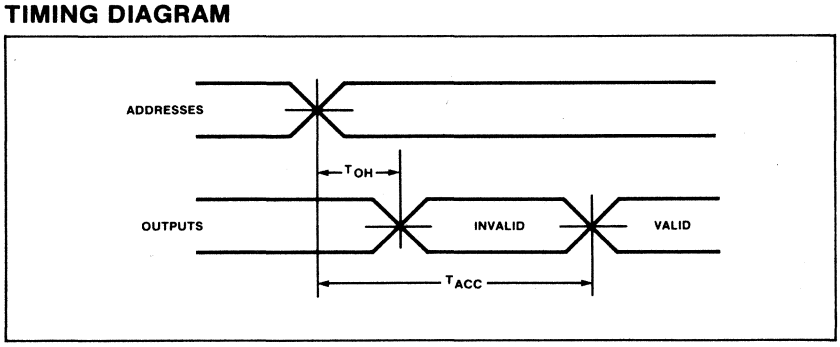
2. This parameter is peiodically sampled and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%, unless otherwise specified.

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
t_{ACC}	Address access time	Data out	Address	Output load: 1 TTL load and 100pF			450	ns
T_{OH}	Previous data valid after address change delay	Data out invalid	Address		20			ns

TIMING DIAGRAM



OBJECTIVE SPECIFICATION 2632-F,I,N

DESCRIPTION

This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The two chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined by the designer and the desired chip select logic level is fixed during the masking process. These two programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

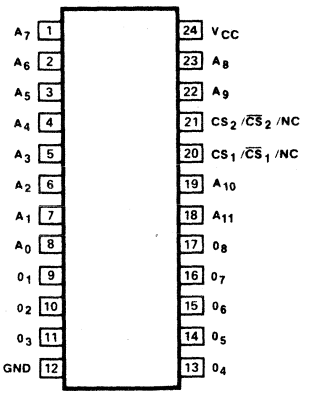
The 2632 Read Only Memory is fabricated with n-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits.

FEATURES

- **Guaranteed 450ns address time**
- **Completely TTL compatible**
- **Single +5V power supply**
- **3-state output—OR-tie capability**
- **Fully decoded—on chip address decode**
- **Inputs protected—all inputs have protection against static charge**

PIN CONFIGURATION

F,I,N PACKAGE



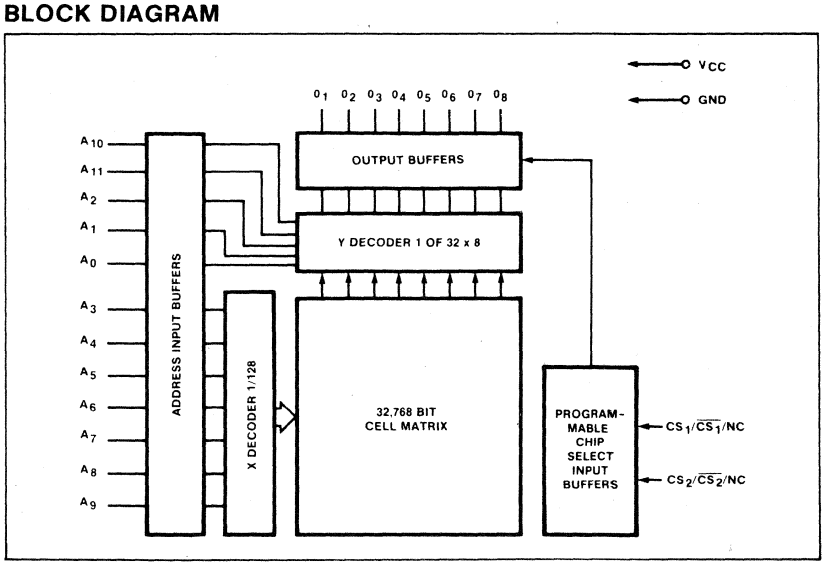
ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating	0° to +70	
T_{STG}	Storage	-65° to +150	
P_D	Power dissipation	1.2	W
	Applied voltage		V
	Input	-0.5 to +7	
	Output	-0.5 to +7	
	Supply voltage to ground potential	-0.5 to +7	V

NOTE

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



OBJECTIVE SPECIFICATION 2632-F,I,N

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%, unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low[2]		-0.5		0.8	
V_{IH}	High		2.2		V_{CC}	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA			0.4	
V_{OH}	High	I_{OH} = -100μA	2.4		V_{CC}	
I_{LI}	Input load current	OV ≤ V_{IN} ≤ 5.25V			10	μA
I_{LO}	Output leakage	Chip deselected V_{OUT} = +0.4V to V_{CC}			10	μA
I_{CC}	Supply current	Output unloaded T_A = 25°C, V_{IN} = V_{CC}			80	mA
	Capacitance[3]	T_A = 25°C, f = 1MHz, all pins except pin under test tied to ground				pF
C_{IN}	Input				7	
C_{OUT}	Output				10	

NOTES

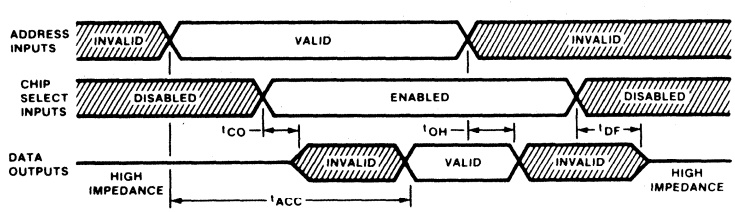
2. Input levels that swing more negative than -0.5 will be clamped and may cause damage to the device.
3. This parameter is periodically sampled and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ± 5%, Output load = 1 TTL load and 100pF, Input transition time = 20ns, Timing reference levels: Input = 0.8V and 2.2V, Output = 0.4V and 2.4V unless otherwise specified.

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
t_{ACC}	Address access time			450	ns
t_{CO}	Chip select delay			200	ns
t_{DF}	Chip deselect delay			200	ns
t_{OH}	Previous data valid after address change delay	20			ns

TIMING DIAGRAM



OBJECTIVE SPECIFICATION 2664-F,I,N

DESCRIPTION

This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The chip select input is programmable. Active high or active low level chip select input can be defined by the designer and the desired chip select logic level is fixed during the masking process. The programmable chip select input, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

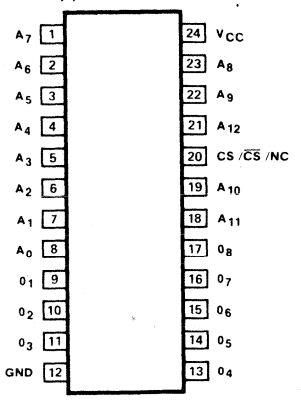
The 2664 Read Only Memory is fabricated with n-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits.

FEATURES

- **Guaranteed 450ns access time**
- **Completely TTL compatible**
- **One +5V power supply**
- **3-state output—OR-tie capability**
- **Fully decoded—on chip address decode**
- **Inputs protected—all inputs have protection against static charge**

PIN CONFIGURATION

F,I,N PACKAGE



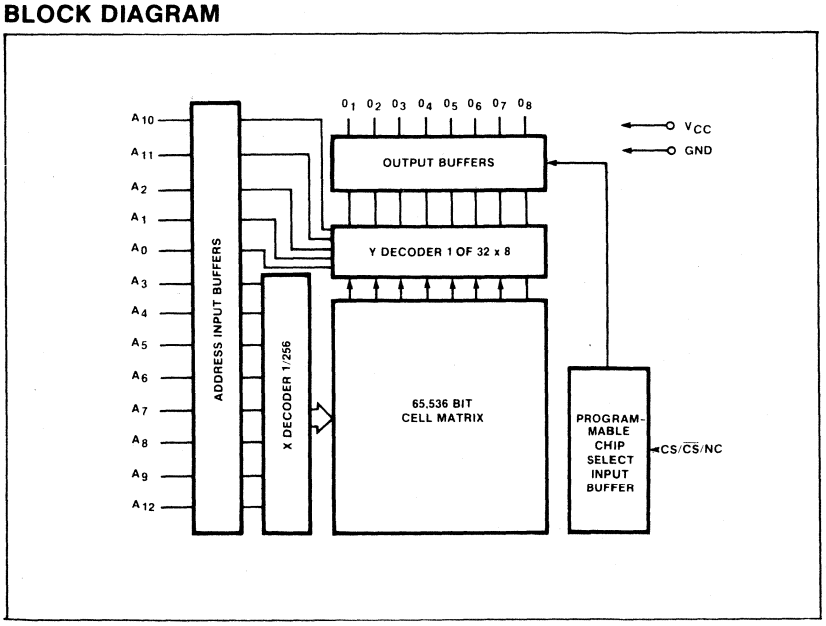
ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating	0° to +70	
T_{STG}	Storage	-65° to +150	
P_D	Power dissipation	1.5	W
	Applied voltage		V
	Input	-0.5 to +7	
	Output	-0.5 to +7	
	Supply voltage to ground potential	-0.5 to +7	V

NOTE

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%, unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low[2]		-0.5		0.8	
V_{IH}	High		2.2		V_{CC}	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA			0.4	
V_{OH}	High	I_{OH} = -100μA	2.4		V_{CC}	
I_{LI}	Input load current	0V ≤ V_{IN} ≤ 5.25V			10	μA
I_{LO}	Output Leakage	Chip deselected, V_{OUT} = +0.4V to V_{CC}			10	μA
I_{CC}	Supply current	Output unloaded T_A = 25°C, V_{IN} = V_{CC}			150	mA
	Capacitance[3]	T_A = 25°C, f = 1MHz, all pins except pin under test tied to ground				pF
C_{IN}	Input				7	
C_{OUT}	Output				10	

NOTES

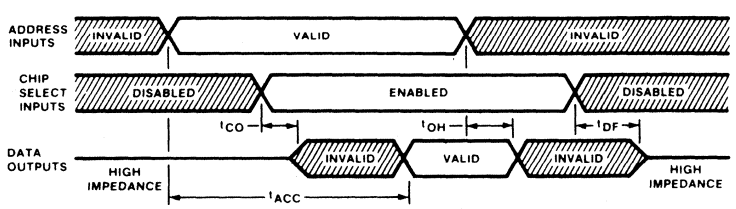
2. Input levels that swing more negative than -0.5V will be clamped and may cause damage to the device.
3. This parameter is periodically sampled and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%, Output load = 1 TTL load and 100pF, Input transition time = 20ns, Timing reference levels: Input = 0.8V and 2.2V, Output = 0.4V and 2.4V unless otherwise specified.

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
t_{ACC}	Address access time			450	ns
t_{CO}	Chip select delay			200	ns
t_{DF}	Chip deselect delay			200	ns
t_{OH}	Previous data valid after address change delay	20			ns

TIMING DIAGRAM



2101-F,N • 2101-1-F,N • 2101-2-F,N

DESCRIPTION

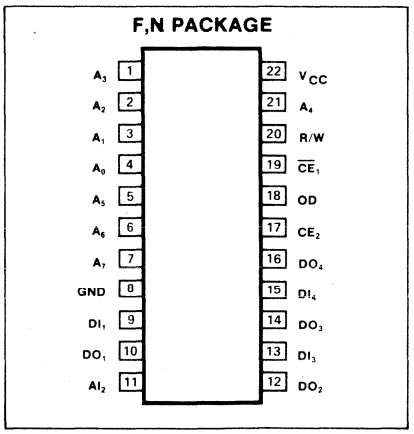
The 2101 series is high performance, low power static read/write RAM's.

The 2101 series is fabricated with n-channel silicon gate technology which allows the design of high performance easy to use MOS circuits and provides a high functional density on a given monolithic chip.

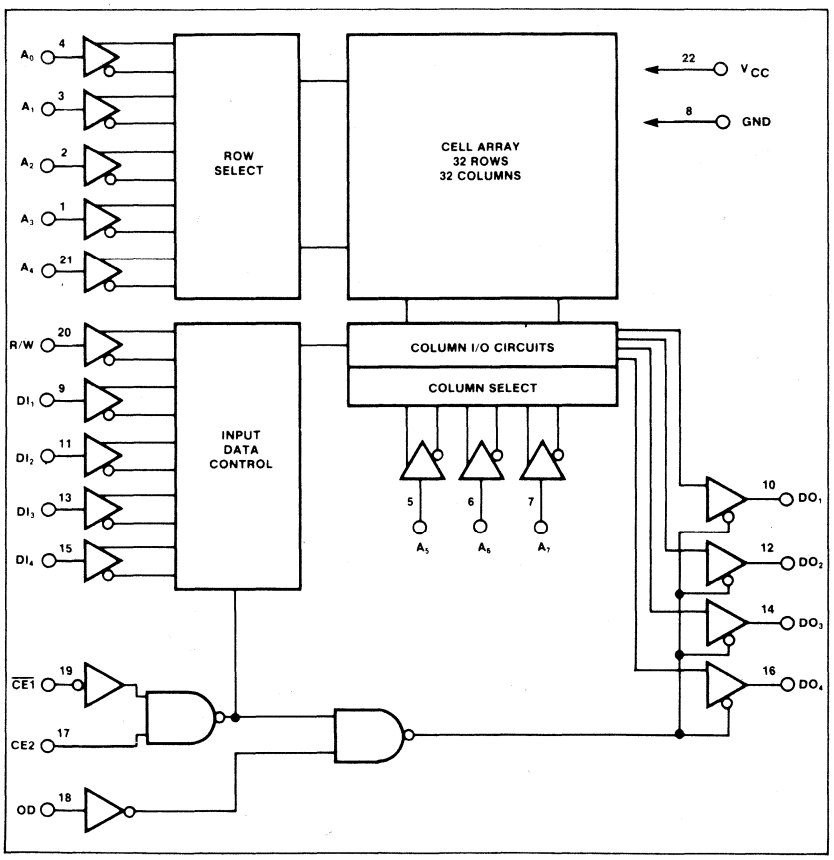
FEATURES

- **Fully static**
- **No refresh operations, sense amps or clocks required**
- **All inputs and outputs are TTL compatible**
- **One 5V power supply required**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating under bias	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation	1	W
	Voltage on any pin with respect to ground	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low		-0.5		0.65	
V_{IH}	High		2.2		V_{CC}	
	Output voltage					V
V_{OL}	Low	I_{OL} = 2.0mA			0.45	
V_{OH}	High	I_{OH} = 150μA	2.2			
I_{LI}	Input current	V_{IN} = 0 to 5.25V			10	μA
	I/O leakage current[3]	$\overline{CE}_1$ = 2.2V				μA
I_{LOH}		V_{OUT} = 4.0V			15	
I_{LOL}		V_{OUT} = 0.45V			-50	
	Supply current	V_{IN} = 5.25V, I_O = OmA				mA
I_{CC1}		T_A = 25°C		30	60	
I_{CC2}		T_A = 0°C			70	
	Capacitance[3]					pF
C_{IN}	Input (All pins)	V_{IN} = 0V		4	8	
C_{OUT}	Output	V_{OUT} = 0V		8	12	

AC ELECTRICAL CHARACTERISTICS

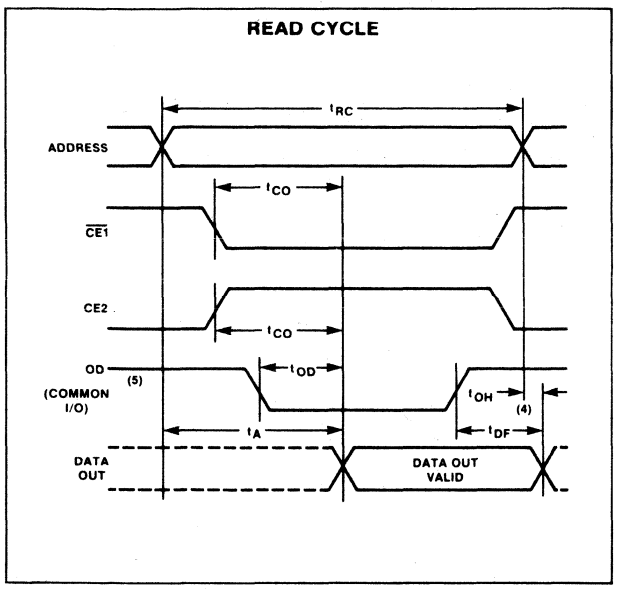
T_A =0°C to 70°C, V_{CC} = 5V ± 5%, Input pulse levels = +0.65V to 2.2V, Input pulse rise and fall times = 20ns, Timing measurement reference level = 1.5V, Output load = 1 TTL gate and C_L = 100pF, unless otherwise specified.

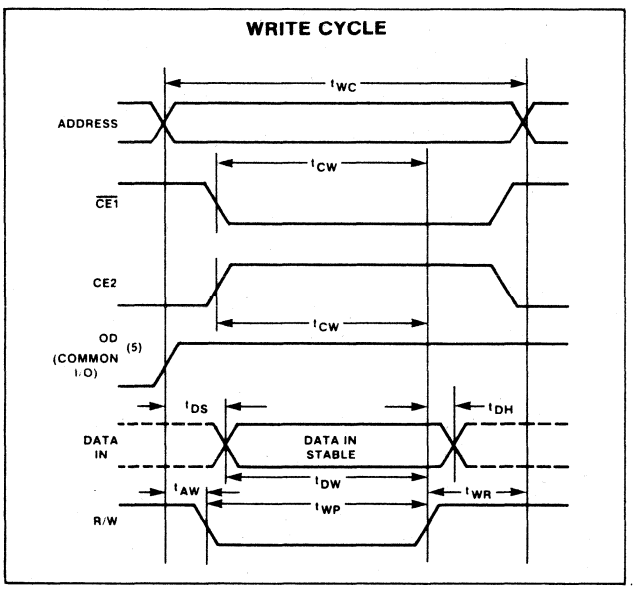
PARAMETER		TO	FROM	2101			2101-1			2101-2			UNIT
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	READ CYCLE												
t_{RC}	Read cycle			1,000			500			650			ns
t_A	Access time					1,000			500			650	ns
t_{CO}		Output	Chip enable			800			350			400	ns
t_{OD}		Output	Output disable			700			300			350	ns
t_{DF}[4]		High Z state	Data output	0		200	0		150	0		150	ns
t_{OH}	Previous read data valid after change of address			40			40			40			ns
	WRITE CYCLE												
t_{WC}	Write cycle			1,000			500			650			ns
t_{AW}	Write delay			150			100			150			ns
t_{CW}		Write	Chip enable	900			400			550			ns
	Setup and hold time												ns
t_{DW}	Setup time	Rise of R/W	Data in	700			280			400			
t_{DH}	Hold time	Change of data in	Rise of R/W	100			100			100			
t_{DS}	Setup time	Output	Output disable	200			150			150			
t_{WP}	Write pulse			750			300			400			ns
t_{WR}	Write recovery			50			50			50			ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values are for T_A = 25°C and typical supply voltage.
3. This parameter is periodically sampled and is not 100% tested.
4. t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, CE_2 or OD, whichever occurs first.
5. CD should be tied low for separate I/O operation.

TIMING DIAGRAMS





DESCRIPTION

The 2101 series is a family of high performance, low power static read/write RAM's.

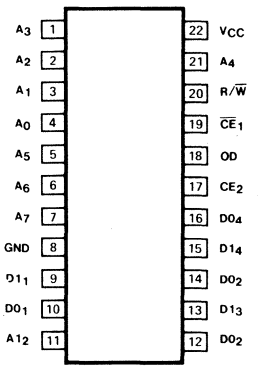
The 2101 series is fabricated with n-channel silicon gate technology which allows the design of high performance, easy-to-use MOS circuits and provides a high functional density on a given monolithic chip.

FEATURES

- **Fully static**
- **No refresh operations, sense amps or clocks required**
- **All inputs and outputs are TTL compatible**
- **Single 5V power supply required**
- **22-pin standard dip**
- **Output disable control**

PIN CONFIGURATION

F,N PACKAGE



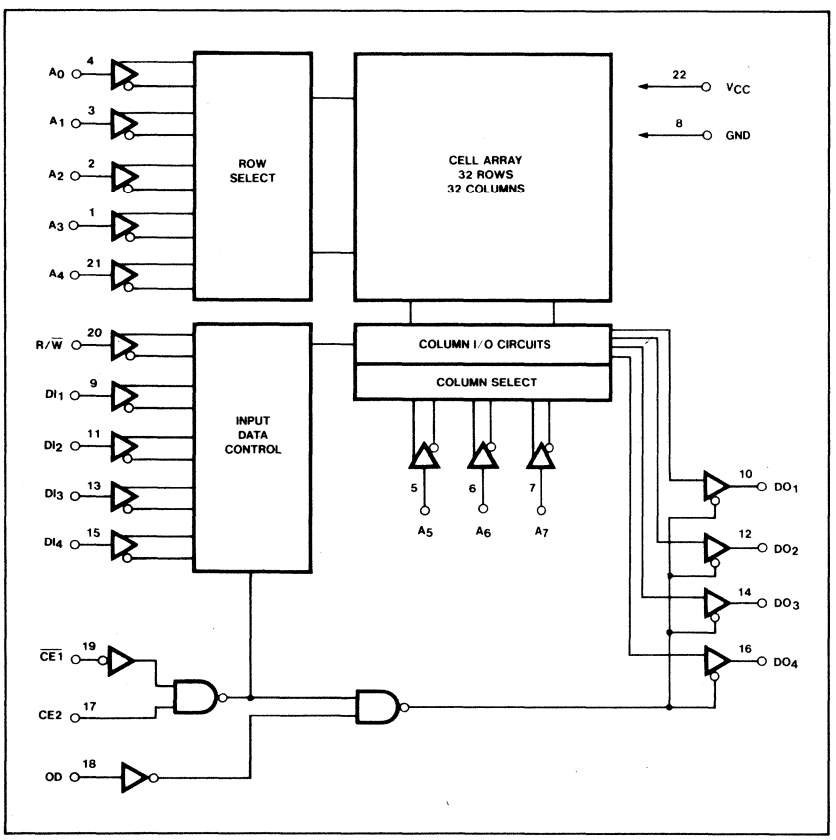
ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	−65 to 150	
P_D	Power dissipation	1	W
	Voltage on any pin with respect to ground	−0.5 to 7	V

NOTE

1. Stresses above those listed under "Absolute Maximum Ratings" cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

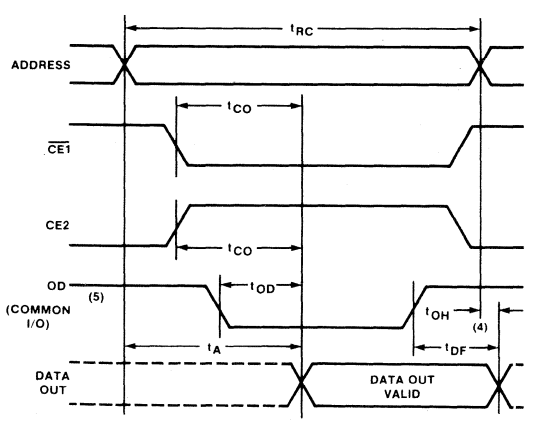
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low		−0.5		.8	
V_{IH}	High		2.0		V_{CC}	
	Output voltage					V
V_{OL}	Low	I_{OL} = 2.0mA			0.45	
V_{OH}	High	I_{OH} = 200μA	2.4			
I_{LI}	Input current	V_{IN} = 0 to 5.25V			10	μA
	I/O leakage current[3]	CE_1 = 2.0V				μA
I_{LOH}		V_{OUT} = 4.0V			10	
I_{LOL}		V_{OUT} = 0.45V			−10	
	Supply current	V_{IN} = 5.25V, I_O = OmA				mA
I_{CC1}		T_A = 25°C		40	55	
I_{CC2}		T_A = 0°C			70	
	Capacitance[3]					pF
C_{IN}	Input (all pins)	V_{IN} = 0V		4	8	
C_{OUT}	Output	V_{OUT} = 0V		8	12	

NOTES

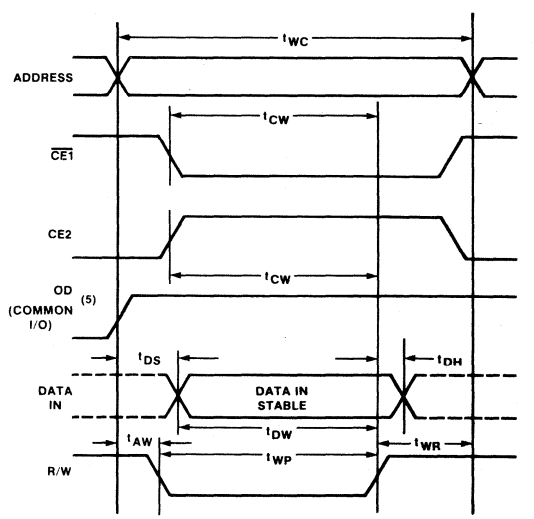
2. Typical values are for T_A = 25°C and typical supply voltage.
3. This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE



AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, Input pulse levels = +.8V to 2.0V, Input pulse rise and fall times = 20ns, Timing measurement reference level = 1.5V, Output load = 1 TTL gate and C_L = 100pF, unless otherwise specified.

	PARAMETER	TO	FROM	2101A-4			2101A			2101A-2			UNIT
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	READ CYCLE												ns
t_{RC}	Read cycle			450			350			250			
t_A	Access time					450			350			250	
t_{CO}		Output	Chip enable			310			240			180	
t_{OD}[5]		Output	Output disable			250			180			130	
t_{DF}[4]		High Z state	Data output	0		200	0		150	0		150	
t_{OH}	Previous read data valid after change of address			40			40			40			
	WRITE CYCLE												ns
t_{WC}	Write cycle			450			350			250			
t_{AW}	Write delay			20			20			20			
t_{CW}		Write	Chip enable	250			200			150			
	Setup and hold time												ns
t_{DW}	Setup time	Rise of R/$\overline{W}$	Data in	250			200			150			
t_{DH}	Hold time	Change of data in	Rise of R/$\overline{W}$	0			0			0			
t_{DS}	Setup time	Output	Output disable	20			20			20			
t_{WP}	Write pulse			250			200			150			ns
t_{WR}	Write recovery			0			0			0			ns

NOTES

4. t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, CE_2, or OD, whichever occurs first.
5. OD should be tied low for separate I/O operation.

2111-I,N • 2111-1-I,N • 2111-2-I,N

DESCRIPTION

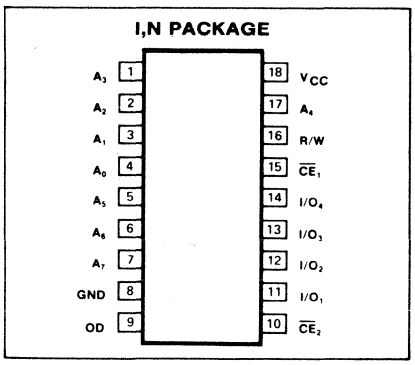
The 2111 series is a high-performance, low-power static read/write RAM.

The 2111 series is fabricated with n-channel silicon gate technology which allows the design of high performance easy to use MOS circuits and provides a high functional density on a given monolithic chip.

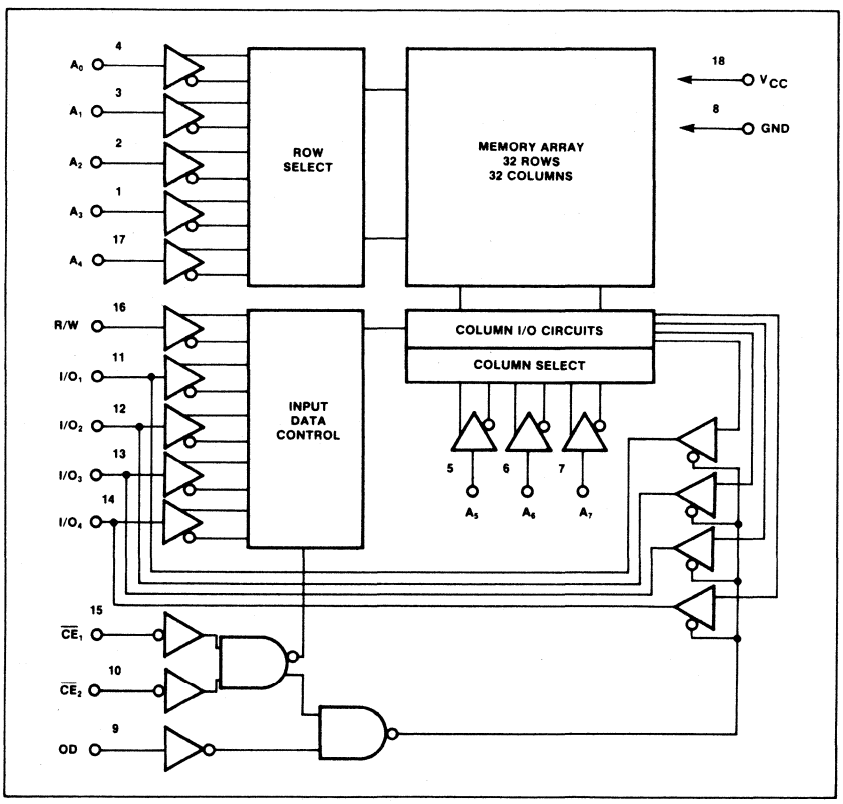
FEATURES

- **Fully static**
- **Requires no refresh operations, sense amps or clocks**
- **Completely TTL compatible**
- **Only one 5V power supply required**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating under bias	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation	1	W
	Voltage on any pin with respect to ground	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low		-0.5		0.65	
V_{IH}	High		2.2		V_{CC}	
	Output voltage					V
V_{OL}	Low	I_{OL} = 2.0mA			0.45	
V_{OH}	High	I_{OH} = -150μA	2.2			
I_{LI}	Input load current	V_{IN} = 0 to 5.25V			10	μA
	I/O leakage current	$\overline{CE_1} = \overline{CE_2}$ = 2.2V				μA
I_{LOH}		$V_{1/0}$ = 4.0V			15	
I_{LOL}		$V_{1/0}$ = 0.45V			-50	
	Supply current	V_{IN} = 5.25V, $I_{1/0}$ = OmA				mA
I_{CC1}		T_A = 25°C		30	60	
I_{CC2}		T_A = 0°C			70	
	Capacitance[3]	T_A = 25°C, f = 1MHz				pF
C_{IN}	Input	V_{IN} = OV		4	8	
$C_{I/O}$	I/O	$V_{I/O}$ = OV		10	15	

AC ELECTRICAL CHARACTERISTICS

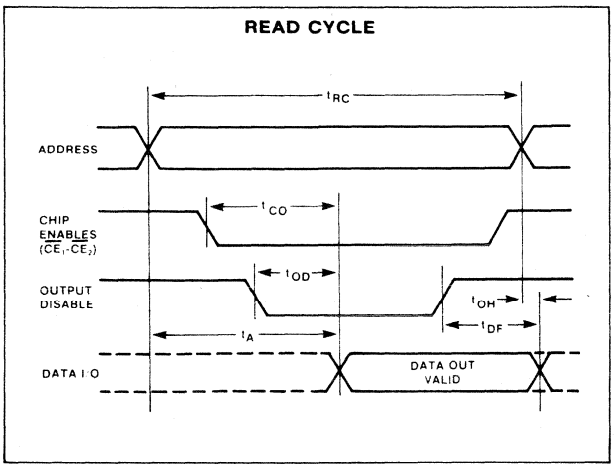
T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified,
Input pulse levels = 0.65V to 2.2V, Input pulse rise and fall times = 20ns,
Timing measurement reference level = 1.5V,
Output load = 1 TTL gate and C_L = 100pF

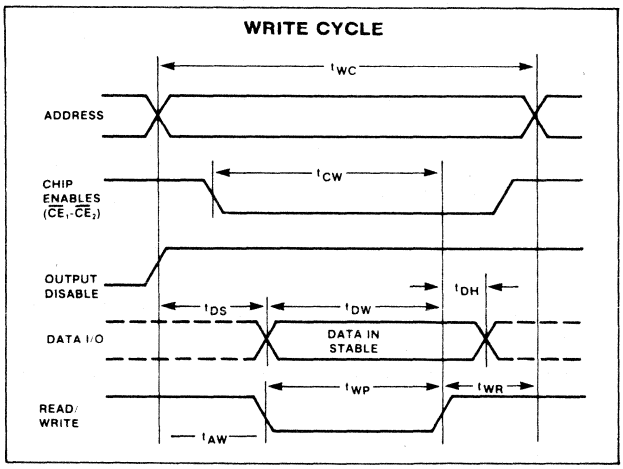
PARAMETER		TO	FROM	2111			2111-1			2111-2			UNIT
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	READ CYCLE												
t_{RC}	Read cycle			1,000			500			650			ns
t_A	Access time					1,000			500			650	ns
t_{CC}		Output	Chip enable			800			350			400	ns
t_{OD}		Output	Output disable			700			300			350	ns
t_{DF}[3]		High Z state	Data output	0		200	0		150	0		150	ns
t_{OH}	Previous read data valid after change of address			40			40			40			ns
	WRITE CYCLE												
t_{WC}	Write cycle			1,000			500			650			ns
t_{AW}	Write delay			150			100			150			ns
t_{CW}		Write	Chip enable	900			400			550			ns
	Setup and hold time												ns
t_{DW}	Setup time	R/W	Data	700			280			400			
t_{DH}	Hold time	Data	R/W	100			100			100			
t_{DS}	Setup time	Output	Output disable	200			150			150			
t_{WP}	Write pulse			750			300			400			ns
t_{WR}	Write recovery			50			50			50			ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values for T_A = 25°C and supply voltage.
3. This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAMS





DESCRIPTION

The 2111A series is a family of high-performance, low-power static read/write RAM's.

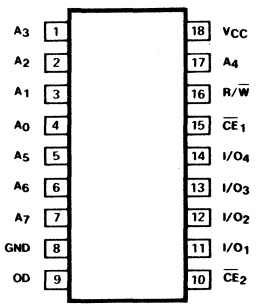
The 2111A series is fabricated with n-channel silicon gate technology which allows the design of high performance, easy-to-use MOS circuits and provides a high functional density on a given monolithic chip.

FEATURES

- **Fully static**
- **Requires no refresh operations, sense amps or clocks**
- **Completely TTL compatible**
- **Single 5V power supply required**
- **Output disable control**
- **Common data input and output**
- **18-pin standard dip**

PIN CONFIGURATION

F,N PACKAGE



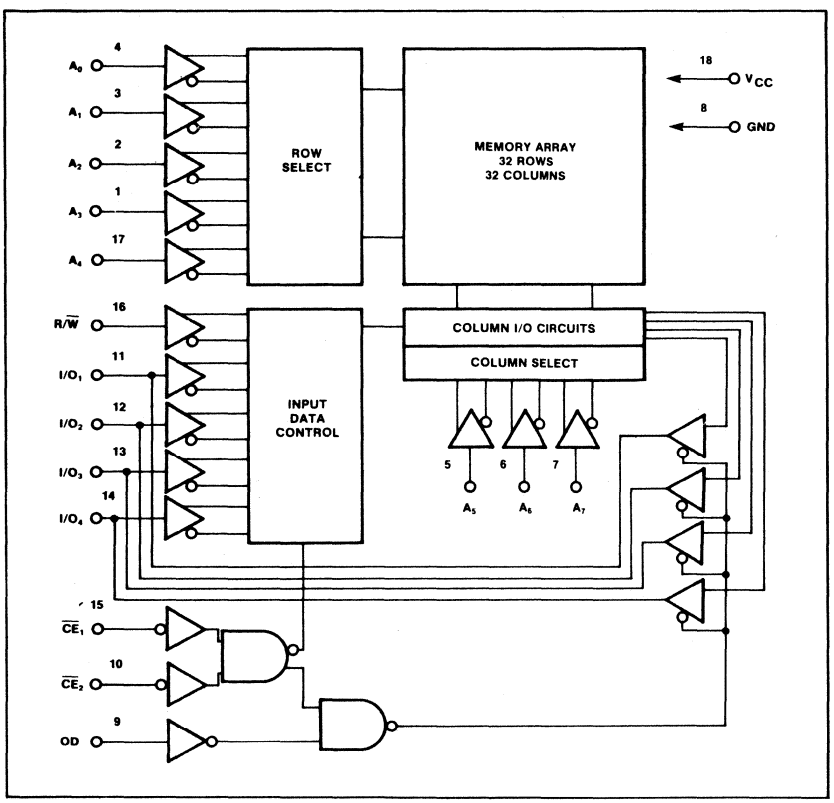
ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	−65 to 150	
P_D	Power dissipation	1	W
	Voltage on any pin with respect to ground	−0.5 to 7	V

NOTE

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified, Input pulse levels = .8V to 2.0V, Input pulse rise and fall times = 20ns, Timing measurement reference level = 1.5V, Output load = 1 TTL gate and C_L = 100pF

	PARAMETER	TO	FROM	2111A-4			2111A			2111A-2			UNIT
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	READ CYCLE												ns
t_{RC}	Read cycle			450			350			250			
t_A	Access time					450			350			250	
t_{CC}		Output	Chip enable			310			240			180	
t_{OD}		Output	Output disable			250			180			130	
t_{DF}		High Z state	Data output	0		200	0		150	0		150	
t_{OH}	Previous read data valid after change of address			40			40			40			
	WRITE CYCLE												ns
t_{WC}	Write cycle			450			350			250			
t_{AW}	Write delay			20			20			20			
t_{CW}		Write	Chip enable	250			200			150			
	Setup and hold time												ns
t_{DW}	Setup time	R/$\overline{W}$	Data	250			200			150			
t_{DH}	Hold time	Data	R/$\overline{W}$	0			0			0			
t_{DS}	Setup time	Output	Output disable	20			20			20			
t_{WP}	Write pulse			250			200			150			ns
t_{WR}	Write recovery			0			0			0			ns

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

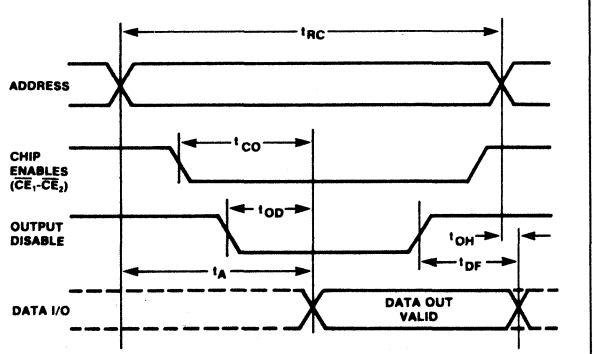
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low		−0.5		8	
V_{IH}	High		2.0		V_{CC}	
	Output voltage					V
V_{OL}	Low	I_{OL} = 2.0mA			0.45	
V_{OH}	High	I_{OH} = −200μA	2.4			
I_{LI}	Input load current	V_{IN} = 0 to 5.25V			10	μA
	I/O leakage current	$\overline{CE}_1 = \overline{CE}_2$ = 2.2V				μA
I_{LOH}		$V_{I/O}$ = 4.0V			10	
I_{LOL}		$V_{I/O}$ = 0.45V			−10	
	Supply current	V_{IN} = 5.25V, $I_{I/O}$ = 0mA				mA
I_{CC1}		T_A = 25°C		40	55	
I_{CC2}		T_A = 0°C			70	
	Capacitance[3]	T_A = 25°C, f = 1MHz				pF
C_{IN}	Input	V_{IN} = 0V		4	8	
$C_{I/O}$	I/O	$V_{I/O}$ = 0V		10	15	

NOTES

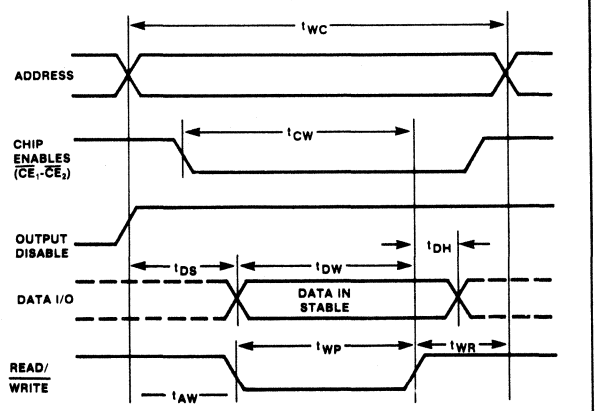
2. Typical values for T_A = 25°C and supply voltage.
3. This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE



2112-F,N • 2112-1-F,N • 2112-2-F,N

DESCRIPTION

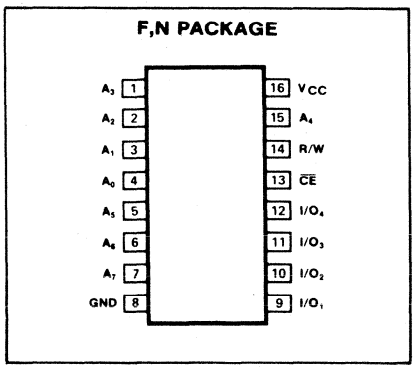
The 2112 series is high performance, low power static read/write RAMs.

The 2112 series is fabricated with n-channel silicon gate technology which allows the design of high performance easy to use MOS circuits and provides a high functional density on a given monolithic chip.

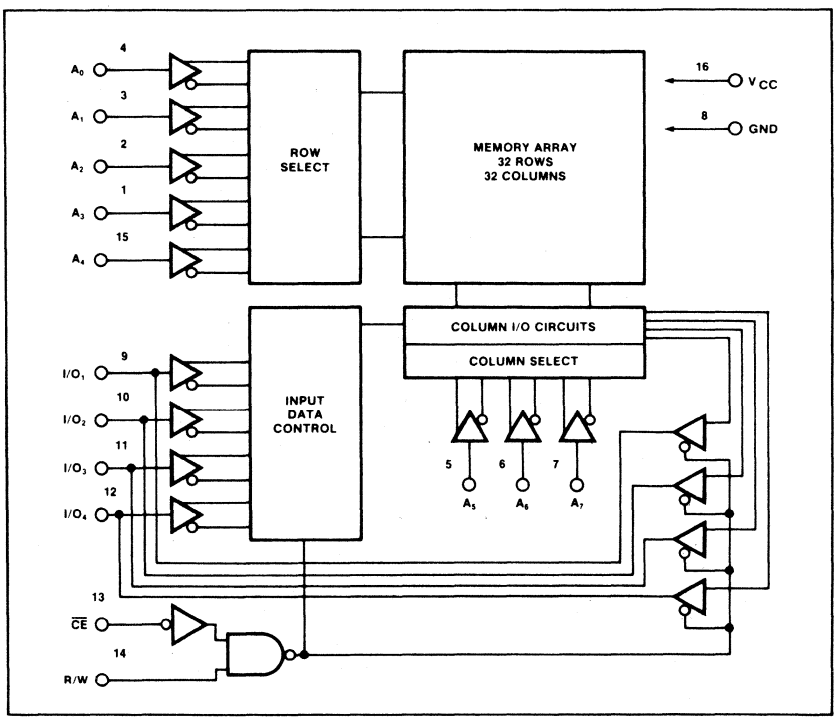
FEATURES

- **Fully static**
- **No refresh operations, sense amps or clocks required**
- **Directly TTL compatible**
- **One 5V power supply**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating under bias	0 to 70	
T_{STG}	Storage	-65 to 150	
	Voltage on any pin with respect to ground	-0.5 to 7	V
P_D	Power dissipation	1	W

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low		-0.5		0.65	
V_{IH}	High		2.2		V_{CC}	
	Output voltage					V
V_{OL}	Low	I_{OL} = 2mA			0.45	
V_{OH}	High	I_{OH} = -150μA	2.2			
I_{LI}	Input current	V_{IN} = 0 to 5.25V			10	μA
	I/O leakage current	$\overline{CE}$ = 2.2V				μA
I_{LOH}		$V_{I/O}$ = 4.0V			15	
I_{LOL}		$V_{I/O}$ = 0.45V			-50	
	Supply current	V_{IN} = 5.25V, $I_{I/O}$ = 0mA				mA
I_{CC1}		T_A = 25°C		30	60	
I_{CC2}		T_A = 0°C			70	
	Capacitance[3]	T_A = 25°C, f = 1MHz				pF
C_{IN}	Input (All pins)	V_{IN} = 0V		4	8	
$C_{I/O}$	I/O	$V_{I/O}$ = 0V		10	15	

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified, t_R and t_F = 20ns, V_{IN} = 0.65V to 2.2V, Timing reference = 1.5V, Load = 1 TTL gate and C_L = 100pF

PARAMETER		TO	FROM	2112			2112-1			2112-2			UNIT
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	READ CYCLE												
t_{RC}	Read cycle			1000			500			650			ns
t_A	Access time					1000			500			650	ns
t_{CO}		Output	Chip enable			800			150			500	ns
t_{CD}		Output disable	Chip enable	0		200	0		100	0		150	ns
t_{OH}	Previous read data valid after change of address			40			40			40			ns
	WRITE CYCLE #1												
t_{WC1}	Write cycle			850			500			500			ns
	Setup and hold time												ns
t_{AW1}	Setup time	Write	Address	150			100			100			
t_{DW1}	Setup time	R/W high	Data	650			250			280			
t_{CS1}	Setup time	$\overline{CE}$ low	R/W low	0			0			0			
t_{CH1}	Hold time	$\overline{CE}$ high	R/W high	0			0			0			
t_{DH1}	Hold time	Data	R/W high	100			50			50			
t_{CW1}	Setup time	R/W high	$\overline{CE}$ low	650			250			350			
t_{WP1}	Write pulse width			650			250			350			ns
t_{WR1}	Write recovery time			50			50			50			ns
	WRITE CYCLE #2												
t_{WC2}	Write cycle			1050			500			650			ns
	Setup and hold time												ns
t_{AW2}	Setup time	Write	Address	150			100			100			
t_{DW2}	Setup time	R/W high	Data	650			250			280			
t_{CS2}	Setup time	$\overline{CE}$ low	R/W low	0			0			0			
t_{CH2}	Hold time	$\overline{CE}$ high	R/W high	0			0			0			
t_{DH2}	Hold time	Data	R/W high	100			50			50			
t_{WD2}	Disable time	R/W high	Data	200			200			200			ns
t_{WR2}	Write recovery time			50			50			50			ns

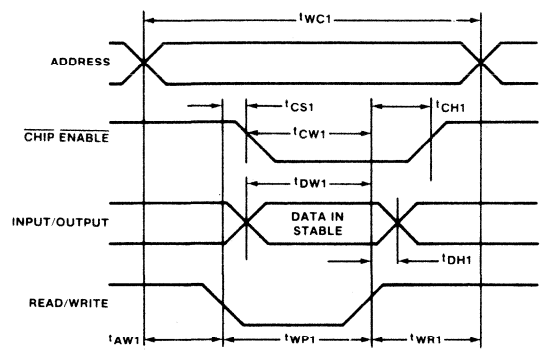
NOTES on following page.

NOTES

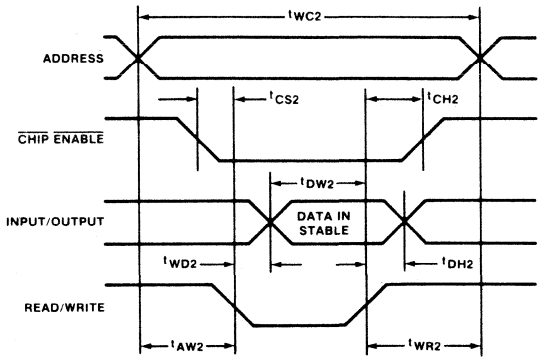
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values are for T_A = 25°C and typical supply voltage.
3. This parameter is periodically sampled and is not 100% tested.
4. Output is enabled and t_{CO} commences only with both CE low and WE high.
5. Output is disabled and t_{DF} combined from either the rising edge of CE or the falling edge of WE.
6. Minimum t_{WP} is valid when CE has been high at least t_{DF} before WE goes low. Oherwise $t_{WP(min)} = t_{DW(min)} + t_{DF(max)}$.
7. When WE goes high at the end of the write cycle, it will be possible to turn on the output buffers if CE is still low. The data out will be the same as the data just written and so will not conflict with input data that may still be on the I/O bus.

VOLTAGE WAVEFORMS

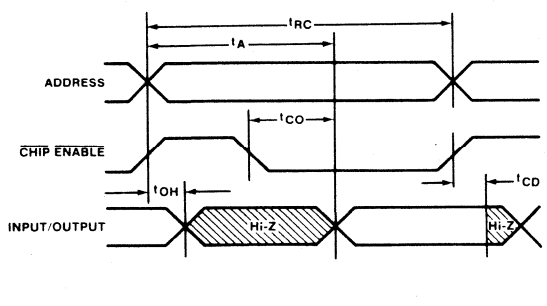
WRITE CYCLE #1



WRITE CYCLE #2



READ CYCLE



DESCRIPTION

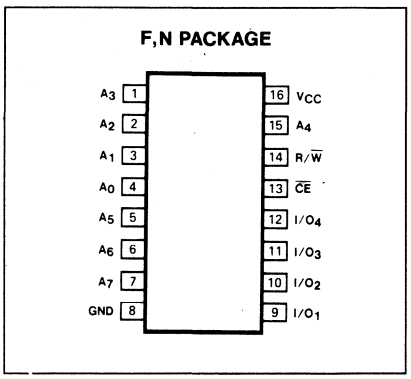
The 2112 series is a family of high performance, low power static read/write RAM's.

The 2112 series is fabricated with n-channel silicon gate technology which allows the design of high performance, easy-to-use MOS circuits and provides a high functional density on a given monolithic chip.

FEATURES

- **Fully static**
- **No refresh operations, sense amps or clocks required**
- **Directly TTL compatible**
- **Single 5V power supply**
- **16-pin standard dip**
- **Bus oriented I/O data**

PIN CONFIGURATION



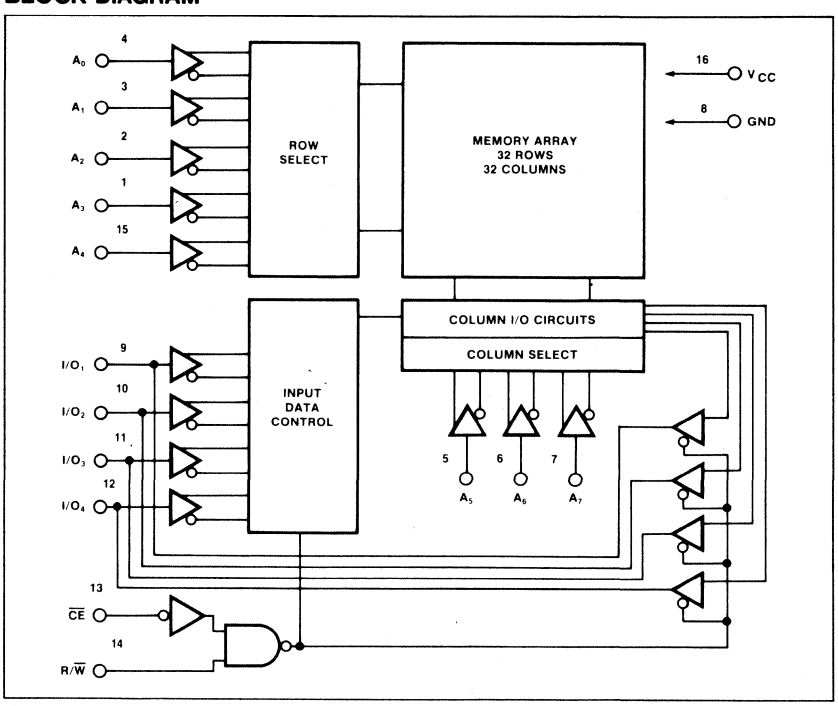
ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	−65 to 150	
P_D	Power dissipation	1	W
	Voltage on any pin with respect to ground	−0.5 to 7	V

NOTE

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

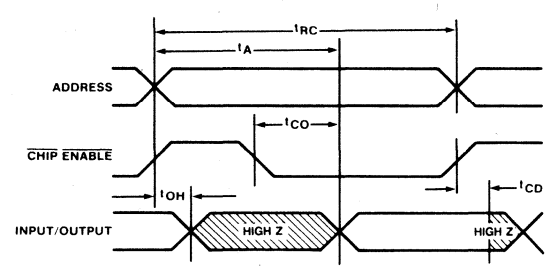
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low		−0.5		.8	
V_{IH}	High		2.0		V_{CC}	
	Output voltage					V
V_{OL}	Low	I_{OL} = 2.0mA			.45	
V_{OH}	High	I_{OH} = −200μA	2.4			
I_{LI}	Input current	V_{IN} = 5.25V, $I_{I/O}$ = 0mA			10	μA
	I/O leakage current	$\overline{CE}$ = 2.0V				
I_{LOH}		$V_{I/O}$ = 4.0V			10	
I_{LOL}		$V_{I/O}$ = 0.45V			−10	
	Supply current	V_{IN} = 5.25V, $I_{I/O}$ = 0mA				mA
I_{CC1}		T_A = 25°C		40	55	
I_{CC2}		T_A = 0°C			70	
	Capacitance[3]	T_A = 25°C, f = 1MHz				pF
C_{IN}		V_{IN} = 0V		4	8	
$C_{I/O}$		$V_{I/O}$ = 0V		10	15	

NOTES

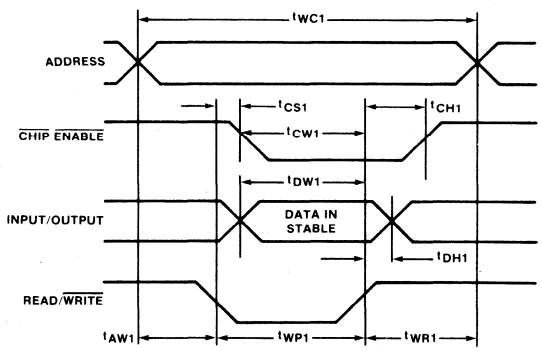
2. Typical values are for T_A = 25°C and typical supply voltage.
3. This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAMS

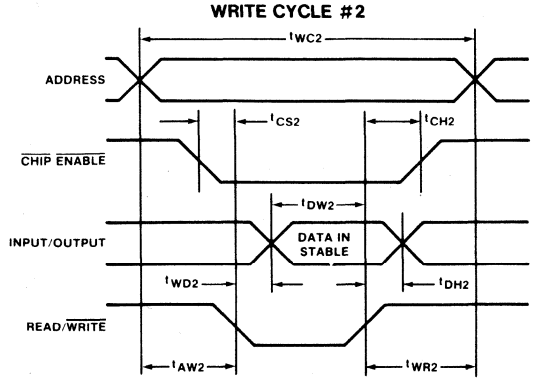
READ CYCLE



WRITE CYCLE #1



WRITE CYCLE #2



AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified, t_R and t_F = 20ns, V_{IN} = .8V to 2.0V, Timing reference = 1.5V, Load = 1 TTL gate and C_L = 100pF

PARAMETER		TO	FROM	2112A-4			2112A			2112A-2			UNIT
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	READ CYCLE[4,5]												ns
t_{RC}	Read cycle			450			250			250			
t_A	Access time					450			350			250	
t_{CO}		Output	Chip enable			310			240			150	
t_{CD}		Output disable	Chip enable	0		260	0		200	0		150	
t_{OH}	Previous read data valid after change of address			40			40			40			
	WRITE CYCLE 1[6,7]												
t_{WC1}	Write cycle			450			350			250			ns
	Setup and hold time												ns
t_{AW1}	Setup time	Write	Address	20			20			20			
t_{DW1}	Setup time	R/$\overline{W}$ high	Data	300			250			180			
t_{CS1}	Setup time	$\overline{CE}$ low	R/$\overline{W}$ low	0			0			0			
t_{CH1}	Hold time	$\overline{CE}$ high	R/$\overline{W}$ high	0			0			0			
t_{DH1}	Hold time	Data	R/$\overline{W}$ high	0			0			0			
t_{CW1}	Setup time	R/$\overline{W}$ high	$\overline{CE}$ low	300			250			180			
t_{WP1}	Write pulse width			300			250			180			ns
t_{WR1}	Write recovery time			0			0			0			
	WRITE CYCLE 2[7]												
t_{WC2}	Write cycle			580			470			320			ns
	Setup and hold time												ns
t_{AW2}	Setup time	Write	Address	20			20			20			
t_{DW2}	Setup time	R/$\overline{W}$ high	Data	300			250			180			
t_{CS2}	Setup time	$\overline{CE}$ low	R/$\overline{W}$ low	0			0			0			
t_{CH2}	Hold time	$\overline{CE}$ high	R/$\overline{W}$ high	0			0			0			
t_{DH2}	Hold time	Data	R/$\overline{W}$ high	0			0			0			
t_{WD2}	Disable time	R/$\overline{W}$ high	Data	260			200			120			ns
t_{WR2}	Write recovery time			0			0			0			

NOTES

4. Output is enabled and t_{CO} commences only with both $\overline{CE}$ low and R/$\overline{W}$ high.
5. Output is disabled and t_{CD} combined from either the rising edge of $\overline{CE}$ or the falling edge of R/$\overline{W}$.
6. Minimum t_{WP} is valid when $\overline{CE}$ has been high at least t_{CD} before R/$\overline{W}$ goes low. Otherwise $t_{WP(min)} = t_{DW(min)} + t_{CD(max)}$.
7. When R/$\overline{W}$ goes high at the end of the write cycle, it will be possible to turn on the output buffers if $\overline{CE}$ is still low. The data out will be the same as the data just written and so will not conflict with input data that may still be on the I/O bus.

2606-F,I,N • 2606-1-F,I,N

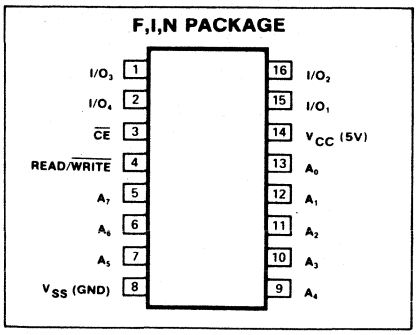
DESCRIPTION

The 2606 is fabricated with n-channel silicon gate MOS technology and achieves an access time of less than 750ns.

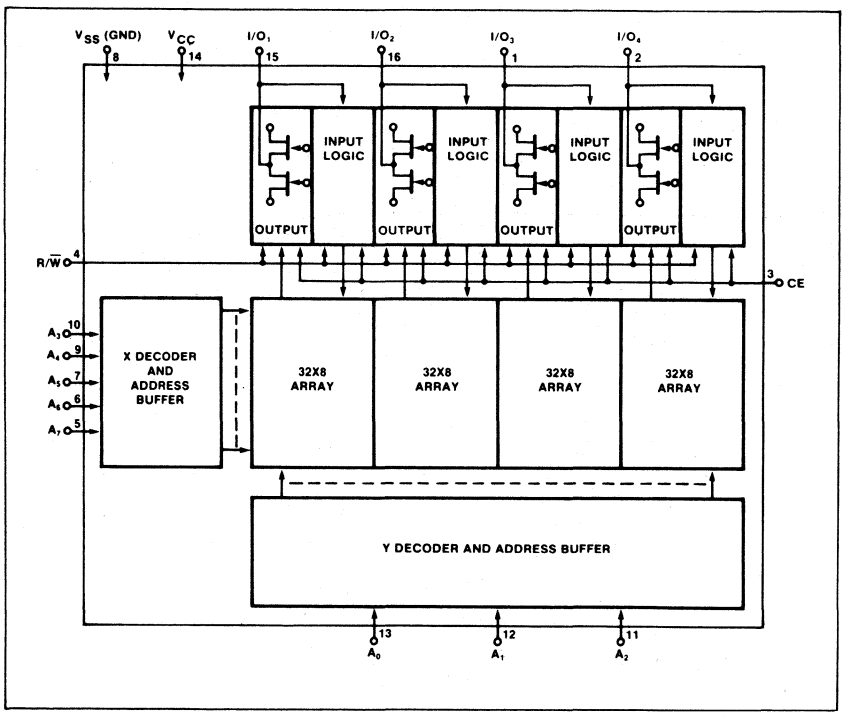
FEATURES

- **Fully decoded**
- **No clocks required**
- **All interface signals, including power supply directly TTL compatible**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating under bias	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation	1	W
	Voltage on any pin with respect to ground	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low		-0.5		0.65	
V_{IH}	High		2.2		V_{CC}	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.9mA			0.45	
V_{OH}	High	I_{OH} = -100μA	2.4			
I_{LI}	Input current	V_{IN} = 0 to 5.25V			10	μA
	I/O leakage current	$\overline{CE}$ = 2.2V				μA
I_{LOH}		$V_{I/O}$ = 4.0V			10	
I_{LOL}		$V_{I/O}$ = 0.45V			-100	
	Supply current	V_{IN} = 5.25V, $I_{I/O}$ = OmA				mA
I_{CC1}		T_A = 25°C			70	
I_{CC2}		T_A = 0°C			80	
	Capacitance[3]	T_A = 25°C, f = 1MHz				pF
C_{IN}	Input (All pins)	V_{IN} = OV		4	7	
$C_{I/O}$	I/O	V_{OUT} =OV		7	10	

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C, V_{CC} = 5V ± 5% unless other specified.[4,5,6,7]

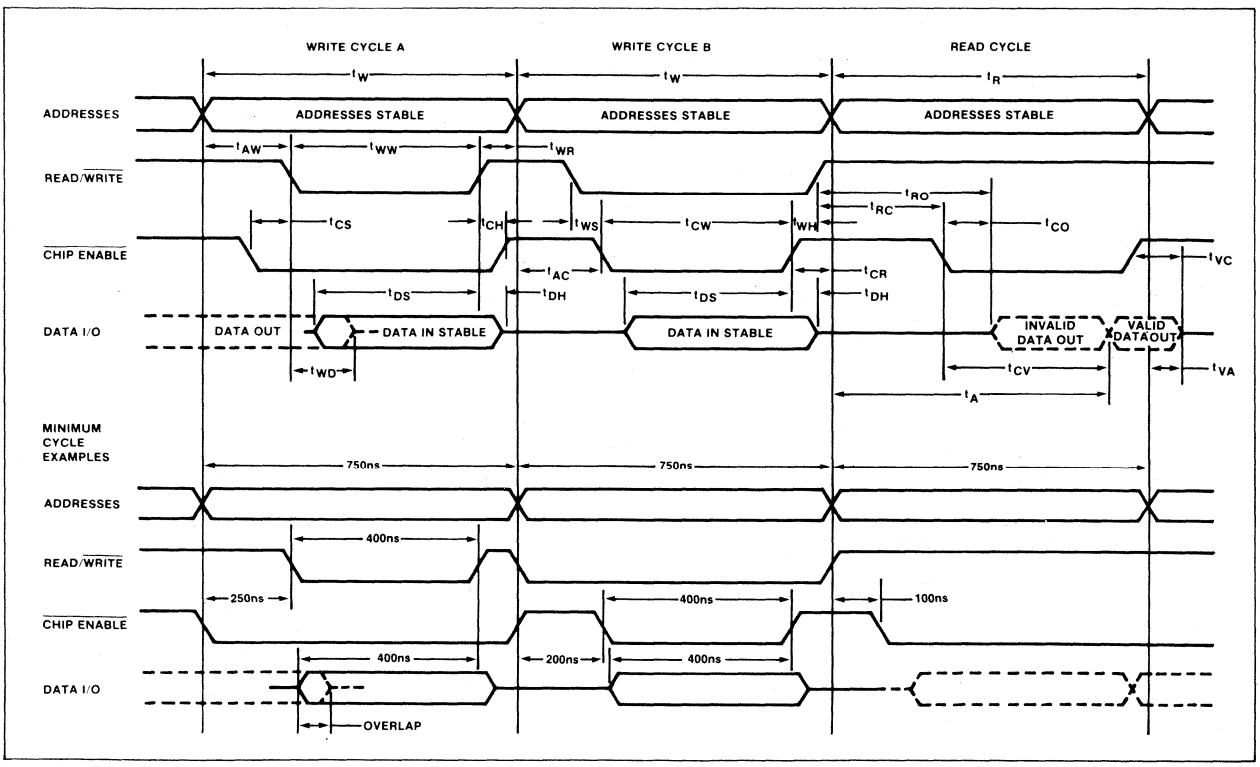
PARAMETER		TO	FROM	2606			2606-1			UNIT
				Min	Typ	Max	Min	Typ	Max	
	READ CYCLE									
t_R	Read cycle time			750			500			ns
t_A	Access time					750			500	ns
T_{RO}[8]		Output enable	Read	100			75			ns
t_{CO}[8]		Output enable	Chip enable	0			0			ns
	Previous data valid with respect to									ns
t_{VC}	Chip disable			0		150	0		100	
t_{VA}	Address change			50			50			
t_{CV}	Delay time	Data valid	Chip enable			400			300	ns
t_{RC}		Chip enable	Read	100			50			ns
	WRITE CYCLE A									
t_W	Write cycle time			750			500			ns
t_{AW}		Write	Address	250			150			ns
t_{WW}	Write pulse width			400			300			ns
t_{WR}	Write recovery time			100			50			ns
	Setup and hold time									ns
t_{CS}	Setup time	R/W	Chip enable	0			0			
t_{CH}	Hold time	Chip enable	R/W							
t_{DS}	Setup time	R/W	Data	380			280			
t_{DH}	Hold time[9]	Data	R/W	0			0			
t_{WD}	Disable delay[10]	Data out	Write			125			100	ns
	WRITE CYCLE B									
t_W	Write cycle time			750			500			ns
t_{AC}		Chip enable	Address	250			150			ns
t_{CW}	Chip enable pulse width			400			300			ns
t_{CR}	Chip enable recovery time			100			50			ns
	Setup and hold time[11]									ns
t_{WS}	Setup time	Chip enable	R/W	200			100			
t_{WH}	Hold time	R/W	Chip enable	0			0			
t_{DS}	Setup time	Chip enable	Data	380			280			
t_{DH}	Hold time[8]	Data	Chip enable	0			0			

NOTES on following page.

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values are for T_A = 25°C and typical supply voltage.
3. This parameter is periodically sampled and is not 100% tested.
4. Input levels swing between 0.65V and 2.2V.
5. Input signal transition times are 20ns.
6. Timing reference level is 1.5V.
7. Bus load is 100pF, 1 TTL tri-state output.
8. R/$\overline{W}$ must be high and CE must be low in order for output buffers to turn on.
9. Maximum t_{DH} governed by potential conflict with data out during next cycle.
10. The output buffers will turn off within the specified time after write mode is selected.
11. Write setup required to prevent data overlap. For write cycle B the R/$\overline{W}$ line will typically change with the addresses.

TIMING DIAGRAM



2102-F,I,N • 2102-1-F,I,N • 2102-2-F,I,N

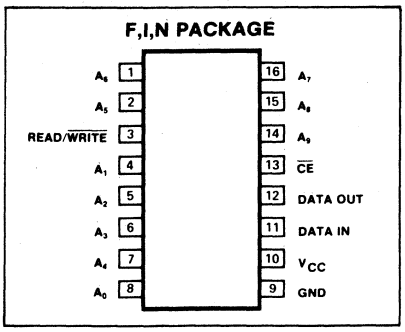
DESCRIPTION

The 2102, 2102-1 and 2102-2 are static random access read/write memories fabricated with low threshold n-channel silicon gate technology.

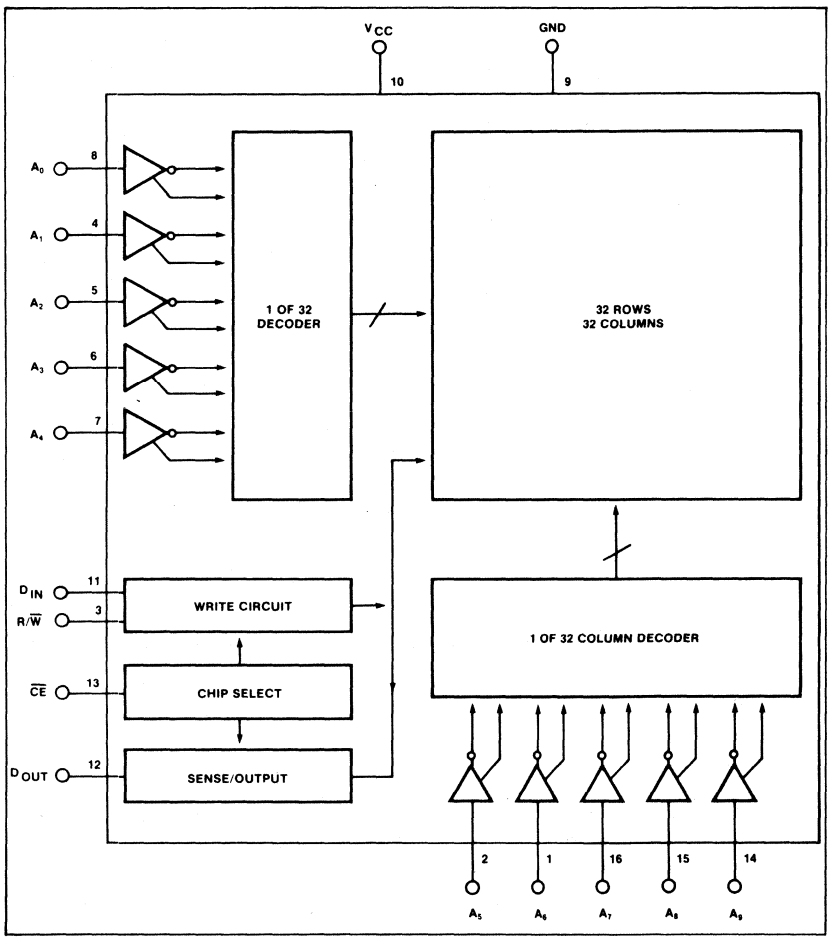
FEATURES

- **Fully static**
- **Require no clocks**
- **Completely DTL/TTL compatible**
- **Single 5V power supply**
- **Three-state output for OR-tie capability**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation[2]		
	N package	640	mW
	F package	1	W
	I package	1	W
	All input, output and supply voltages with respect to ground	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ[1]	Max	
Input voltage					V
V_{IL} Low		-0.5		0.65	
V_{IH} High		2.2		V_{CC}	
Output voltage					V
V_{OL} Low	I_{OL} = 1.9mA			0.45	
V_{OH} High	I_{OH} = -100μA	2.2			
I_{LI} Input load current (All input pins)	V_{IN} = 0 to 5.25V			10	μA
Leakage current	$\overline{CE}$ = 2.2V				μA
I_{LOH}	V_{OUT} = 4.0V			10	
I_{LOL}	V_{OUT} = 0.45V			-100	
Supply current	All inputs = 5.25V, Data out open				mA
I_{CC1}	T_A = 25°C		30	60	
I_{CC2}	T_A = 0°C			70	

AC ELECTRICAL CHARACTERISTICS

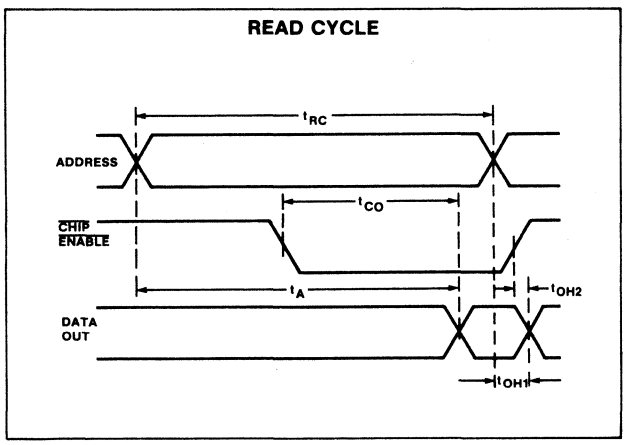
T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified.

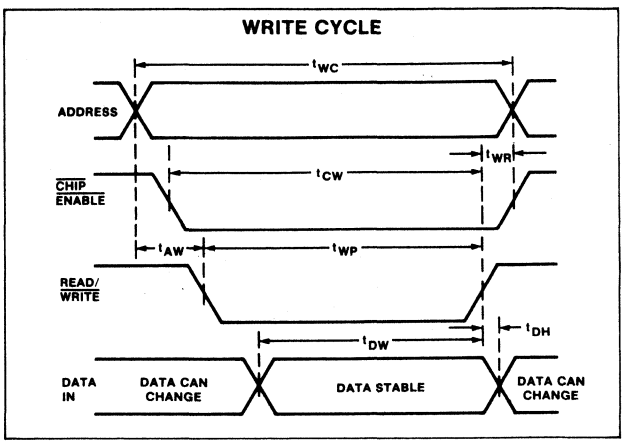
PARAMETER	TO	FROM	2102			2102-1			2102-2			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
READ CYCLE												
t_{RC} Read cycle			1,000			500			650			ns
t_A Access time					1,000			500			650	ns
t_{CO}	Output	Chip enable			500			350			400	ns
Previous data valid with respect to												ns
t_{OH1} Address			50			50			50			
t_{OH2} Chip enable			0			0			0			
WRITE CYCLE												
t_{WC} Write cycle			1,000			500			650			ns
t_{WP} Write pulse width			750			300			400			ns
t_{WR} Write recovery time			50			50			50			ns
Setup and hold time												ns
t_{AW} Setup time	Write	Address	200			150			200			
t_{DW} Setup time	Rise of R/$\overline{W}$	Data in	800			330			450			
t_{DH} Hold time	Change of data in	Rise of R/$\overline{W}$	100			100			100			
t_{CW} Setup time	Write	Chip enable	900			400			550			

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device of these or any other condition above those indicated in the operation of the device of these or any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient ("B" package).
3. All inputs protected against static charge.
4. Parameter valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and typical supply voltages.

TIMING DIAGRAMS





DESCRIPTION

The 2102A is a high speed static random access memory element using n-channel MOS devices integrated on a monolithic array. It uses fully dc stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The 2102A is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. A low standby power version (2102AL) is also available, and has all the same operating characteristics of the 2102A with the added feature of 35mW maximum power dissipation in standby and 174mW in operations.

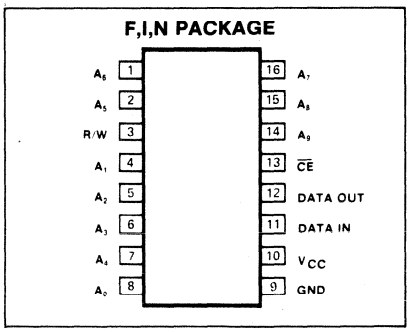
A separate chip enable ($\overline{CE}$) lead allows easy selction of an individual package when outputs are OR-tied.

The 2102A is fabricated with n-channel silicon gate technology, which allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or p-channel silicon gate technology.

FEATURES

- **Single 5V supply voltage**
- **Fully TTL compatible**
- **Standby power mode (2102AL)**
- **Tri-state output**
- **OR-tie capability**
- **All inputs protected against static charge**
- **Low cost packaging**

PIN CONFIGURATION



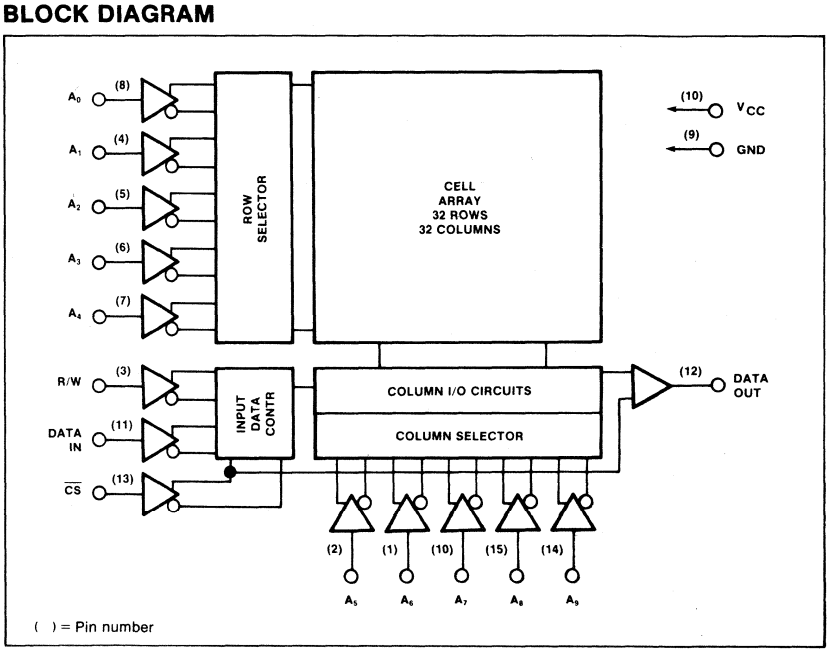
PIN DESIGNATION

PIN NO.	SYMBOL	FUNCTION	TYPE
11	D_{IN}	Data input	
1,2,4-8,14,16	A_0-A_9	Address inputs	
3	R/W	Read/write input	
13	$\overline{CE}$	Chip enable	
12	D_{OUT}	Data output	
10	V_{CC}	Power (5V)	
9	GND	Ground	

TRUTH TABLE

$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	High Z	Not selected
L	L	L	L	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{OUT}	Read

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating under bias	-10 to 80	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation	1	W
	Voltage on any pin with respect to ground	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	2102A/2102A-4/ 2102AL/2102AL-4			2102A-2/ 2102AL-2			2102A-6			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage											V
V_{IL}	Low		-0.5		0.8	-0.5		0.8	-0.5		0.65	
V_{IH}	High		2.0		V_{CC}	2.0		V_{CC}	2.2		V_{CC}	
	Output voltage											V
V_{OL}	Low	$I_{OL} = 2.1mA$			0.4			0.4			0.45	
V_{OH}	High	$I_{OH} = -100\mu A$	2.4			2.4			2.2			
I_{LI}	Input load current	$V_{IN} = 0$ to 5.25V		1	10		1	10		1	10	μA
	Output leakage current	$\overline{CE} = 2.0V$										μA
I_{LOH}		$V_{OUT} = V_{OH}$		1	5		1	5		1	5	
I_{LOL}		$V_{OUT} = 0.4V$		-1	-10		-1	-10		-1	-10	
I_{CC}	Supply current[3]	Data out open, $T_A = 0°C$		33			33			33	55	mA
	Capacitance[4]											pF
C_{IN}	Input (All pins)	$V_{IN} = 0V$		3	5		3	5		3	5	
C_{OUT}	Output	$V_{OUT} = 0V$		7	10		7	10		7	10	

STANDBY CHARACTERISTICS

$T_A = 0°C$ to $70°C$

PARAMETER		TEST CONDITIONS	2102AL, 2102AL-4			2102AL-2			UNIT
			Min	Typ[5]	Max	Min	Typ[5]	Max	
V_{PD}	V_{CC} in standby		1.5			1.5			V
V_{CES}	$\overline{CE}$ bias in standby[6]	$2.0V \le V_{PD} \le V_{CC}$ max	2.0			2.0			V
		$1.5V \le V_{PD} < 2.0V$	V_{PD}			V_{PD}			
	Standby current								mA
I_{PD1}		All inputs = $V_{PD1} = 1.5V$		15	23		20	28	
I_{PD2}		All inputs = $V_{PD2} = 2.0V$		20	30		25	38	
t_{CP}	Chip deselect to standby time		0			0			ns
t_R	Standby recovery time[7]		t_{RC}			t_{RC}			ns

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise noted,
Input pulse levels = 0.8V to 2.0V, Input rise and fall times = 10ns,
Timing measurement reference level inputs = 1.5V
Output = 0.8V and 2.0V, Output load = 1 TTL gate and C_L = 100pF

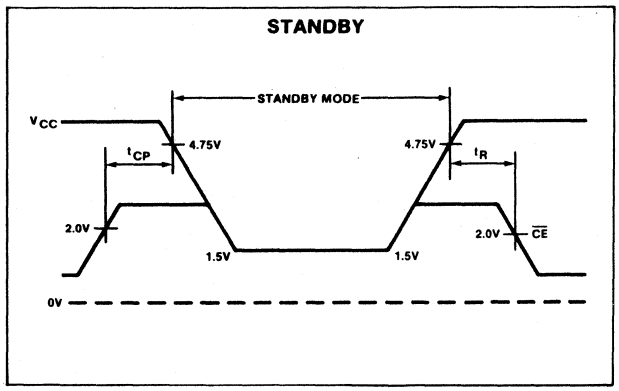
PARAMETER		TO	FROM	2102A-2, 2102AL-2			2102A, 2102AL			UNIT
				Min	Typ	Max	Min	Typ	Max	
	READ CYCLE									
t_{RC}	Read cycle			250			350			ns
t_A	Access time					250			350	ns
t_{CO}		Output time	Chip enable			130			180	ns
	Previous read data valid with respect to									ns
t_{OH1}	Address			40			40			
t_{OH2}	Chip enable			0			0			
	WRITE CYCLE									
t_{WC}	Write cycle			250			350			ns
t_{WP}	Write pulse width			180			250			ns
t_{WR}	Write recovery time			0			0			ns
	Setup and hold time									ns
t_{AW}	Setup time	Write	Address	20			20			
t_{DW}	Setup time	R/W	Data	180			250			
t_{DH}	Hold time	Output	Data	0			0			
t_{CW}	Setup time	Data	R/W	180			250			

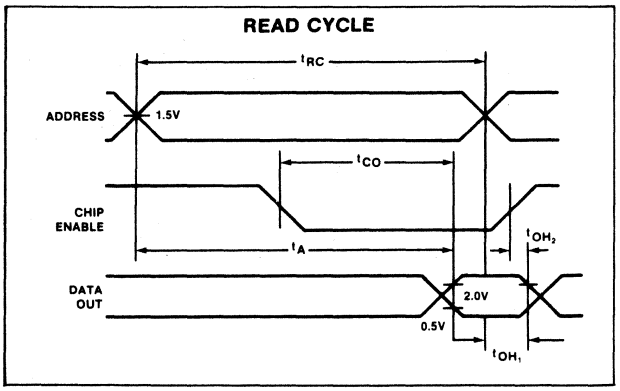
PARAMETER		TO	FROM	2102A-4, 2102AL-4			2102A-6			UNIT
				Min	Typ	Max	Min	Typ	Max	
	READ CYCLE									
t_{RC}	Read cycle			450			650			ns
t_A	Access time					450			650	ns
t_{CO}		Output time	Chip enable			230			400	ns
	Previous read data valid with respect to									ns
t_{OH1}	Address			40			50			
t_{OH2}	Chip enable			0			0			
	WRITE CYCLE									
t_{WC}	Write cycle			450			650			ns
t_{WP}	Write pulse width			300			400			ns
t_{WR}	Write recovery time			0			50			ns
	Setup and hold time									ns
t_{AW}	Setup time	Write	Address	20			200			
t_{DW}	Setup time	R/W	Data	300			450			
t_{DH}	Hold time	Output	Data	0			20			
t_{CW}	Setup time	Data	R/W	300			550			

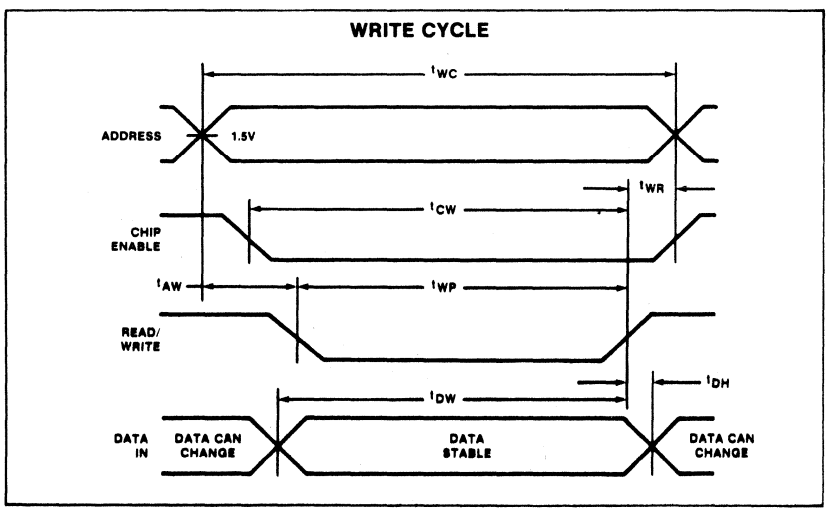
NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values are for T_A = 25°C and typical supply voltage.
3. The maximum I_{CC} value is the 55mA for the 2102A and 2102A-4, and 33mA for the 2102AL, 2102AL-2, and 2102AL-4, and 65mA for 2102A-2.
4. This parameter is periodically sampled and is not 100% tested.
5. Typical values are for T_A = 25°C.
6. Consider the test conditions as shown: if the standby voltage (V_{PD}) is between 5.25V (V_{CC} max) and 2.0V, then $\overline{CE}$ must be held at 2.0V min (V_{IH}). If the standby voltage is less than 2.0V but greater than 1.5V (V_{PD} min), then $\overline{CE}$ and standby voltage must be at least the same value or, if they are different, $\overline{CE}$ must be the more positive of the 2.
7. $t_R = t_{RC}$ (read cycle time).

VOLTAGE WAVEFORMS







21F02-F,I,N • 21F02-2 - F,I,N • 21F02-4 - F,I,N

DESCRIPTION

The 21F02 is a high speed static random access memory element using n-channel MOS devices integrated on a monolithic array. It uses fully dc stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

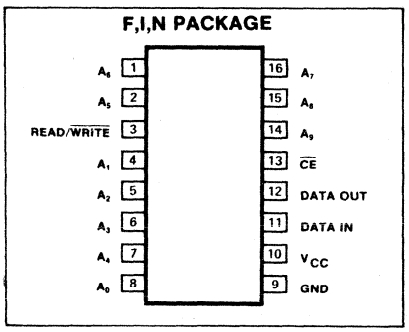
The 21F02 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. A separate chip enable (CE) lead allows easy selection of an individual package when outputs are OR-tied.

The Signetics 21F02 is fabricated with n-channel silicon gate technology. This technology allows the design and production of high performance easy to use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or p-channel silicon gate technology.

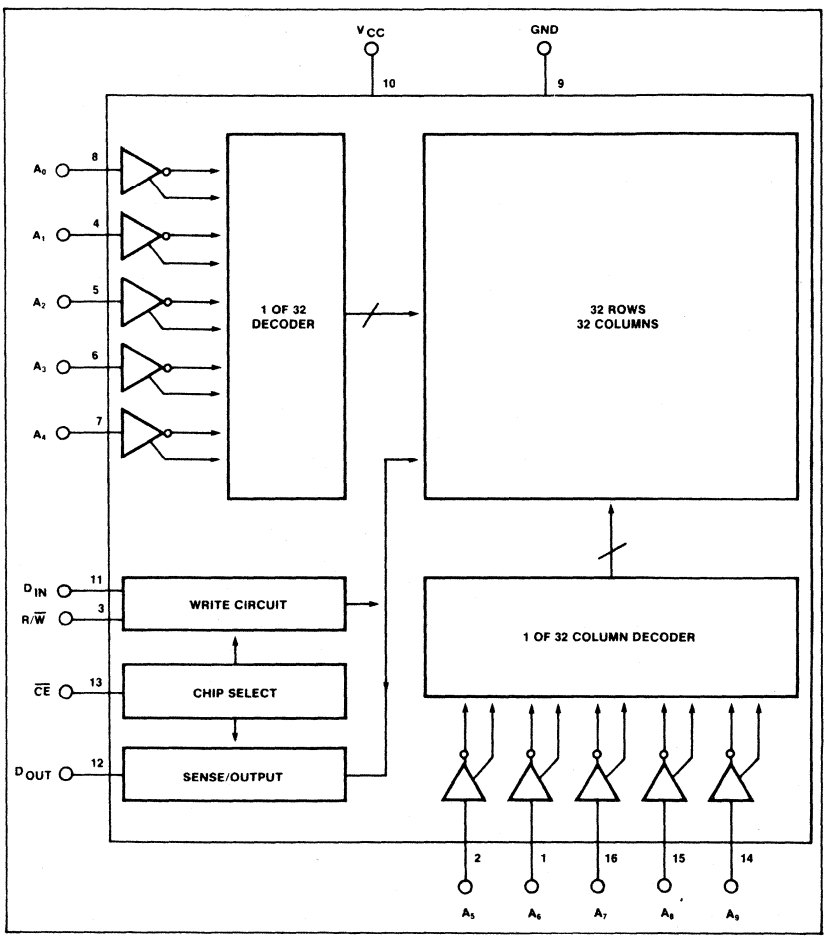
FEATURES

- **Fully TTL compatible**
- **Single 5V supply**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation[2]		
	N package	640	mW
	F package	1	W
	I package	1	W
	All input, output and supply voltages with respect to ground	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
	Input voltage					V
V_{IL}	Low		-0.5		0.8	
V_{IH}	High		2.0		V_{CC}	
	Output voltage					V
V_{OL}	Low	I_{OL} = 2.1mA			0.4	
V_{OH}	High	I_{OH} = -100μA	2.4			
I_{LI}	Input load current (All input pins)	V_{IN} = 0 to 5.25V			10	μA
	Output leakage current	$\overline{CE}$ = 2.0V				μA
I_{LOH}		V_{OUT} = 2.4 to V_{CC}			5	
I_{LOL}		V_{OUT} = 0.4V			-10	
	Supply current	All inputs = 5.25V, Data out open				mA
I_{CC1}		T_A = 25°C		30	60	
I_{CC2}		T_A = 0°C			70	

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified,
Input pulse levels = 0.65 to 2.2V, Input pulse rise and fall times = 20ns,
Timing measurement reference level = 1.5V,
Output load = 1 TTL gate and C_L = 100pF

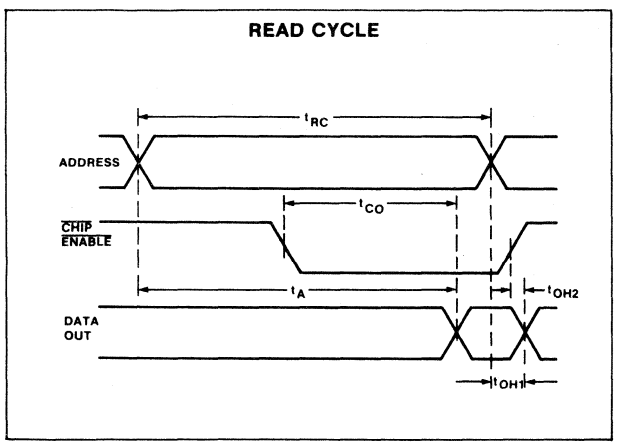
PARAMETER		TO	FROM	21F02			21F02-2			21F02-4			UNIT
				Min	Typ[3]	Max	Min	Typ[3]	Max	Min	Typ[3]	Max	
	READ CYCLE												
t_{RC}	Read cycle			350			250			450			ns
t_A	Access time					350			250			450	ns
t_{CO}		Output time	Chip enable			180			130			230	ns
	Previous read data valid with respect to												ns
t_{OH1}	Address			40			40			40			
t_{OH2}	Chip enable			0			0			0			
	WRITE CYCLE												
t_{WC}	Write cycle			350			250			450			ns
t_{WP}	Write pulse width			250			180			300			ns
t_{WR}	Write recovery time			20			20			20			ns
	Setup and hold time												ns
t_{AW}	Setup time	Write	Address	20			20			20			
t_{DW}	Setup time	Output	Data	250			180			300			
t_{DH}	Hold time	Output	Data	0			0			0			
t_{CW}	Setup time	Write	Chip enable	250			180			300			

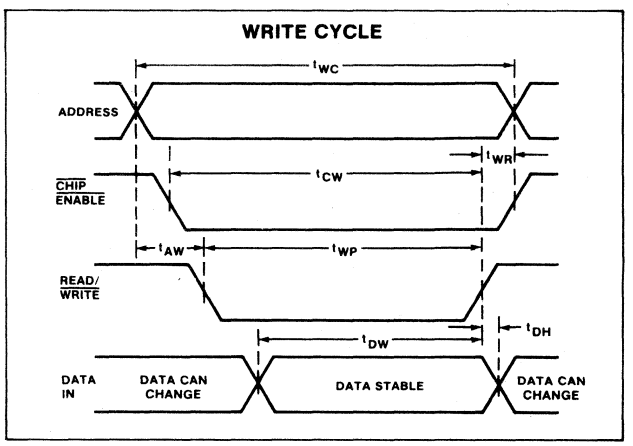
NOTES on following page.

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device of these or any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient (B package).
3. Typical values are at +25°C and typical supply voltages.
4. All inputs protected against static charge.
5. Parameter valid over operating temperature range unless otherwise specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserves the right to make design and process changes and improvements.

TIMING DIAGRAMS





21L02-F,I,N • 21L02-1-F,I,N • 21L02-2-F,I,N • 21L02-3-F,I,N

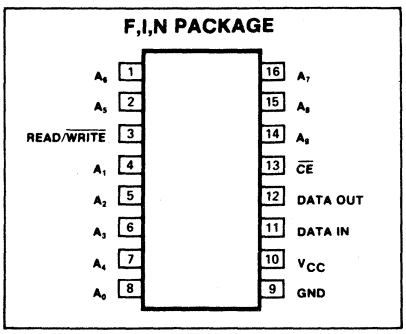
DESCRIPTION

The 21L02, 21L02-1, 21L02-2, and 21L02-3 are low power static random access read/write memories fabricated with low threshold n-channel silicon gate technology.

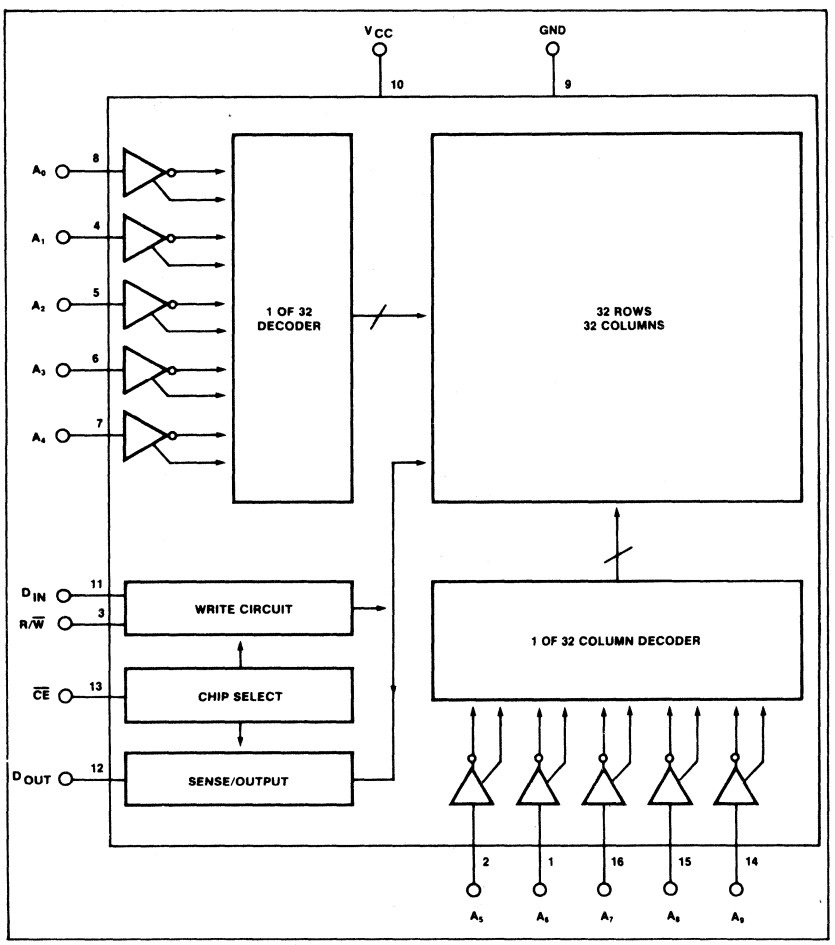
FEATURES

- **Fully static**
- **Requires no clocks**
- **Completely DTL/TTL compatible**
- **Single 5V power supply**
- **Three-state output for OR-tie capability**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation[2]		
	N package	640	mW
	F package	1	W
	I package	1	W
	All input, output and supply voltages with respect to ground	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
	Input voltage					V
V_{IL}	Low		-0.5		0.65	
V_{IH}	High		2.2		V_{CC}	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.9mA			0.45	
V_{OH}	High	I_{OH} = -100μA	2.2			
I_{LI}	Input load current (All input pins)	V_{IN} = 0 to 5.25V			10	μA
	Output leakage current	$\overline{CE}$ = 2.2V				μA
I_{LOH}		V_{OUT} = 4.0V			10	
I_{LOL}		V_{OUT} = 0.45V			-100	
	Supply current	All inputs = 5.25V, Data out open				mA
I_{CC1}		T_A = 25°C		30	40	
I_{CC2}		T_A = 0°C			40	

AC ELECTRICAL CHARACTERISTICS

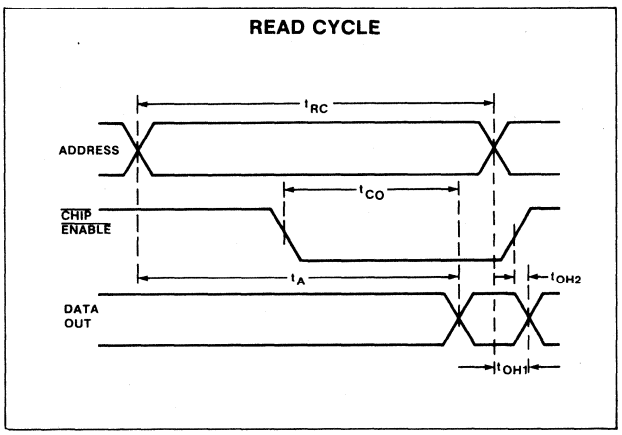
T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified,
Input pulse levels = 0.65V to 2.2V, Input pulse rise and fall times = 20ns,
Timing measurement reference level = 1.5V, Output load = 1 TTL gate
and C_L = 100pF

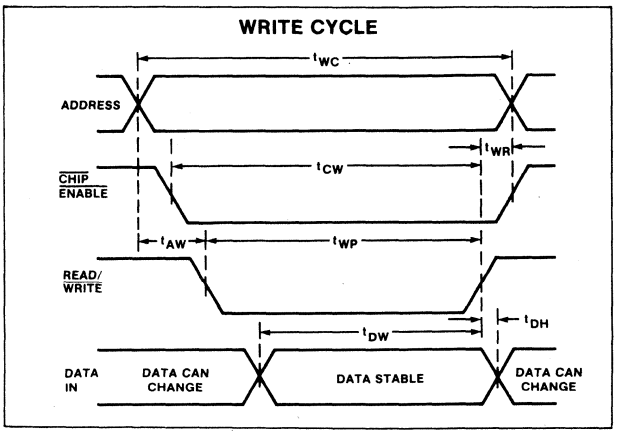
PARAMETER		TO	FROM	21L02			21L02-1			21L02-2			21L02-3			UNIT
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	READ CYCLE															
t_{RC}	Read cycle			1,000			500			650			400			ns
t_A	Access time					1,000			500			650		400		ns
t_{CO}		Output time	Chip enable			500			350			400		300		ns
	Previous read data valid with respect to															ns
t_{OH1}	Address			50			50			50			50			
t_{OH2}	Chip enable			0			0			0			0			
	WRITE CYCLE															
t_{WC}	Write cycle			1,000			500			650			400			ns
t_{WP}	Write pulse width			750			300			400			250			ns
T_{WR}	Write recovery time			50			50			50			50			ns
	Setup and hold time															ns
t_{AW}	Setup time	Write	Address	200			150			200			100			
t_{DW}	Setup time	Rise of R/$\overline{W}$	Data in	800			330			450			300			
t_{DH}	Hold time	Change of data in	Rise of R/$\overline{W}$	100			100			100			50			
t_{CW}	Setup time	Write	Chip enable	900			400			550			300			

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device of these or any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient (B package).
3. Typical values are at +25°C and typical supply voltages.
4. All inputs protected against static charge.
5. Parameter valid over operating temperature range unless otherwise specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserves the right to make design and process changes and improvements.

TIMING DIAGRAMS





MILITARY

MILITARY PRODUCTS/ PROCESS LEVELS

The Signetics MIL 38510/883 Program is organized to provide a broad selection of processing options, structured around the most commonly requested customer flows. The program is designed to provide our customers:

- Fully compliant 883 flows on all products.
- Standard processing flows to help minimize the need for custom specs.
- Cost savings realized by using standard processing flows in lieu of custom flows.
- Better delivery lead times by minimizing spec negotiation time, plus allows customer to buy product off-the-shelf or in various stages of production rather than waiting for devices started specifically to custom specs.

The following explains the different processing options available to you. Special device marking clearly distinguishes the type of screening performed. Refer to Tables 2, 3, 4 and 5.

JAN CASE OUTLINE AND LEAD FINISH	SIGNETICS MILITARY PACKAGE TYPES				
			DUAL-IN-LINE		
	8-PIN	10-PIN	14-PIN	16-PIN	24-PIN
CB	—	—	F	—	—
EB	—	—	—	F	—
JB	—	—	—	—	F
DB	—	—	W	—	—
FB	—	—	—	W	—
ZC	—	—	—	—	Q
GC	T	—	—	—	—
IC	—	K	—	—	—

All products listed are also available in Die form.

Table 1 MILITARY PACKAGE AVAILABILITY

	JB	RB	RC
	Jan Qualified	883B	883C
54/54H	X	X	X
54LS	X	X	X
54S	X	X	X
82/8T	X	X	X
93XX	X	X	X
96XX	—	X	X
Linear	Planned	X	X
Bipolar Memory	Planned	X	X
Microprocessor	—	X	X

Table 2 MILITARY SUMMARY

JAN QUALIFIED (JB)

JAN Qualified product is designed to give you the optimum in quality and reliability. The JAN processing level is offered as the result of the government's product standardization programs, and is monitored by the Defense Electronic Supply Center (DESC), through the use of industry-wide procedures and specifications.

JAN Qualified products are manufactured, processed and tested in a government certified facility to Mil-M 38510, and appropriate device slash sheet specifications. Design documentation, lot sampling plans, electrical test data and qualification data for each specific part type has been approved by the Defense Electronic Supply Center (DESC) and products appear on the DESC Qualified Products List (QPL-38510).

Group B testing, per Mil-Std-883 Method 5005, is performed on each six weeks of production on each slash sheet for each package type. Group C, per Mil-Std-883 Method 5005, is performed every ninety days for each microcircuit group. Group D testing, per Mil-Std-883 Method 5005, is performed every six months for each package type.

In addition to the common specs used throughout the industry for processing and testing, JAN Qualified products also possess a requirement for a standard marking used throughout the IC industry.

MIL-STD-883, LEVEL B

Processing to this option is ideal when no JAN slash sheets are released on devices required. Product is processed to Mil-Std-883 Method 5004, and is 100% electrically tested to industry data sheets. Devices are selectively available as custom processed parts with electricals screened to the JAN Slash Sheets.

MIL-STD-883, LEVEL C

If you need a Military temp, range device, but do not require burn in screening performed, our 883C product is ideal. 883C parts are the standard full Mil-Temperature range product to the Signetics data sheet parameters and screened to MIL-STD-883, Class C.

MILITARY GENERIC DATA

Signetics has a new program for those customers who require quality conformance data on their products. This program allows our customers to obtain reliability information without the necessity or running Groups B, C and D inspections for their particular purchase order. It provides for the customer something that has not been readily available before in the semiconductor industry in that all Military Generic Data is controlled and audited by both Government Inspection in the case of JAN data and Signetics Quality Assurance.

Signetics Military Generic Data is compiled by the Military Products Division based on data from 1) JAN quality conformance lots, and 2) Data generated by quality conformance lots run for other reliability programs. Refer to Table 4.

A Military Generic family is defined as consisting of die function and package type families.

Military Generic Data

- Allows our customers to qualify Signetics products based on existing quality conformance data performed at Signetics.
- Allows our customers to reduce costs and improve deliveries.
- Provides assurance that all Signetics die function families and packages meet Mil-M-38510 and customer reliability requirements.
- Provides an attributes summary to the customer backed by lot identity and traceability.

PROCESS LEVEL AND MARKETING	PRE-CAP VISUAL	BURN IN	FUNCTIONAL TEST	DC/AC @25°C	DC/AC @TEMP	QPL	OFFSHORE
JB JM38510XXXXX	2010, Cond. B	Yes	100%	100%	100%	Yes	No
RB SXXXX883B	2010, Cond.B	Yes	100%	100%	100%	No	Yes
RC SXXXX883C	2010, Cond. B	No	100%	100% dc Sample ac	Sample dc only	No	Yes

Table 3 MILITARY PRODUCTS PROCESSING MATRIX

QUALIFIED SUB-GROUPS	QUALIFIES	OPTION 1	OPTION 2
A*	Electrical Test		
B	Package—Same package construction and lead finish.	Data selected from devices manufactured within 6 weeks of the manufacturing period on the same production line through final seal.	Data selected from devices manufactured within 24 weeks of manufacturing period.
C	Die/Process—Devices representing the same process families.	Data selected from representative devices from the same microcircuit group and sealed within 12 weeks of the manufacturing period.	Data selected from the representative devices from the same microcircuit group and sealed within 48 weeks of the manufacturing period.
D	Package—Same package construction and lead finish.	Data selected from the devices representing the same package construction and lead finish manufactured within the 24 weeks of manufacturing period. If specific data not available, Option 2 will be supplied.	Data selected from the devices representing the same package construction and lead finish manufactured within the 52 weeks of manufacturing period.

NOTE*
Group A is performed on each lot or sublot of Signetics devices.

Table 4 DEFINITION AND QUALIFYING MANUFACTURING PERIODS FOR GENERIC DATA

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS			
			CLASS S	JAN QUALIFIED (JB)	883B (RB)	883C (RC)
General Mil-M-38510	The Manufacturer shall establish and implement a Products Assurance Program Plan and provide for a manufacturer survey by the qualifying activity, Para. 3.4.1.1	—	X	X	N/A	N/A
1. Pre-Certification						
A. Product Assurance Program Plan						
B. Manufacturer's Certification						
2. Certification	Received after manufacturer has completed a successful survey, Para. 3.4.1.2	—	X	X	N/A	N/A
3. Device Qualification	Device qualification shall consist of subjecting the desired device to groups A, B, C & D of method 5005 to tightened LTPD, Para. 3.4.1.2	—	X	X	N/A	N/A
4. Traceability	Traceability maintained back to a production lot Para. 3.4.6	—	X	X	X	X
5. Country of Origin	Devices must be manufactured, assembled, and tested within the U.S. or its territories, Para. 3.2.1	—	X	X	N/A	N/A
Screening Per Method 5004 of Mil-Std-883						
6. Internal Visual (Precap)	2010, Cond. A or B	100%	XA	XB	XB	XB
7. Stabilization Bake	1008, Cond. C Min; (24 Hrs @ 150°C)	100%	X	X	X	X
8. Temperature Cycling*	1010, Cond. C; (10 cycles, −65°C to +150°C)	100%	X	X	X	X
*For Class B and C devices thermal shock may be substituted, 1011, Cond. A; (15 cycles, 0° to +100°C)						
9. Constant Acceleration	2001, Cond. E; (30kg in YI Plane)	100%	X	X	X	X
10. Visual Inspection	There is no test method for this screen; it is intended only for the removal of "Catastrophic Failures" defined as "Missing Leads, Broken Packages or Lids Off."	100%	X	X	X	X
11. Seal (Hermeticity)	1014					
A. Fine	Cond. A or B (5.0 X 10^{-8}CC/Sec)	100%	X	X	X	X
B. Gross	Cond. C2 Min.	100%	X	X	X	X
12. Interim Electricals (Pre Burn-In)	Per applicable device specification	100% Optional	100% Read & Record	Slash Sheet	Data Sheet	N/A
13. Burn-In	1015, Cond. as specified (160 hrs. Min. at 125°C)	100%	100% 240 hrs.	X		N/A
14. Final Electricals	Per applicable Device Specification	100%	100% Read & Record	Slash Sheet	Data Sheet	Data Sheet
A. Static Tests @ 25°C	Sub Group 1		X	X	X	X
B. Static Tests @ +125°C	Sub Group 2		X	X	X	N/A
C. Static Tests @ −55°C	Sub Group 3		X	X	X	N/A

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD CLASS B PRODUCTS

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS			
			CLASS S	JAN QUALIFIED (JB)	883B (RB)	883C (RC)
D. Dynamic Test @25°C	Sub Group 4 (for Linear Product Mainly)		X	X	X	X
E. Functional Test @25°C	Sub Group 7		X	X	X	X
F. Switching Test @25°C	Sub Group 9		X	X	X	N/A
15. Percent Defective allowable (PDA)	A PDA of 10% is a normal requirement applied against the static tests @ 25°C (A-1). This is controlled by the slash sheets for JB & JBX products. For RBX & RB 10% is standard	10%	5%	X	X	N/A
16. Marking	Fungus Inhibiting Paint	100%	As Req'd	JM38510/XXXX Slash Sheet #	S X X X X 883B	SXXXX 883C
17. X-Ray	2012		100%	N/A	N/A	N/A
18. External Visual	2009	100%	X	X	X	X
Quality Conformance Inspection per Method 5005 of Mil-Std 883						
19. Group A	Electrical Tests-Final Electricals (#14 above) repeated on a sample basis. (Sub Groups 1 thru 12 as specified.)	Each Lot	X	X	X	X
20. Group B	Package functional and constructional related test I.E. package dimensions, resistance to solvents, internal visual & mechanical, bond strength & solderability.	Every 6 week per microcircuit group	X	X	Generic Data Available	
21. Group C	Die related tests I.E. 1,000 hr. operating life, temperature cycling, & constand acceleration.	Every 3 months per package type	X	X	Generic Data Available	
22. Group D	Package related tests I.E. physical dimensions, lead fatigue, thermal shock, temperature cycle, moisture resistance, mechanical shock, vibration variable frequency constant acceleration, & salt atmosphere.	Every 6 months per package type	X	X	Generic Data Available	

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD CLASS B PRODUCTS (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT-PACK	DIP	FLAT-PACK
5400	Quad 2-Input NAND Gate	/00104	1	1	F	W
5401	Quad 2-Input NAND Gate with o/c	/00107	1	1	F	W
5402	Quad 2-Input NOR Gate	/00401	1	1	F	W
5403	Quad 2-Input NAND Gate with o/c	/00109	1	—	F	—
5404	Hex Inverter	/00105	1	1	F	W
5405	Hex Inverter with o/c	/00108	1	1	F	W
5406	Hex Inverter w/Buffer/Driver with o/c	/00801	—	—	F	W
5407	Hex Buffer/Driver with o/c	/00803	—	—	F	W
5408	Quad 2-Input AND Gate	/01601	1	1	F	W
5409	Quad 2-Input AND Gate with o/c	/01602	1	1	F	W
5410	Triple 3-Input NAND Gate	/00103	1	1	F	W
5411	Triple 3-Input NAND Gate	—	—	—	F	W
5412	Triple 3-Input NAND Gate with o/c	/00106	—	—	F	W
5413	Dual NAND Schmitt Trigger	/15101	2	2	F	W
5414	Hex Schmitt Trigger	/15102	*	2	F	W
5416	Hex Inverter Buffer/Driver with o/c	/00802	—	—	F	W
5417	Hex Buffer/Driver with o/c	/00804	—	—	F	W
5420	Dual 4-Input NAND Gate	/00102	1	1	F	W
5421	Dual 4-Input AND Gate	—	—	—	F	W
5426	Quad 2-Input NAND Gate with o/c	/00805	1	—	F	—
5427	Triple 3-Input NOR Gate	/00404	1	1	F	W
5428	Quad 2-Input NOR Buffer	/16201	*	*	F	W
5430	8-Input NAND Gate	/00101	1	1	F	W
5432	Quad 2-Input OR Gate	/16101	2	2	F	W
5433	Quad 2-Input NOR Buffer with o/c	—	—	—	F	W
5437	Quad 2-Input NAND Buffer	/00302	1	1	F	W
5438	Quad 2-Input NAND Buffer with o/c	/00303	1	1	F	W
5439	Quad 2-Input NAND Buffer	—	—	—	F	W
5440	Dual 4-Input NAND Buffer	/00301	1	1	F	W
5442	BCD-to-Decimal Decoder	/01001	1	1	F	W
5443	Excess 3-to-Decimal Decoder	/01002	1	1	F	W
5444	Excess 3-Gray-to-Decimal Decoder	/01003	1	1	F	W
5445	BCD-to-Decimal Decoder/Driver with o/c	/01004	—	—	F	W
5446A	BCD-to-7 Segment Decoder/ Driver	/01006	—	—	F	W
5447A	BCD-to-7 Segment Decoder/ Driver	/01007	—	—	F	W
5448	BCD-to-7 Segment Decoder Driver/	/01008	—	—	F	W
5450	Expandable Dual 2-Wide 2-Input AOI	/00501	1	1	F	W
5451	Dual 2-Wide 2-Input AOI Gate	/00502	1	1	F	W
5453	4-Wide 2-Input AOI Gate (Expandable)	/00503	1	1	F	W
5454	4-Wide 2-Input AOI Gate	/00504	1	1	F	W
5455	2-Wide 4-Input AOI Gate	/04005	—	—	—	—

NOTE

Per QPL 38510-32 dated 10 January 1978
1 = Level 1 Qualification
2 = Level 2 Qualification
* = In process

LOGIC—5400 SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT-PACK	DIP	FLAT-PACK
5460	Dual 4-Input Expander	—	—	—	F	W
5470	J-K Flip-Flop	/00206	1	1	F	W
5472	J-K Master-Slave Flip-Flop	/00201	1	1	F	W
5473	Dual J-K Master-Slave Flip-Flop	/00202	1	1	F	W
5474	Dual D-Type Edge-Triggered Flip-Flop	/00205	1	1	F	W
5475	Quad Bistable Latch	/01501	1	1	F	W
5476	Dual J-K Master-Slave Flip-Flop	/00204	1	1	F	W
5477	Quad Bistable Latch	/01502	—	1	—	W
5480	Gated Full Adder	—	—	—	F	W
5483	4-Bit Binary Full Adder	/00602	1	1	F	W
5485	4-Bit Magnitude Comparator	/15001	1	1	F	W
5486	Quad 2-Input Exclusive-OR Gate	/00701	1	1	F	W
5490	Decade Counter	/01307			F	W
5491	8-Bit Shift Register	—	—	—	F	W
5492	Divide-by-Twelve Counter	/01301	1	1	F	W
5493	4-Bit Binary Counter	/01302	1	1	F	W
5494	4-Bit Shift Register {PISO}	—	—	—	F	W
5495	4-Bit Left-Right Shift Register	/00901	1	—	F	W
5496	5-Bit Shift Register	/00902	1	1	F	W
54100	4-Bit Bistable Latch {Dual}	—	—	—	F	W
54107	Dual J-K Master-Slave Flip-Flop	/00203	1	—	F	—
54109	Dual J-K Positive Edge-Triggered Flip-Flop	—	—	—	F	W
54116	Dual 4-Bit Latch with Clear	/01503	2	—	1	—
54121	Monostable Multivibrator	/01201	1	1	F	W
54122	Retriggerable Monostable Multivibrator	/01202	—	—	—	—
54123	Retriggerable Monostable Multivibrator	/01203	1	1	F	W
54125	Quad Bus Buffer Gate w/Tri-State Outputs	/15301	2	2	F	W
54126	Quad Bus Buffer Gate w/Tri-State Outputs	/15302	2	2	F	W
54128	Quad 2-Input NOR Buffer	—	—	—	F	W
54132	Quad Schmitt Trigger	/15103	*	2	F	W
54145	BCD-to-Decimal Decoder/Driver with o/c	/01005	—	—	F	W
54147	10-Line to 4-Line Priority Encoder	/15601	*	*	F	W
54148	8-Line to 3-Line Priority Encoder	/15602	2	2	F	W
54150	l6-Line to l-Line Mux	/01401	2	—	l	—
54151	8-Line to 1-Line Mux	/01406	1	1	F	W
54152	8-Line to 1-Line Mux	—	—	—	F	W
54153	Dual 4-Line to 1-Line Mux	/01403	1	1	F	W
54154	4-Line to 16-Line Decoder/Demux	/15201	2	—	1	Q
54155	Dual 2-Line to 4-Line Decoder/Demux	/15202	—	—	F	W
54156	Dual 2-Line to 4-Line Decoder/Demux	/15203	—	—	F	W
54157	Quad 2-Input Data Selector {non-inv.}	/01405	1	1	F	W
54158	Quad 2-input Data Selector {inv.}	—	—	—	F	W
54160	Synchronous 4-Bit Decade Counter	/01303	1	1	F	W

NOTE

Per QPL 38510-32 dated 10 January 1978

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DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT-PACK	DIP	FLAT-PACK
54161	Synchronous 4-Bit Binary Counter	/01306	1	1	F	W
54162	Synchronous 4-Bit Decade Counter	/01305	1	1	F	W
54163	Synchronous 4-Bit Binary Counter	/01304	1	1	F	W
54164	8-Bit Parallel-Out Serial Shift Register	/00903	1	—	F	—
54165	Parallel-Load 8-Bit Shift Register	/00904	•	•	F	W
54166	8-Bit Shift Register	—	—	—	F	W
54170	4X4 Register File	/01801	—	—	F	—
54174	Hex D-Type Flip-Flop with Clear	/01701	1	1	F	W
54175	Quad D-Type Edge-Triggered Flip-Flop	/01702	1	1	F	W
54180	8-Bit Odd/Even Parity Checker	/01901	1	1	F	W
54181	4-Bit Arithmetic Logic Unit	/01101	2	—	1	—
54182	Look-Ahead Carry Generator	/01102	1	1	F	W
54190	Synchronous Up/Down Counter (BCD)	—	—	—	•	•
54191	Synchronous Up/Down Counter (Binary)	—	—	—	•	•
54192	Synchronous Decade Up/Down Counter	/01308	•	•	F	W
54193	Synchronous 4-Bit Binary Up/Down Counter	/01309	•	•	F	W
54194	4-Bit Bidirectional Universal Shift Register	/00905	•	•	F	W
54195	4-Bit Parallel-Access Shift Register	/00906	•	•	F	W
54198	8-Bit Register	—	—	—	1	Q
54199	8-Bit Register	—	—	—	—	—
54221	Dual Monostable Multivibrator	—	—	—	F	W
54279	Quad S-R Latch	—	—	—	F	W
54298	Quad 2-Input Mux with Storage	—	—	—	F	W
54365	Hex Buffer w/Common Enable (3-State)	/16301	•	•	•	•
54366	Hex Buffer w/Common Enable (3-State)	/16302	•	•	F	W
54367	Hex Buffer, 4-Bit and 2-Bit (3-State)	/16303	•	•	F	W
54368	Hex Buffer, 4-Bit and 2-Bit (3-State)	/16304	•	•	F	W

NOTE

Per QPL 38510-32 dated 10 January 1978
1=Level 1 Qualification
2=Level 2 Qualification
•=In Process

LOGIC-54H SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT-PACK	DIP	FLAT-PACK
54H00	Quad 2-Input NAND Gate	/02304	1	1	F	W
54H01	Quad 2-Input NAND Gate with o/c	/02306	1	1	F	W
54H04	Hex Inverter	/02305	1	1	F	W
54H05	Hex Inverter with o/c	—	—	—	F	W
54H08	Quad 2-Input AND Gate	/15501	1	—	F	W
54H10	Triple 3-Input NAND Gate	/02303	1	1	F	W
54H11	Triple 3-Input NAND Gate	/15502	1	—	F	W
54H20	Dual 4-Input NAND Gate	/02302	1	1	F	W
54H21	Dual 4-Input AND Gate	/15503	1	—	F	W
54H22	Dual 4-Input NAND Gate with o/c	/02307	1	—	F	W
54H30	8-Input NAND Gate	/02301	1	1	F	W
54H40	Dual 4-Input NAND Buffer	/02401	1	1	F	W
54H50	Expandable Dual 2-Wide 2-Input A01	/04001	1	1	F	W
54H51	Dual 2-Wide 2-Input A01 Gate	/04002	1	1	F	W
54H52	Expandable 4-Wide 2-2-2-3 Input AND-OR Gate	—	—	—	F	W
54H53	4-Wide 2-Input A01 Gate (Expandable)	/04003	1	1	F	W
54H54	4-Wide 2-Input A01 Gate	/04004	1	1	F	W
54H55	2-Wide 2-Input A01 Gate	/04005	1	1	F	W
54H60	Dual 4-Input Expander	—	—	—	F	W
54H61	Triple 3-Input Expander	—	—	—	F	W
54H62	3-2-2-3 Input AND-OR Expander	—	—	—	F	W
54H71	J-K Master-Slave Flip-Flop with AND-OR Inputs	—	—	—	F	W
54H72	J-K Master-Slave Flip-Flop	/02201	1	1	F	W
54H73	Dual J-K Master-Slave Flip-Flop	/02202	1	1	F	W
54H74	Dual D-Type Edge-Triggered Flip-Flop	/02203	1	1	F	W
54H76	Dual J-K Master-Slave Flip-Flop	/02204	1	1	F	W
54H101	J-K Negative Edge-Triggered Flip-Flop	/02205	1	1	F	W
54H102	J-K Negative Edge-Triggered Flip-Flop	—	—	—	F	W
54H103	Dual J-K Negative Edge-Triggered Flip-Flop	/02206	1	1	F	W
54H106	Dual J-K Negative Edge-Triggered Flip-Flop	—	—	—	F	W
54H108	Dual J-K Negative Edge—Triggered Flip-Flop	—	—	—	F	—

NOTE

Per QPL 38510-32 dated 10 January 1978
1=Level 1 Qualification
2=Level 2 Qualification
*=In Process

LOGIC-54LS SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT-PACK	DIP	FLAT-PACK
54LS00	Quad 2-Input NAND Gate	/30001	1	1	F	W
54LS01	Quad 2-Input NAND Gate with o/c	—	—	—	F	W
54LS02	Quad 2-Input NOR Gate	/30301	1	1	F	W
54LS03	Quad 2-Input NAND Gate with o/c	/30002	2	2	F	W
54LS04	Hex Inverter	/30003	1	1	F	W
54LS05	Hex Inverter with o/c	/30004	1	1	F	W
54LS08	Quad 2-Input AND Gate	/31004	2	2	F	W
54LS09	Quad 2-Input AND Gate with o/c	—	—	—	F	W
54LS10	Triple 3-Input NAND Gate	/30005	1	1	F	W
54LS11	Triple 3-Input NAND Gate	/31001	2	2	F	W
54LS12	Triple 3-Input NAND Gate with o/c	/30006	1	1	F	W
54LS13	Dual NAND Schmitt Trigger	/31301	2	2	F	W
54LS14	Hex Schmitt Trigger	/31302	2	2	F	W
54LS15	Triple 3-Input AND Gate with o/c	/31002	1	1	F	W
54LS20	Dual 4-Input NAND Gate	/30007	1	1	F	W
54LS21	Dual 4-Input AND Gate	/31003	1	1	F	W
54LS22	Dual 4-Input NAND Gate with o/c	/30008	1	1	F	W
54LS26	Quad 2-Input NAND Gate	/32102	2	2	F	W
54LS27	Triple 3-Input NOR Gate	/30302	1	1	F	W
54LS28	Quad 2-Input NOR Buffer	/80204	2	2	F	W
54LS30	8-Input NAND Gate	/30009	1	1	F	W
54LS32	Quad 2-Input OR Gate	/30501	2	2	F	W
54LS33	Quad 2-Input NOR Buffer with o/c	—	—	—	F	W
54LS37	Quad 2-Input NAND Buffer	/30202	1	1	F	W
54LS38	Quad 2-Input NAND Buffer with o/c	/30203	2	2	F	W
54LS40	Dual 4-Input NAND Buffer	/30201	1	1	F	W
54LS42	BCD-to-Decimal Decoder	/30703	—	—	F	W
54LS51	Dual 2-Wide 2-Input A01 Gate	/03401	1	1	F	W
54LS54	4-Wide 2-Input A01 Gate	/30402	1	1	F	W
54LS55	2-Wide 4-Input A01 Gate	—	—	—	F	W
54LS73	Dual J-K Master-Slave Flip-Flop	/30101	—	—	F	W
54LS74	Dual D-Type Edge-Triggered Flip-Flop	/30102	*	*	F	W
54LS75	Quad Bistable Latch	—	—	—	F	W
54LS76	Dual J-K Master-Slave FLip-Flop	30110	2	2	F	W
54LS78	Quad Bistable Latch	—	—	—	F	W
54LS83A	4-Bit Binary Full Adder	/31201	*	*	F	W
54LS85	4-Bit Magnitude Comparator Gate	/31101	2	2	F	W
54LS86	Quad 2-Input Exclusive-OR Gate	/30502	2	2	F	W
54LS90	Decade Counter	/31501	*	*	F	W
54LS92	Divide-by-Twelve Counter	/31510	*	*	F	W
54LS93	4-Bit Binary Counter	/31502	*	*	F	W
54LS95	4-Bit Left-Right Shift Register	/30603	*	*	F	W
54LS96	5-Bit Shift Register	/30604	*	*	F	W

NOTE
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10 January 1978
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LOGIC—54LS SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT-PACK	DIP	FLAT-PACK
54LS107	Dual J-K Master-Slave Flip-Flop	/30108	•	•	F	W
54LS109	Dual J-K Positive Edge-Triggered Flip-Flop	/30109	2	2	F	W
54LS112	Dual J-K Negative Edge-Triggered Flip-Flop	/30103	2	2	F	W
54LS113	Dual J-K Negative Edge-Triggered Flip-Flop	/30104	•	•	F	W
54LS114	Dual J-K Negative Edge-Triggered Flip-Flop	/03105	—	—	F	W
54LS122	Retriggerable Monostable Multivibrator	/31408	—	—	—	—
54LS125	Quad Bus Buffer Gate w/Tri-State Outputs	/32301	•	•	F	W
54LS126	Quad Bus Buffer Gate w/Tri-State Outputs	/32302	2	2	F	W
54LS132	Quad Schmitt Trigger	/31303	2	2	F	W
54LS136	Quad Exclusive-or with o/c	—	—	—	F	W
54LS138	3-to-8 Line Decoder/Demux	/30701	•	•	F	W
54LS139	Dual 2-to-4 Line Decoder/Demux	/30702	•	•	F	W
54LS145	BCD to Decimal Decoder/Dye	—	—	—	F	W
54LS151	8-Line to 1-Line Mux	/30901	•	•	•	•
54LS153	Dual 4-Line to 1-Line Mux	/30902	2	2	F	W
54LS154	4-Line to 16-Line Decoder/Demux	—	—	—	1	Q
54LS155	Dual 2-Line to 4-Line Decoder/Demux	—	—	—	F	W
54LS157	Quad 2-Input Data Selector (non-inv.)	/30903	•	•	F	W
54LS158	Quad 2-Input Data Selector (inv.)	/30904	•	•	F	W
54LS160	Synchronous 4-Bit Decade Counter	/31503	•	•	F	W
54LS161	Synchronous 4-Bit Binary Counter	/31504	•	•	F	W
54LS162	Synchronous 4-Bit Decade Counter	/31511	•	•	F	W
54LS163	Synchronous 4-Bit Binary Counter	/31512	•	•	F	W
54LS164	8-Bit Parallel-Out Serial Shift Register	/30605	2	2	F	W
54LS170	4X4 Register FIle	—	—	—	F	W
54LS173	Quad D-Type Flip-Flop (Tri-State) (8T10)	—	—	—	F	W
54LS174	Hex D-Type Flip-Flop with Clear	/30106	2	2	F	W
54LS175	Quad D-Type Edge-Triggered Flip-Flop	/30107	2	2	F	W
54LS181	4-Bit Arithmetic Logic Unit	/30801	2	—	F	W
54LS190	Synchronous Up/Down Counter (BCD)	/31513	•	•	F	W
54LS191	Synchronous Up/Down Counter (Binary)	/31509	•	•	F	W

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LOGIC-54LS SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT-PACK	DIP	FLAT-PACK
54LS192	Synchronous Decade Up/Down Counter	/31507	*	*	F	W
54LS193	Synchronous 4-Bit Binary Up/Down Counter	/31508	*	*	F	W
54LS194	4-Bit Bidirectional Universal Shift Register	/30601	*	*	F	W
54LS195	4-Bit Parallel-Access Shift Register	/30602	*	*	F	W
54LS196	Presettable Decade Counter/ Latch (8290)	/32001	*	*	F	W
54LS197	Presettable Binary Counter/ Latch (8291)	/32002	*	*	F	W
54LS221	Dual Monostable Multivibrator	/31402	*	*	*	*
54LS251	Data Selector/Mux with 3-State Outputs	/30905	*	*	*	*
54LS253	Dual 4-Line to 1-Line Data Selector/Mux	/30908	2	2	F	W
54LS257	Quad 2-Line to 1-Line Data Selector/Mux	/30906	*	*	*	*
54LS258	Quad 2-Line to 1-Line Data Selector/Mux	/30907	*	*	*	*
54LS260	Dual 5-Input NOR Gate	—	—	—	F	W
54LS261	2X4 Parallel Binary Multiplier	—	—	—	F	W
54LS266	Quad Exclusive-NOR Gate	/30303	2	2	F	W
54LS279	Quad S-R Latch	—	—	—	F	W
54LS280	9-Bit Odd/Even Parity Generator/Checker	—	—	—	*	*
54LS283	4-Bit Adder	/31202	*	*	F	W
54LS290	Decade Counter	/32003	*	*	F	W
54LS293	4-Bit Binary Counter	/32004	*	*	F	W
54LS295A	4-Bit Right-Shift Left-Shift Register	/30606	*	*	F	W
54LS298	Quad 2-Input Mux with Storage	—	—	—	F	W
54LS365	Hex Buffer w/common Enable (3-State)	/32201	*	*	F	W
54LS366	Hex Buffer w/Common Enable (3-State)	/32202	*	*	F	W
54LS367	Hex Buffer, 4-Bit and 2-Bit (3-State)	/32203	*	*	F	W
54LS368	Hex Buffer, 4-Bit and 2-Bit (3-State)	/32204	*	*	F	W
54LS375	Quad Latch	—	—	—	F	W
54LS386	Exclusive-OR Gate	—	—	—	F	W
54LS395	4-Bit Cascadealbe Shift Register (3-State)	/30607	*	*	F	W
54LS445	BCD to Decimal Decoder/Dye	—	—	—	F	W
54LS670	4X4 Register File (Tri-State)	—	—	—	F	W

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LOGIC-54S SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT-PACK	DIP	FLAT-PACK
54S00	Quad 2-Input NAND Gate	/07001	1	1	F	W
54S02	Quad 2-Input NOR Gate	/07301	1	1	F	W
54S03	Quad 2-Input NAND Gate with o/c	/07002	1	1	F	W
54S04	Hex Inverter	/07003	1	1	F	W
54S05	Hex Inverter with o/c	/07004	1	1	F	W
54S08	Quad 2-Input AND Gate	/08003	*	*	F	W
54S09	Quad 2-Input AND Gate with o/c	/08004	—	—	F	W
54S10	Triple 3-Input NAND Gate	/07005	1	1	F	W
54S11	Triple 3-Input NAND Gate	/08001	1	1	F	W
54S15	Triple 3-Input AND Gate with o/c	/08002	2	2	F	W
54S20	Dual 4-Input NAND Gate	/07006	1	1	F	W
54S22	Dual 4-Input NAND Gate with o/c	/07007	1	1	F	W
54S30	8-Input NAND Gate	/07008	—	—	—	—
54S32	Quad 2-Input OR Gate	—	—	—	F	W
54S40	Dual 4-Input NAND Buffer	/07201	1	1	F	W
54S51	Dual 2-Wide 2-Input A01 Gate	/07401	1	1	F	W
54S64	4-2-3-2 Input A01 Gate	/07402	1	1	F	W
54S65	4-2-3-2 Input A01 Gate	/07403	2	2	F	W
54S74	Dual D-Type Edge-Triggered Flip-Flop	/07101	2	2	F	W
54S85	4-Bit Magnitude Comparator	/08201	2	—	F	—
54S86	Quad 2-Input Exclusive-OR Gate	/17501	1	1	F	W
54S112	Dual J-K Negative Edge-Triggered Flip-Flop	/07102	*	*	F	W
54S113	Dual J-K Negative Edge-Triggered Flip-Flop	/07103	*	*	F	W
54S114	Dual J-K Negative Edge-Triggered Flip-Flop	/07104	—	—	F	W
54S133	13-Input NAND Gate	/07009	1	1	F	W
54S134	12-Input NAND Gate w/Tri-State Outputs	/07010	2	2	F	W
54S135	Quad Exclusive-OR/NOR Gate	/07502	—	—	—	—
54S138	3-to-8 Line Decoder/Demux	/07701	—	—	—	—
54S139	Dual 2-to-4 Line Decoder/Demux	/07702	—	—	F	W
54S140	Dual 4-Input NAND Line Driver	/08101	2	2	F	W
54S151	8-Line to 1-Line Mux	/07901	2	2	F	W
54S153	Dual 4-Line to 1-Line Mux	/07902	1	1	F	W
54S157	Quad 2-Input Data Selector (non.inv.)	/07903	2	2	F	W
54S158	Quad 2-Input Data Selector (inv)	/07904	2	2	F	W
54S174	Hex D-Type Flip-Flop with Clear	/07105	—	—	F	W
54S175	Quad D-Type Edge-Triggered Flip-Flop	/07106	—	—	*	*
54S181	4-Bit Arthmetic Logic unit	/07801	2	—	F	*
54S182	Look-Ahead Carry Generator	/07802	—	—	*	*
54S194	4-Bit Bidirectional Universal Shift Register	/07601	—	—	—	—
54S195	4-Bit Parallel-Access Shift Register	/07602	—	—	—	—

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LOGIC—54S SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT-PACK	DIP	FLAT-PACK
54S251	Data Selector/Mux with 3-State Outputs	/07905	—	—	—	—
54S253	Dual 4-Line to 1-Line Data Selector/Mux	—	—	—	F	W
54S257	Quad 2-Line to 1-Line Data Selector/Mux	/07906	—	—	—	—
54S258	Quad 2-Line to 1-Line Data Selector/Mux	/07907	—	—	—	—
54S260	Dual 5-Input NOR Gate	—	—	—	F	W
54S280	9-Bit Odd/Even Parity Generator/Checker	/07703	—	—	—	—
54S350	4/6 Bit Shifter-Tri-State	—	—	—	F	—

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DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT-PACK	DIP	FLAT-PACK
8200	Dual 5-Bit Buffer Register	—	—	—	I	Q
8201	Dual 5-Bit Buffer Register with D Inputs	—		—	I	Q
8202	10-Bit Buffer Register	—	—	—	I	Q
8203	10-Bit Buffer Register with D Inputs	—	—	—	I	Q
8230	8-Input Digital Multiplexer	/01402	•	•	F	W
8231	8-Input Digital Multiplexer	—	—	—	F	W
8232	8-Input Digital Multiplexer	—	—	—	F	W
8233	2-Input 4-Bit Digital Multiplexer		—	—	F	W
8234	2-Input 4-Bit Digital Multiplexer		—	—	F	W
8235	2-Input 4-Bit Digital Multiplexer	—	—	—	F	W
8241	Quad Exclusive-OR Gate	—	—	—	F	W
8242	Quad Exclusive-NOR Gate	—	—	—	F	W
8243	8-Bit Position Scaler	—	—	—	1	Q
8250	Binary-to-Octal Decoder	/15204	2	2	F	W
8251	BCD-to-Decimal Decoder	/15205	2	2	F	W
8252	BOD-to-Decimal Decoder	/15206	—	—	F	W
8260	Arithmetic Logic Unit	—	—	—	I	Q
8261	Fast Carry Extender	—	—	—	F	W
8262	9-Bit Parity Generator and Checker	—	—	—	F	W
8263	3-Input 4-Bit Digital Multiplexer	—	—	—	I	Q
8264	3-Input 4-Bit Digital Multiplexer		—	—	I	Q
8266	2-Input 4-Bit Digital Multiplexer	—	—	—	F	W
8267	2-Input 4-Bit Digital Multiplexer	—	—	—	F	W
8268	Gated Full Adder	—	—	—	F	Q
8269	4-Bit Comparator	—	—	—	F	W
8270	4-Bit Shift Register	—	—	—	F	W
8271	4-Bit Shift Register	—	—	—	F	W
8273	10-Bit Serial-In Parallel-Out Shift Register	—	—	—	F	W
8274	10-Bit Parallel-In, Serial-Out Shift Register	—	—	—	F	W
8275	Quad Bistable Latch	—	—	—	F	W
8276	8-Bit Serial Shift Register	—	—	—	F	—
8277	Dual 8-Bit Shift Register	—	—	—	F	—
8280	Presettable Decade Counter	—	—	—	F	W
8281	Presettable Binary Counter	—	—	—	F	W
8284	Binary Up/Down Counter	—	—	—	F	W
8285	Decade Up/Down Counter	—	—	—	F	W
8288	Divide-by-Twelve Counter	—	—	—	F	W
8290	Presettable High Speed Decade Counter	—	—	—	F	W
8291	Presettable High Speed Binary Counter	—	—	—	F	W
8292	Presettable Low Power Decade Counter	—	—	—	F	W
8293	Presettable Low Power Binary Counter	—	—	—	F	W
9300	4-Bit Shift Register	/15901	—	—	F	W
9301	BCD to Decimal Decoder	/15206	2	2	F	W
9308	Dual 4-Bit Latch w/Clear	—	—	—	I	Q
9309	Dual 4-Input Multiplexer	/01404	1	1	F	W
9310	4-Bit Decade Counter	—	—	—	F	W
9312	8-Input Digital Multiplexer	/01402	•	•	F	W
9316	4-Bit Binary Counter	—	—	—	F	W
9322	Data Selector-Multiplexer	—	—	—	F	W
9324	5-Bit Comparator	/15002	•	•	W	—
9334	8-Bit Addressable Latch	/16001	—	—	F	W
9602	Dual Monostable Multivibrator	/01205	•	•	F	W

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LOGIC—8T INTERFACE SERIES

DEVICE	DESCRIPTION	JAN M38510 SHEET	MIL-STD 883	
			DIP	FLAT-PACK
8T04	7-Segment Decoder Display Driver (Active-Low Outputs)	—	F	W
8T05	7-Segment Decoder Display Driver (Active-Hi Outputs)	—	F	W
8T06	7-Segment Decoder Display Driver (Active-Low Outputs)	—	F	W
8T09	Quad Bus Driver with Tri-State Outputs	—	F	W
8T10	Quad D-Type Bus Latch (Tri-State)	—	F	W
8T13	Dual Line Driver	—	F	W
8T14	Triple Line Receiver/Schmitt Trigger	—	F	W
8T18	Dual 2-Input NAND (High Voltage to TTL Interface)	—	F	W
8T20	Bidirectional Monostable Multivibrator (Diff. Input)	—	*	*
8T22	Retriggerable Monostable Multivibrator (54122/9601)	—	F	W
8T26A	Quad Bus Driver/Receiver (Tri-State Outputs)	—	F	W
8T28	Quad Non-Inverting Bus Driver/Receiver (Tri-State Outputs)	—	F	W
8T31	8-Bit Bidirectional I/O Port	—	*	*
8T32	Programmable 8-Bit, I/O Port (3-State)	—	1	*
8T33	Programmable 8-Bit, I/O Port (Open Collector)	—	1	*
8T35	Asynchronous Programmable 8-Bit I/O Port (Open Collector)		1	W
8T37	Hex Bus Receiver with Hysteresis-Schmitt Trigger (D?		F	W
8T38	Quad Bus Transceiver (Open Collector) (DM8838)		F	W
8T80	Quad 2-Input NAND Gate (High Voltage)		F	W
8T90	Hex Inverter (High Voltage)	—	F	W
8T95	High Speed Hex Buffers/Inverters (74365/DM8095)	—	F	W
8T96	High Speed Hex Buffers/Inverters (74366/DM8096)	—	F	W
8T97	High Speed Hex Buffers/Inverters (74367/DM8097)		F	W
8T98	High Speed Hex Buffers/Inverters (74368/DM8098)		F	W

* = Qualification planned

BIPOLAR MEMORY CROSS REFERENCE

DEVICE	ORGANIZATION	PACKAGE*		OUTPUT CIRCUIT	NUMBER OF PINS
PROMs					
82S23	32X8	F	R	OC	16
82S115	512X8	I	R	TS	24
82S123	32X8	F	R	TS	16
82S126	256X4	F	R	OC	16
82S129	256X4	F	R	TS	16
82S130	512X4	F	R	OC	16
82S131	512X4	F	R	TS	18
82S136	1024X4	F,I	R	OC	18
82S137	1024X4	F,I	R	TS	18
82S140	512X8	I	R	OC	24
82S141	512X8	I	R	TS	24
82S180	1024X8	I	R	OC	24
82S181	1024X8	I	R	TS	24
82S184	2048X4	I	R	OC	18
82S185	2048X4	I	R	TS	18
82S2708	1024X8	I	R	TS	24
82S190	2048X8	I		OC	24
82S191	2048X8	I		TS	24
FPLAs					
82S100	16X48X8	I	R	TS	28
82S101	16X48X8	I	R	OC	28
82S102	16X9	I	R	OC	28
82S103	16X9	I	R	TS	28
PLAs					
82S200	16X48X8	I	R	TS	28
82S201	16X48X8	I	R	OC	28
RAMs					
3101A	16X4	F	R	OC	16
54S89	16X4	F	R	OC	16
54S189	16X4	F	R	TS	16
54S200	256X1	F	R	TS	16
54S201	256X1	F	R	TS	16
54S301	256X1	F	R	OC	16
82S09	64X9	I	R	TS	28
82S10	1024X1	F,I	R	OC	16
82S11	1024X1	F,I	R	TS	16
82S16	256X1	F	R	TS	16
82S17	256X1	F	R	OC	16
82S25	16X4	F	R	OC	16
ROMs					
82S215	512X8	I	R	TS	24
82S223	32X8	F	R	OC	16
82S224	32X8	F	R	TS	16
82S226	256X4	F	R	OC	16
82S229	256X4	F	R	TS	16
82S230	512X4	F	R	OC	16
82S231	512X4	F	R	TS	16
82S280	1024X8	I	R	OC	24
82S281	1024X8	I	R	TS	24
82S290	2048X8	I	R	OC	24
82S291	2048X8	I	R	TS	24

R = BeO Flat Pack
F = Cerdip
I = Ceramic DIP

JAN M-38510			
DEVICE	SLASH SHEET	PKG	QUAL STATUS
82S126	20301	F	Part II
82S129	20302	F	Part II
82S130	20401	F	Part II
82S131	20402	F	Part II

JAN per QPL M38510-34 date April 1978

BIPOLAR MICROPROCESSORS

PRODUCT	DESCRIPTION	AVAILABILITY	
		DIP	FLAT PACK
3001	Microprogram Control Unit	I	R
3002	Central Processing Element (2-bit slice)	I	R
8X300	Interpreter/Microcontroller	I	*
2901-1	Central Processing Element (4-bit slice)	*	*

* Under development

MICROPROCESSOR SUPPORT CIRCUITS

PRODUCT	DESCRIPTION	AVAILABILITY	
		DIP	FLAT PACK
LOGIC			
54123	Retriggerable Monostable Multivibrator	F	W
54180	8-Bit Odd/Even Parity Checker	F	W
54298	Quad 2-Input Mux with Storage	F	W
54S182	Look-Ahead Carry Generator	*	*
54S194	4-Bit Bidirectional Shift Register	*	*
54S195	4-Bit Parallel Access Shift Register	*	*
54LS365	High Speed Hex Tri-State Buffer	F	*
54LS366	High Speed Hex Tri-State Buffer	F	*
54LS367	High Speed Hex Tri-State Buffer	F	*
54LS368	High Speed Hex Tri-State Buffer	F	*
8262	9-Bit Parity Generator Checker	F	W
8281	Presettable Binary Counter	F	W
8291	Presettable High Speed Binary Counter	F	W
9602	Dual Monostable Multivibrator	F	W
	INTERFACE		
8T09	Quad Bus Driver with Tri-State Output	F	W
8T10	Quad D-Type Bus Latch (Tri-State Outputs)	F	W
8T13	Dual Line Driver	F	W
8T14	Triple Lin Receiver/Schmitt Trigger	F	W
8T26A	Quad Bus Driver/Receiver (Tri-State)	F	W
8T28	Quad Bus Non-Inverting Driver/Receiver (tri-State)	F	W
8T32	Programmable 8-Bit I/O Port (3-State)	I	*
8T33	Programmable 8-Bit I/O Port (Open Collector)	I	*
8T35	Asynchronous Programmable 8-Bit I/O Port (Open Collector)	I	*
8T95	High Speed Hex Buffer (Tri-State)	F	*
8T96	High Speed Hex Inverter (Tri-State)	F	*
8T97	High Speed Hex Buffer (Tri-State)	F	*
8T98	High Speed Hex Inverter (tri-State)	F	*

* Under development

LINEAR PRODUCTS

DEVICE	DESCRIPTION	PACKAGE	
	COMPARATORS		
SE521	Dual Comparator	F	
SE522	Dual Comparator	F	
SE526	Analog Voltage Comparator	F	K
SE527	Analog Voltage Comparator	F	K
SE529	Analog Voltage Comparator	F	K
LH2111	Dual Comparator	F	
LM111	Comparator	F	T
LM119	Dual Comparator	F	K
LM139	Quad Comparator	F	
LM193/ 193A	Dual Comparator		T
μA710	Differential Voltage Comparator	F	T
μA711	Comparator	F	K
	DIFFERENTIAL AMPLIFIERS		
SE510	Dual Differential Amplifier	F	
SE511	Dual Differential Amplifier	F	
SE515	Differential Amplifier	F	K
μA733	Video Amplifier	F	K
	OPERATIONAL AMPLIFIERS		
LF155/ 156/157	FET Operational Amplifier	T	
LH2101A	Dual Operational Amplifier	F	
LH2108A	Dual Operational Amplifier	F	
LM101	High Performance Operational Amp	F	T
LM101A	High Performance Operational Amp	F	T
LM107	General Purpose Operational Amp	F	F
LM108	Precision Operational Amp	F	T
LM108A	Precision Operational Amp	F	T
LM124	Quad Operational Amplifier	F	
LM158	Dual Operational Amplifier		T
MC1556	Operational Amplifier	F	T
MC1558	Dual Operational Amplifier	F	T
SE532	Dual Operational Amplifier		T
SE535	Hi Slew Rate Operational Amp	T	
SE538	Hi Slew Rate Operational Amp	T	
μA709	Operational Amplifier	F	T
μA709A	Operational Amplifier	F	T
μA741	General Purpose Operational Amp	F	T
μA747	Dual Operational Amplifier	F	K
μA748	General Purpose Amp	F	T
SE530	Hi Slew Op Amp	F	T
SE5530	Dual Hi Slew Op Amp	F	K
SE5534	Lo Noise Op Amp	T	
SE5535	Dual Hi Slew Op Amp	F	K
SE5538	Dual Hi Slew Op Amp	F	K
SE5537	Sample & Hold	F	K
SE5539	Hi Speed Op Amp	F	K

DEVICE	DESCRIPTION	PACKAGE	
	PHASE LOCKED LOOPS		
SE567	Tone Decoder PLL	F	T
SE564	Phase Locked Loop	F	T
	INTERFACE		
55325	Memory Driver	F	
	LINE RECEIVERS		
DM7820	Dual Differential Line Receiver	F	
DM7830	Dual Differential Line Receiver	F	
	AUDIO CIRCUITS		
SE570	Compandor	F	
	TIMERS		
SE555	Timer	F	T
SE556	Dual Timer	F	T
SE558/559	Quad Timer	F	
	VOLTAGE REGULATORS		
LM109	5 Volt Regulator	DA	
SE5551	Dual Track Reg	F	
SE5552	Dual Track Reg	F	
SE5553	Dual Track Reg	F	
SE5554	Dual Track Reg	F	
78XX(7)	Positive Reg	DA	
79XX(7)	Negative Reg	DA	
79MXX(7)	Med Power Reg	DB	
μA723	Precision Voltage Regulator	F	L
†78HV00(7)	Hi Voltage Regulator	DA	
	DRIVERS		
DS1611-1614	Peripheral Drivers		T

*NOTE
F = Cerdip
K/T/L = Metal Can
DA/DB = TO-3 can
Flat pack available—special request

JAN-M-38510				
DEVICE	SLASH SHEET	PACKAGE		QUAL. STATUS
†JB555	10901	F	T	Part II
†JB556	10902	F		Part II
†JB2101A	10105	F		Part II
JB101	10103	F	T	June 1978-Part I
JB741	10101	F	T	June 1978-Part I
JB747	10102	F	K	June 1978-Part I

†JAN per QPL M38510-34 date April 1978

CHIP PROGRAM

Signetics is currently a major supplier of chips to both the Military/Aerospace and Commercial marketplaces. All chip and wafer sales are processed through to Military Products Division.

To further enhance Signetics' ability to service the chip marketplace, Signetics has appointed Engineering Components Corporation (E.C.C.) of Salem, Massachusetts to stock and re-sell our full line of integrated circuit chips.

E.C.C. can be contacted at the following address:

E.C.C.
One Peabody Street
Salem, Massachusetts 01970
Phone: (617) 745-2450

PACKAGES

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings

General

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
   a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across V_{CC} and ground. The values are based upon 120 mils square die for plastic packages and a 90 mils square die in the smallest available cavity for hermetic packages. All units were solder mounted to P.C. boards, with standard stand-off, for measurement.

Plastic Only

5. Lead material: Alloy 42 or equivalent, solder dipped.
6. Body material: Plastic
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.

Hermetic Only

9. Lead material
   a. Alloy 52—gold plated, or solder dipped.
   b. ASTM alloy F-15 (KOVAR) or equivalent—gold plated, tin plated, or solder dipped.
   c. ASTM alloy F-30 (Alloy 42) or equivalent—tin plated.
   d. ASTM alloy F-15 (KOVAR) or equivalent—gold plated.
   e. ASTM alloy F-15 (KOVAR) or equivalent—tin plated.
10. Body Material
    a. 1010 Steel—nickel plated or tin plate over nickel.
    b. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated.
    c. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated, glass body.
    d. Ceramic with glass seal at leads.
    e. BeO ceramic with glass seal at leads.
    f. Ceramic with ASTM alloy F-15 or equivalent.
11. Lid Material
    a. 1010 steel, nickel plated, or tin-plate over nickel, weld seal.
    b. Nickel or tin plated nickel, weld seal.
    c. Ceramic, glass seal.
    d. ASTM alloy F-15 or equivalent, gold plated.
    e. BeO Ceramic with glass seal.
    f. Translucent $A1_2O_3$, glass seal.
12. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
13. Recommended minimum offset before lead bend.
14. Maximum glass climb .010 inches.
15. Maximum glass climb or lid skew is .010 inches.
16. Typical four places.
17. Dimension also applies to seating plane.

PLASTIC PACKAGES

NO. OF LEADS	PACKAGE CODE	Θ_{ja}/Θ_{jc}(°C/W)	DESCRIPTION[1]
Standard Dual-In-Line			
8	NE	162/65	
14	NH	150/65	TO-116/MO-001
16	NJ	137/53	MO-001
18	NK	135/53	
20	NL	135/53	
22	NM	120/53	
24	NN	116/53	MO-015
24	NND[3]	TBD	
28	NQ	116/53	MO-015
40	NW[3]	110/50	MO-015
Power Dual-in-Line			
8	NEA[2,3]	TBD	Heatsink
14	NHA[2]	95/33	Heatsink
16	NJA[2]	95/33	Heatsink
18	NKA[2]	90/26	Heatsink
20	NLA[2]	90/26	Heatsink
22	NMA[2,3]	TBD	Heatsink
24	NNA[2]	60/23	Heatsink
28	NQA[2]	56/21	Heatsink
40	NWA[2,3]	TBD	Heatsink
Power			
3	S	200/70	TO-92
3	UCA	75/3	TO-220
3 + GND	UC	95/15	Single-in-Line (SIL)
4 + GND	UD	95/15	Single-in-Line (SIL)
5 + GND	UEA	TBD	TO-220
7 + GND	UGA[3]	TBD	TO-220
12 + GND	PH/PHA	95/15	Batwing

HERMETIC PACKAGES

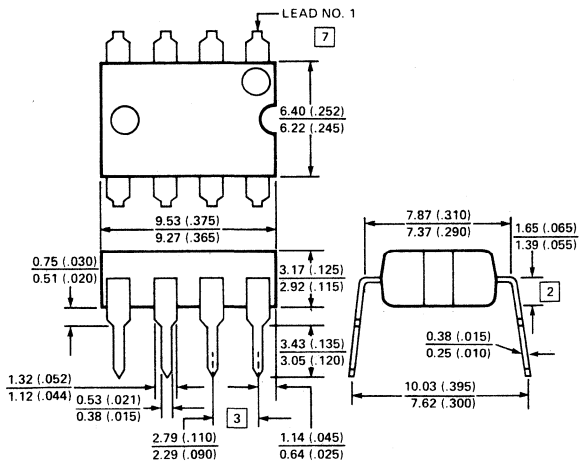
NO. OF LEADS	PACKAGE CODE	Θ_{ja}/Θ_{jc}(°C/W)	DESCRIPTION[1]
Metal Headers			
2	DA	TBD	TO-3 Solid Header
3	DB	TBD	TO-39 Solid Header, Short Can
4	DC	TBD	TO-72 Solid Header
4	DE	TBD	TO-72 Glass Filled Header
8	T	150/45	TO-99 Header (.200 Dia.)
10	K	150/45	TO-100 Header, Short Can
10	L	150/45	TO-100 Header, Tall Can
Flat Packs			
10	WF	240/50	Flat Ceramic
14	WH	205/50	Flat Ceramic
16	WJ	200/50	Flat Ceramic
24	WN	155/40	Flat Ceramic
16	RJA	145/26	Flat Ceramic, BeO
18	RKA	107/22	Flat Ceramic, BeO
24	RNA	96/22	Flat Ceramic, BeO
28	RQA	92/22	Flat Ceramic, BeO
40	RWA	77/20	Flat Ceramic, BeO
10	QFA	230/55	Flat Ceramic Laminate
14	QHA	185/45	Flat Ceramic Laminate
16	QJA	170/45	Flat Ceramic Laminate
24	QNA	155/44	Flat Ceramic Laminate
68	GBA[3]	TBD	Flat Ceramic Laminate, Leadless
Cerdip Family			
8	FE	140/32	Dual-in-Line Ceramic
14	FH	110/30	Dual-in-Line Ceramic
16	FJ	100/30	Dual-in-Line Ceramic
18	FK	93/27	Dual-in-Line Ceramic
20	FL	88/27	Dual-in-Line Ceramic
22	FM	75/27	Dual-in-Line Ceramic
24	FN	60/26	Dual-in-Line Ceramic
28	FQ	55/26	Dual-in-Line Ceramic
40	FW[3]	TBD	Dual-in-Line Ceramic
Laminated Ceramic, Side Brazed Lead			
8	IEA	100/30	Dip Laminate
14	IHA	95/25	Dip Laminate
16	IJA	90/25	Dip Laminate
18	IKA	88/25	Dip Laminate
22	IMA	80/25	Dip Laminate
24	INC	65/25	Dip Laminate
28	IQA	60/25	Dip Laminate
40	IWA	55/25	Dip Laminate
50	IZA	42/20	Dip Laminate

NOTES

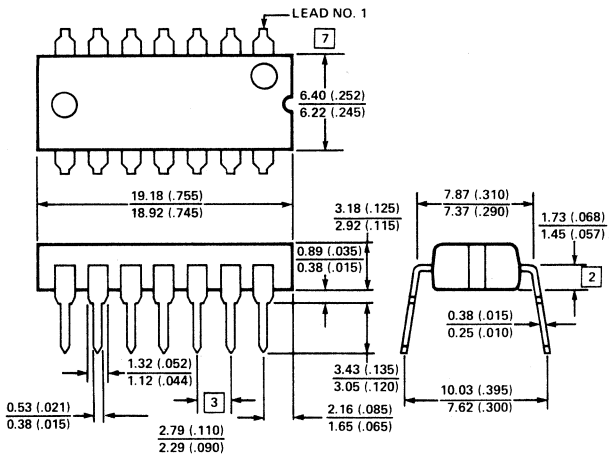
1. Dual-in-Line packages unless otherwise described.
2. Package outline is the same as corresponding standard Dual-in-Line package with identical number of leads
3. Package not yet available, scheduled for 1978 release

PLASTIC: Standard and Power Dual-In-Line

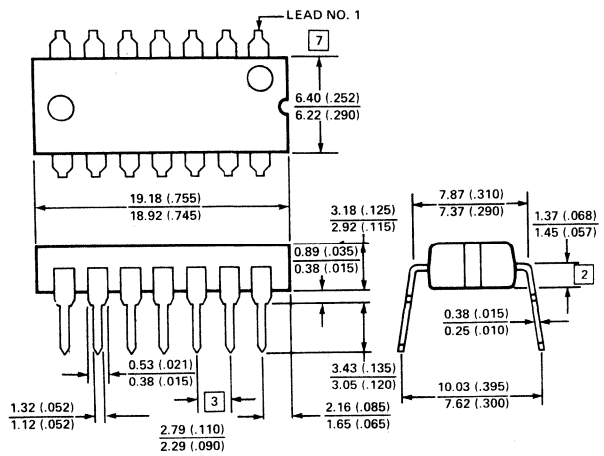
NE Package and NEA Package



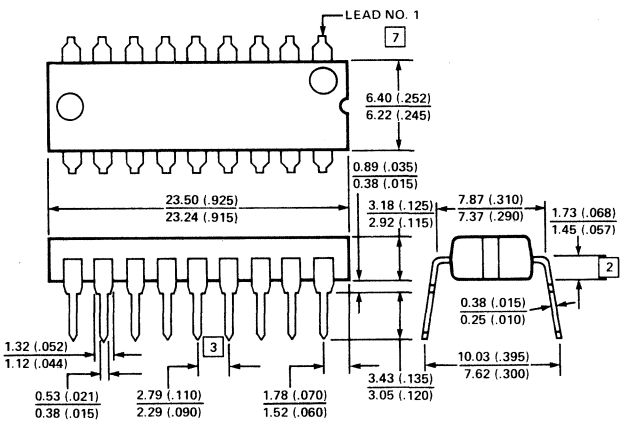
NH Package and NHA Package



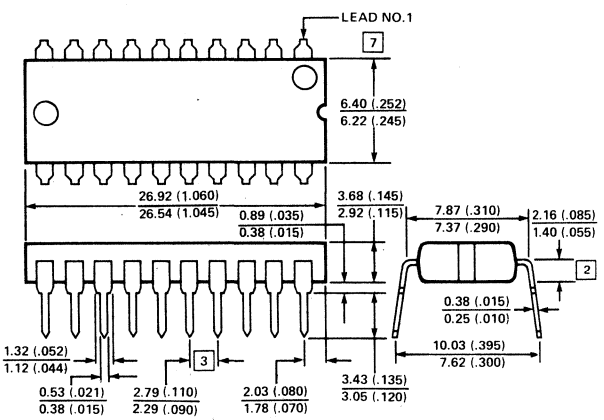
NJ Package and NJA Package



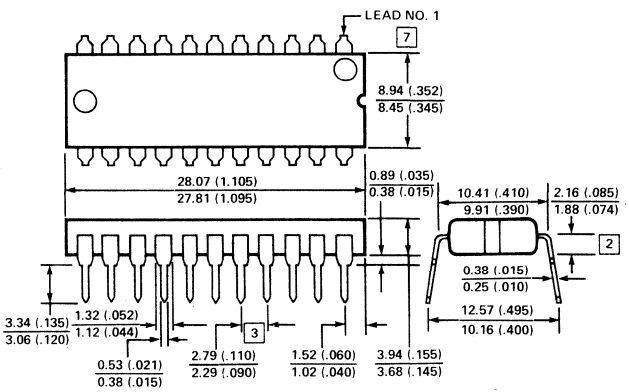
NK Package and NKA Package



NL Package and NLA Package



NM Package and NMA Package

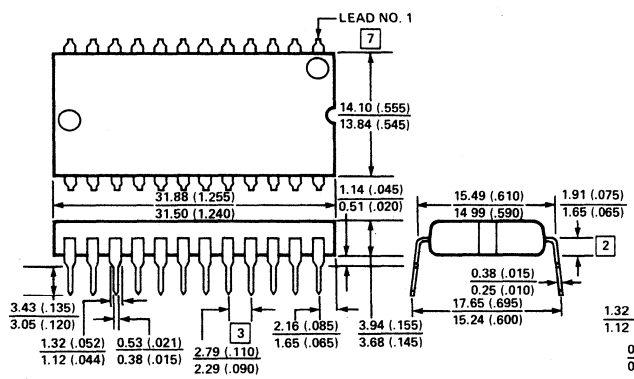


PLASTIC: Standard and Power Dual-In-Line (cont't.)

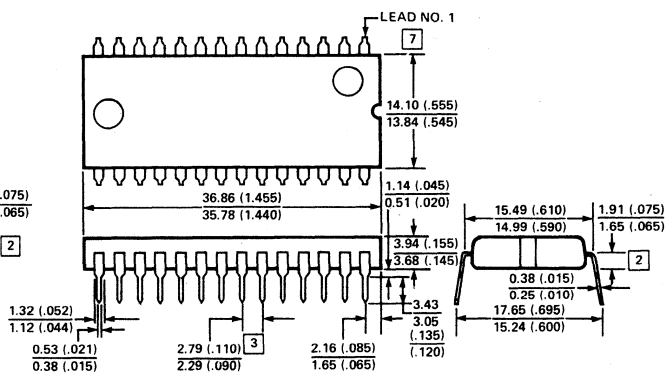
NND Package

Package not yet available.
Scheduled for 1978 release.

NN Package and NNA Package



NQ Package and NQA Package

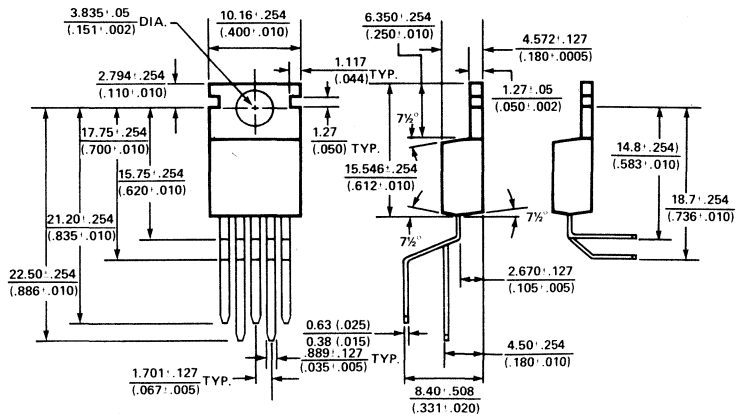


NW Package and NWA Package

Package not yet available.
Scheduled for 1978 release.

PLASTIC: Power (Not Dual-In-Line) (cont'd.)

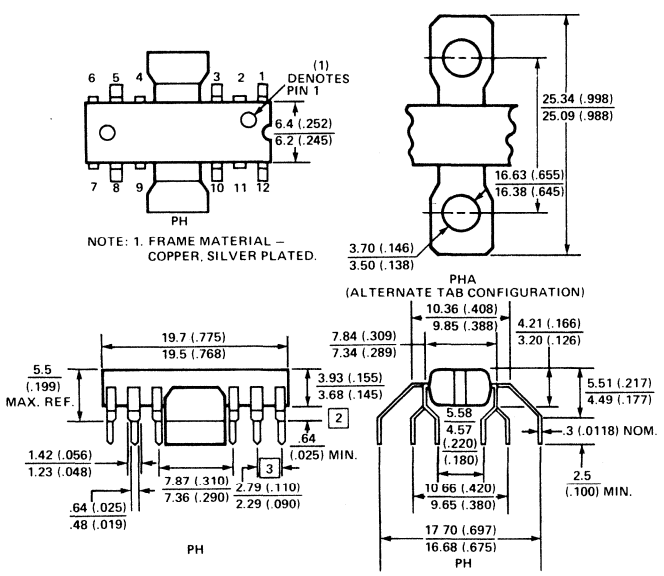
UEA Package



UGA Package

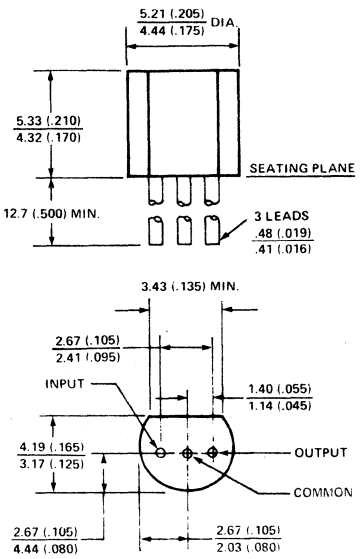
Package not yet available.
Scheduled for 1978 release.

PH/PHA Package

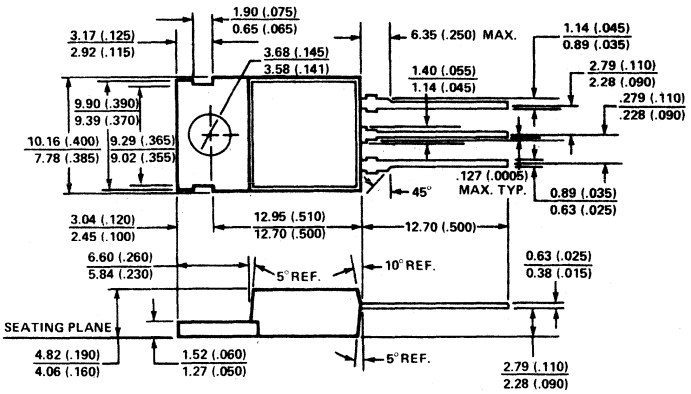


PLASTIC: Power (Not Dual-In-Line)

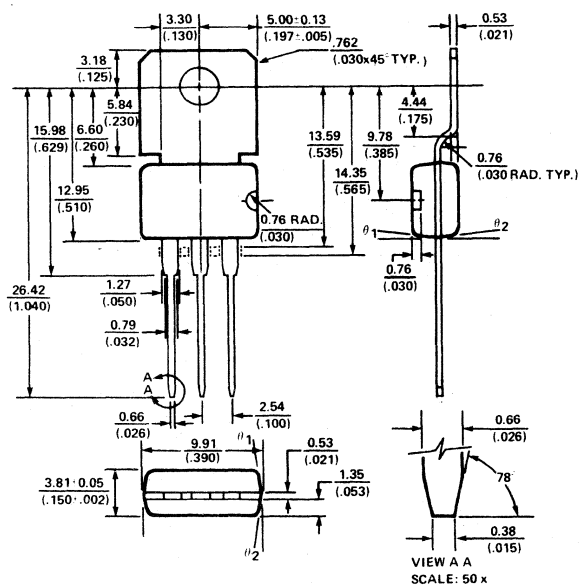
S Package



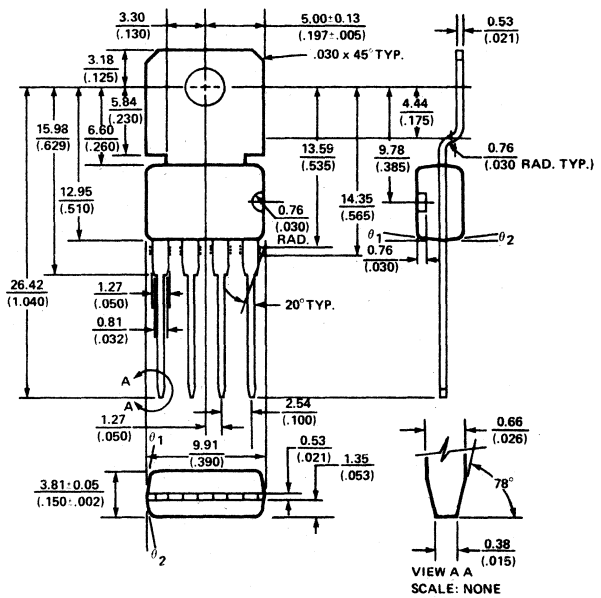
UCA Package



UC Package

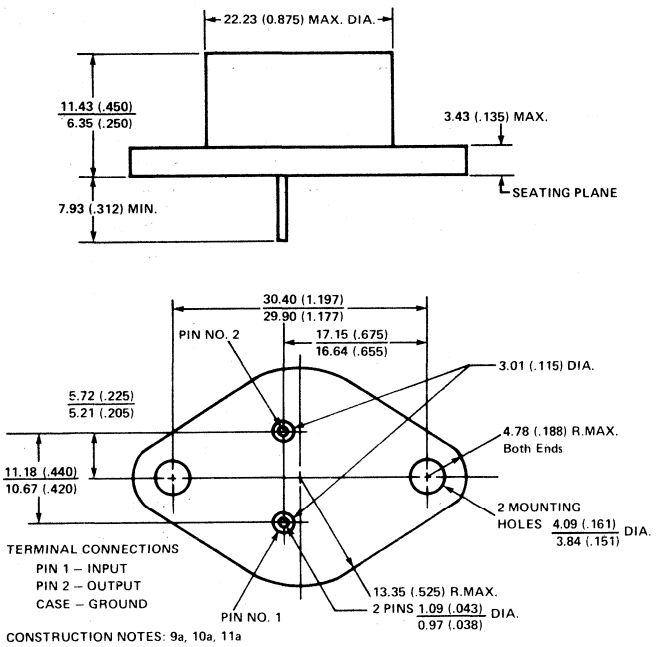


UD Package



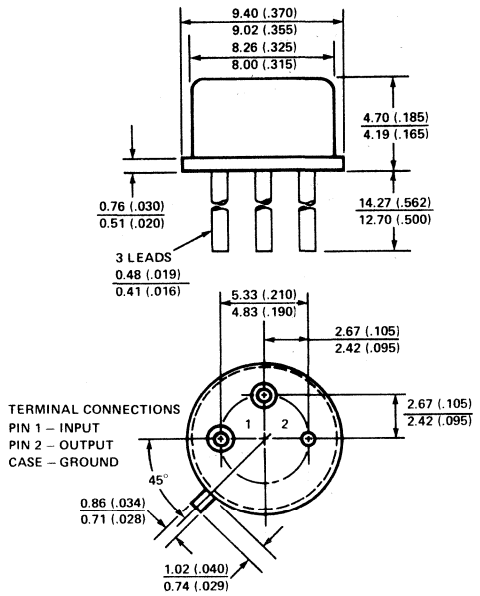
HERMETIC: Metal Headers

DA Package



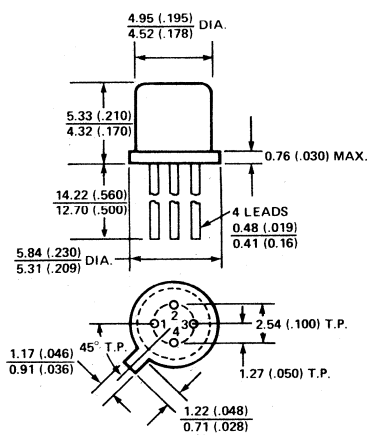
CONSTRUCTION NOTES: 9a, 10a, 11a

DB Package



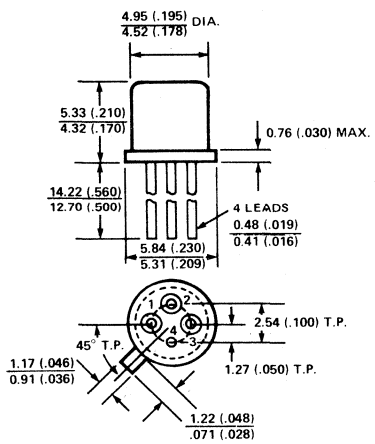
CONSTRUCTION NOTES: 9b, 10b, 11b

DC Package



CONSTRUCTION NOTES: 9b, 10b, 11b

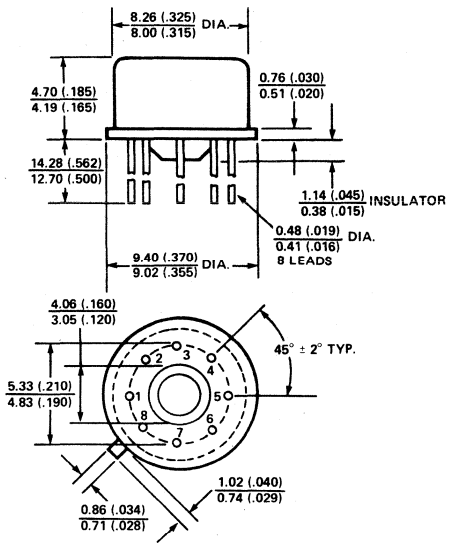
DE Package



CONSTRUCTION NOTES: 9b, 10c, 11b

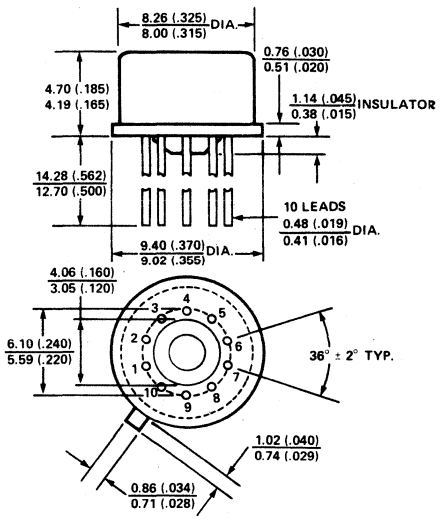
HERMETIC: Metal Headers (cont'd.)

T Package



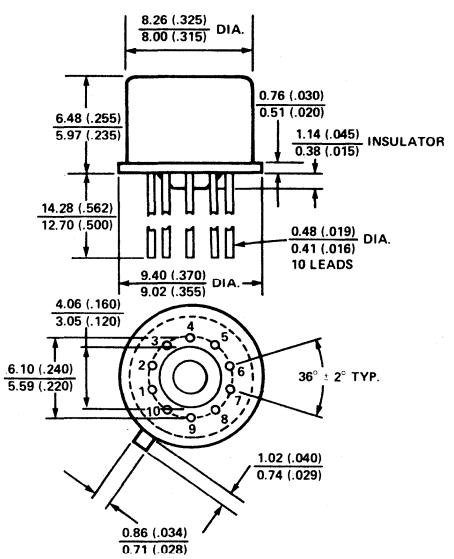
CONSTRUCTION NOTES: 9b, 10c, 11b

K Package



CONSTRUCTION NOTES: 9b, 10c, 11b

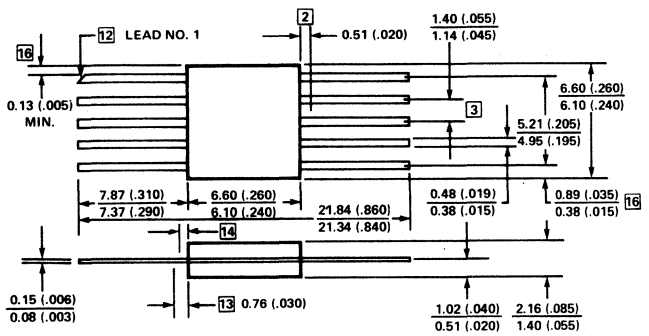
L Package



CONSTRUCTION NOTES: 9b, 10c, 11b

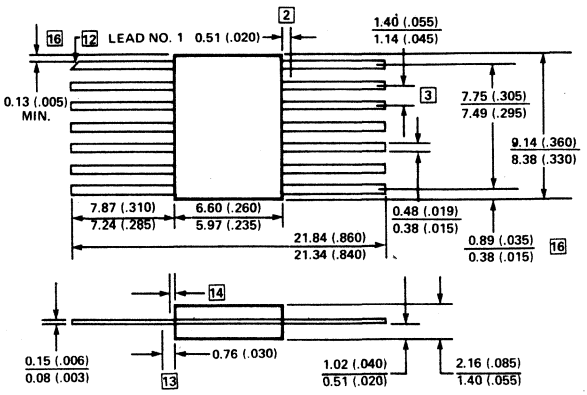
HERMETIC: Flat Packs

WF Package



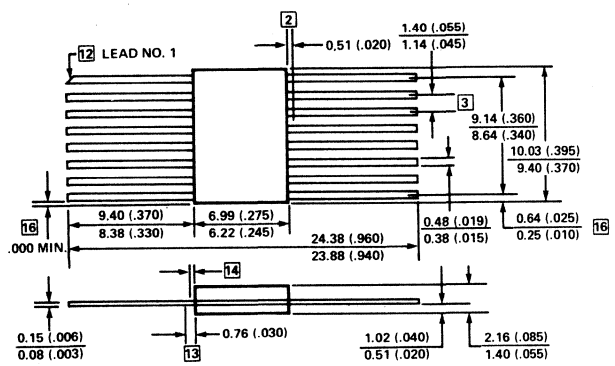
CONSTRCUTION NOTES: 9c, 10d, 11c

WH Package



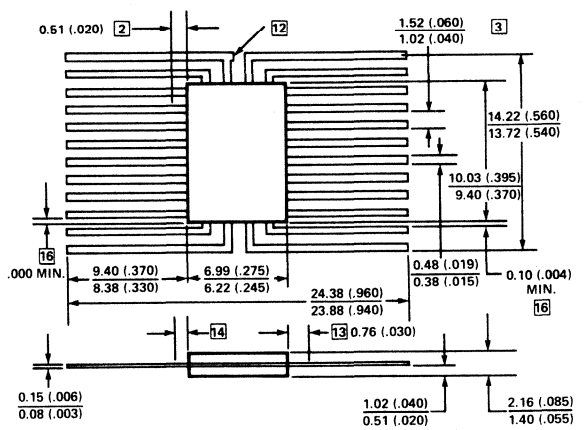
CONSTRUCTION NOTES: 9c, 10d, 11c

WJ Package



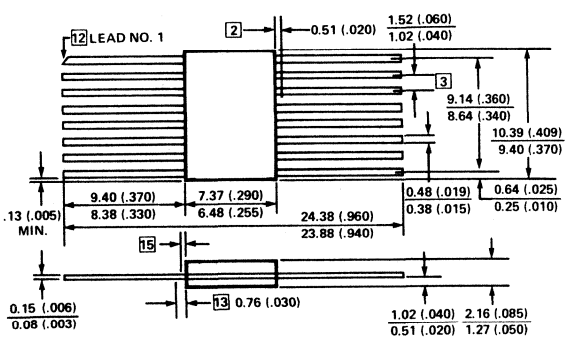
CONSTRUCTION NOTES: 9c, 10d, 11c

WN Package



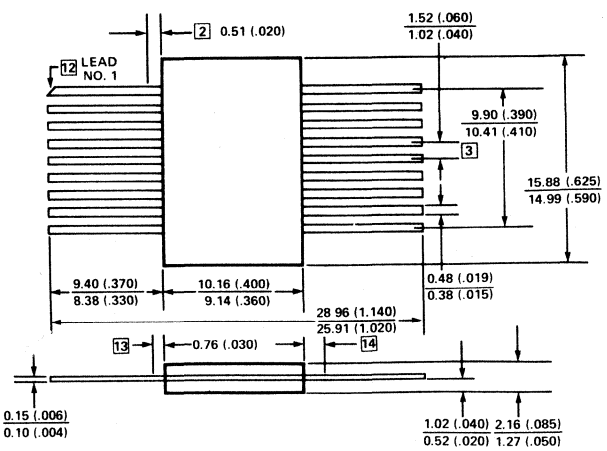
CONSTRUCTION NOTES: 9c, 10d, 11c

RJA Package



RJA CONSTRUCTION NOTES: 9c, 10e, 11e

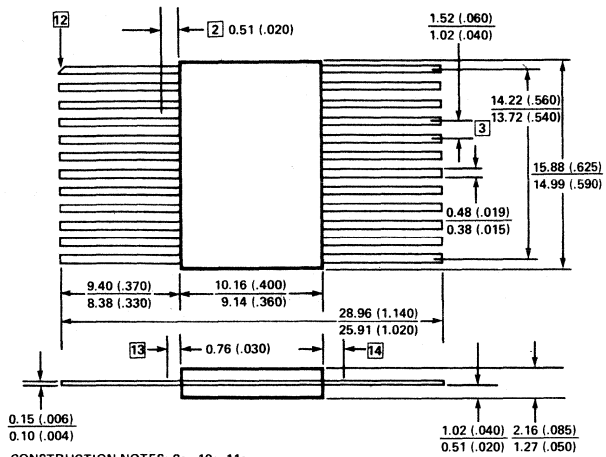
RKA Package



CONSTRUCTION NOTES: 9c, 10e, 11e

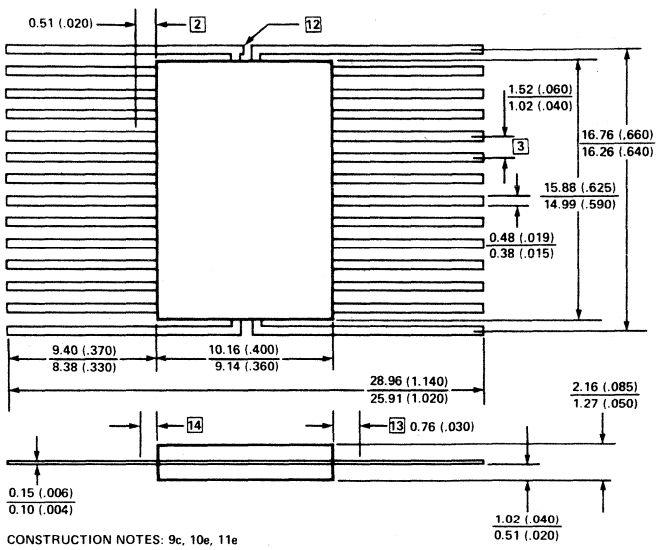
HERMETIC: Flat Packs (cont'd.)

RNA Package



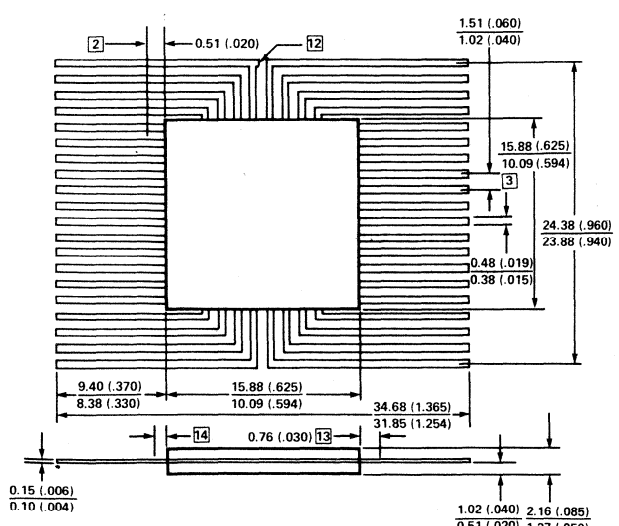
CONSTRUCTION NOTES: 9c, 10e, 11e

RQA Package



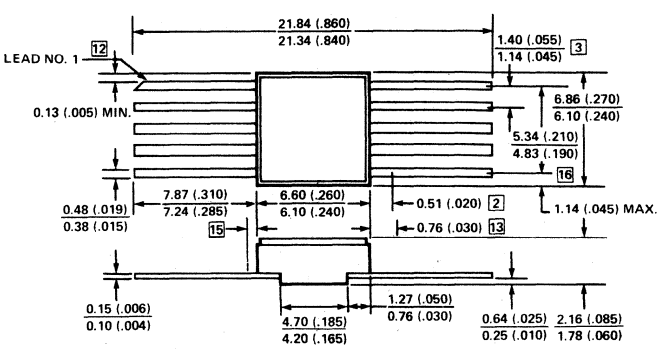
CONSTRUCTION NOTES: 9c, 10e, 11e

RWA Package



CONSTRUCTION NOTES: 9c, 10e, 11e

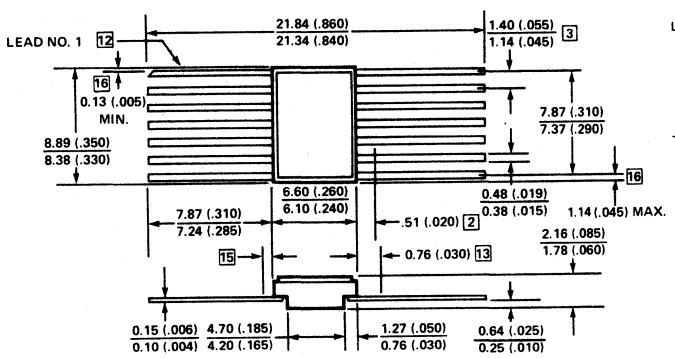
QFA Package



CONSTRUCTION NOTES: 9d, 10f, 11c

HERMETIC: Flat Packs (cont'd.)

QHA Package



CONSTRUCTION NOTES: 9d, 10f, 11c

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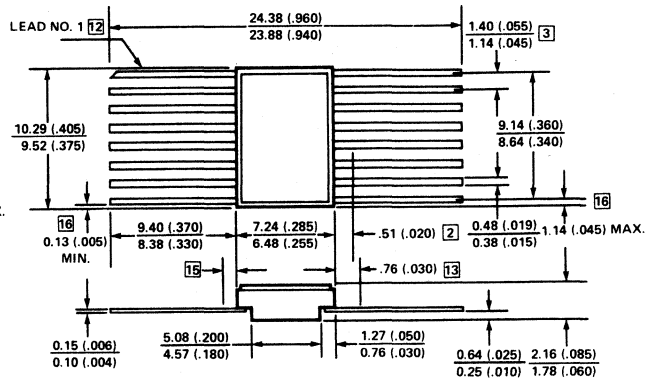

CONSTRUCTION NOTES: 9d, 10f, 11c

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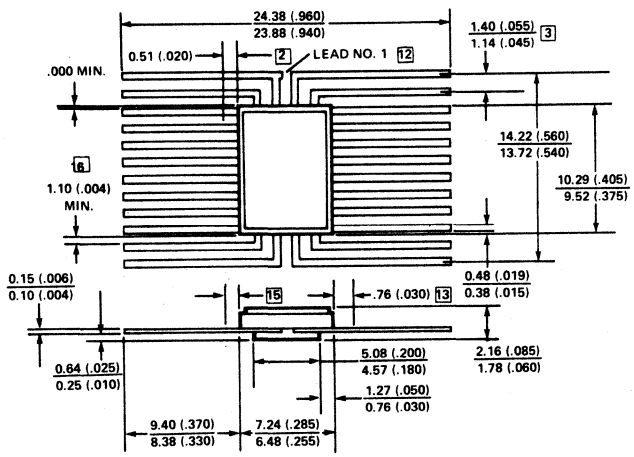


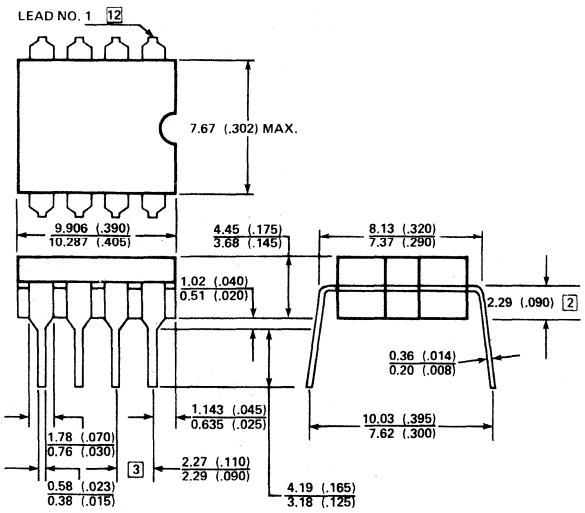
CONSTRUCTION NOTES: 9d, 10f, 11c

GBA Package

Package not yet available.
Scheduled for 1978 release.

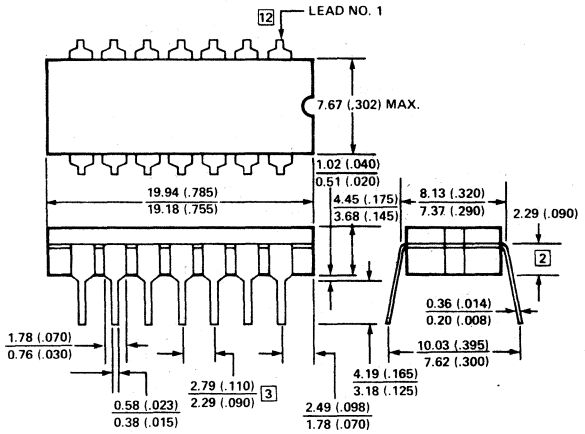
HERMETIC: Cerdip

FE Package



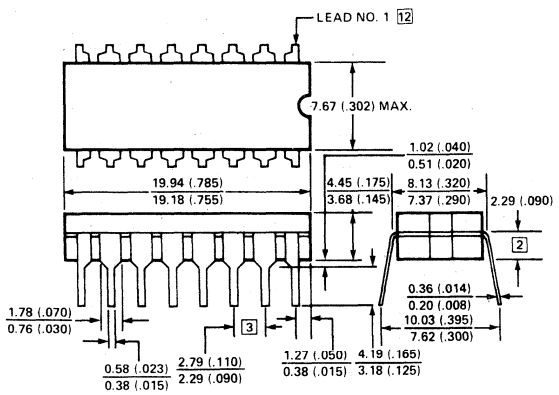
CONSTRUCTION NOTES: 9C, 10D, 11C

FH Package



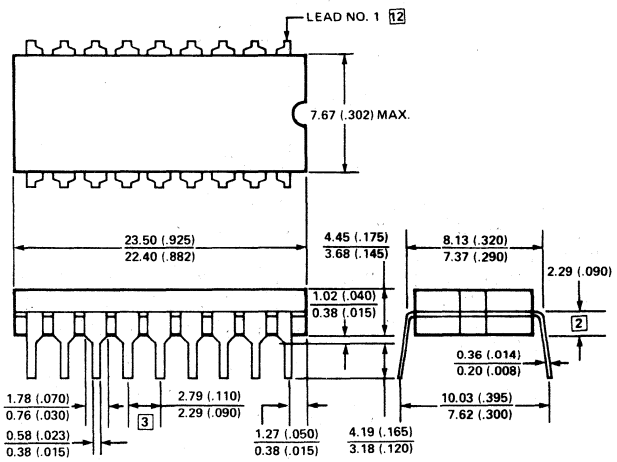
CONSTRUCTION NOTES: 9c, 10d, 11c

FJ Package



CONSTRUCTION NOTES: 9c, 10d, 11c

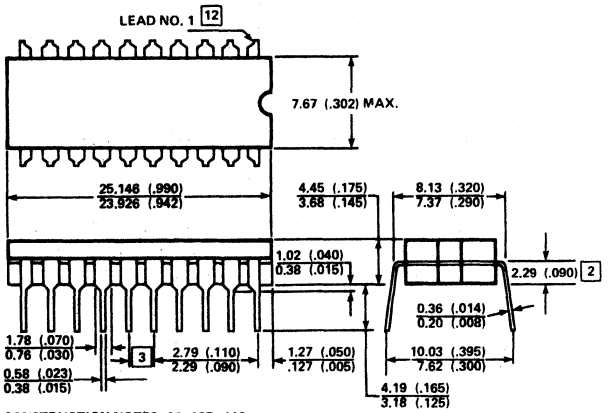
FK Package



CONSTRUCTION NOTES: 9c, 10d, 11c

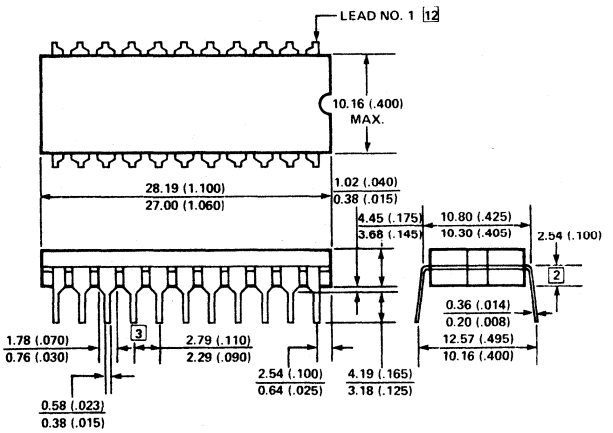
HERMETIC: Cerdip (cont'd.)

FL Package



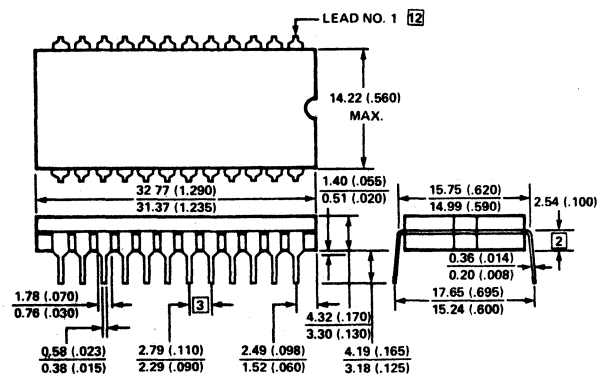
CONSTRUCTION NOTES: 9C, 10D, 11C

FM Package



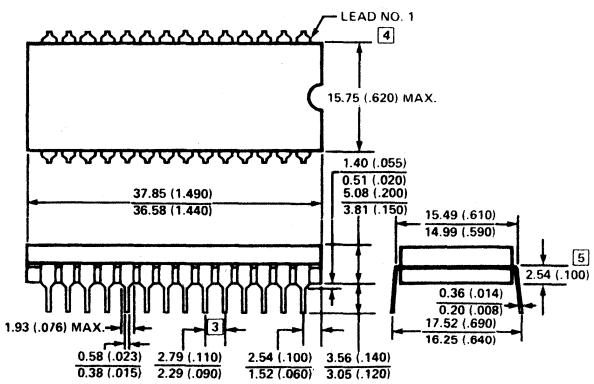
CONSTRUCTION NOTES: 9c, 10d, 11c

FN Package



CONSTRUCTION NOTES: 9c. 10d, 11c

FQ Package



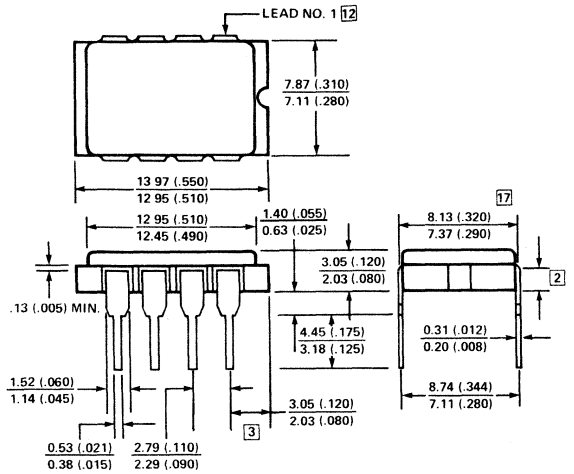
CONSTRUCTIONS NOTES: 9c, 10d, 11c

FW Package

Package not yet available.
Scheduled for 1978 release.

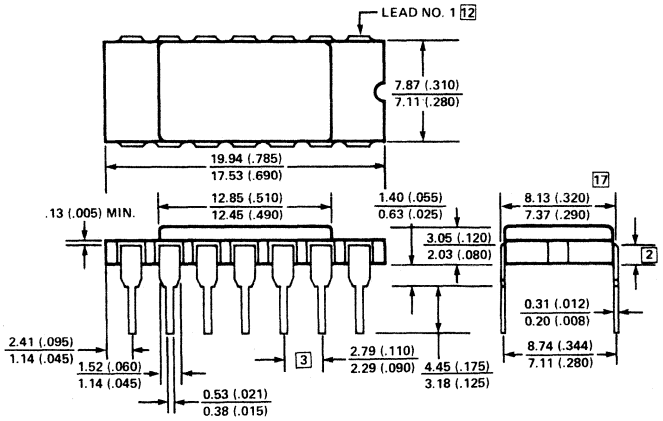
HERMETIC: Laminated Ceramic, Side Brazed Lead

IEA Package



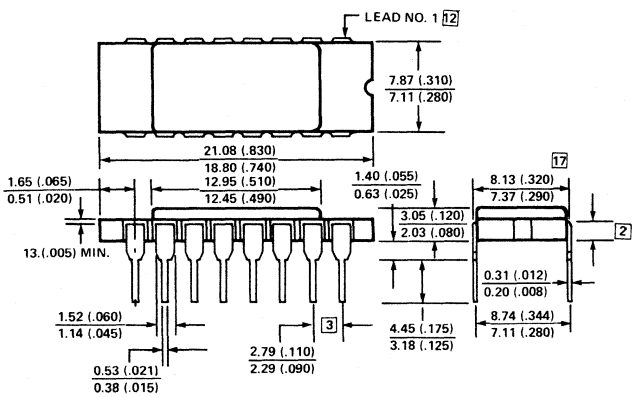
CONSTRUCTION NOTES: 9e, 10f, 11c

IHA Package



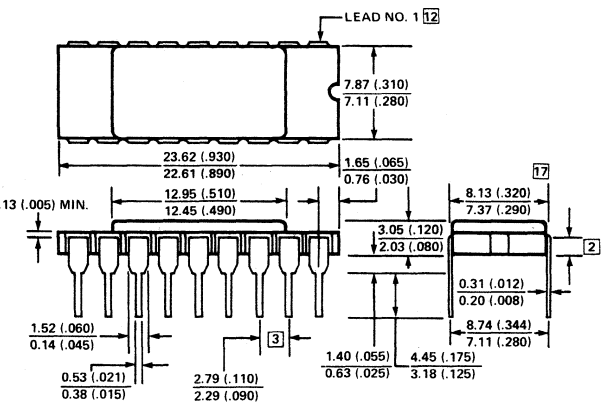
CONSTRUCTION NOTES: 9e, 10f, 11c

IJA Package



CONSTRUCTION NOTES: 9e, 10d,11c

IKA Package



CONSTRUCTION NOTES: 9e, 10f, 11c

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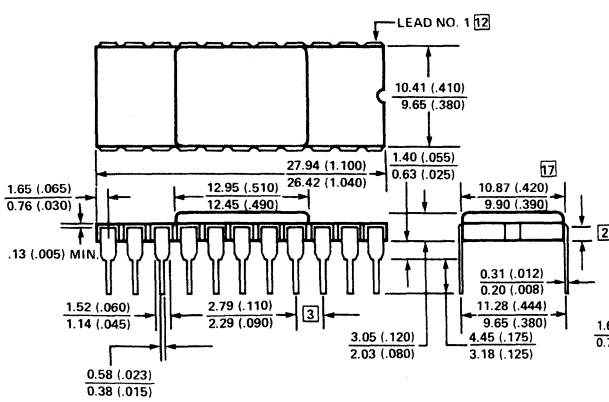
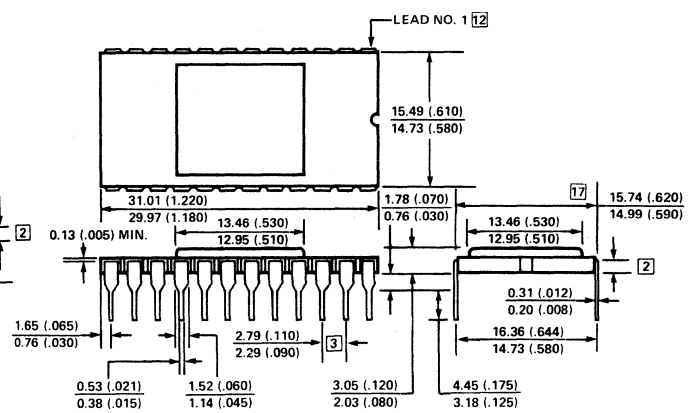


CONSTRUCTION NOTES: 9e, 10f, 11c

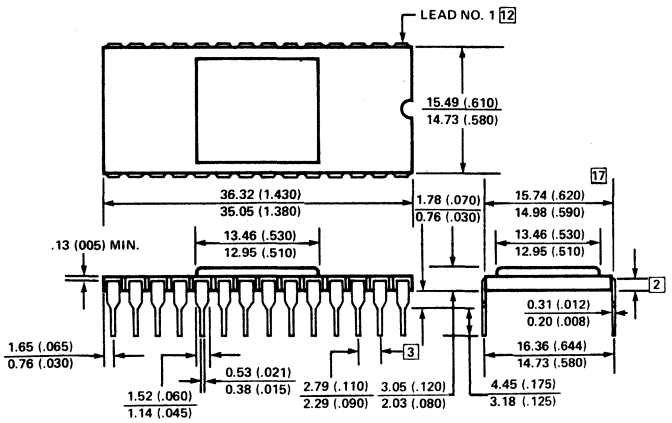
INC Package



CONSTRUCTION NOTES: 9e, 10f, 11f (IND)

HERMETIC: Laminated Ceramic, Side Brazed Lead (cont'd.)

IQA Package



CONSTRUCTION NOTES: 9e, 10f, 11c

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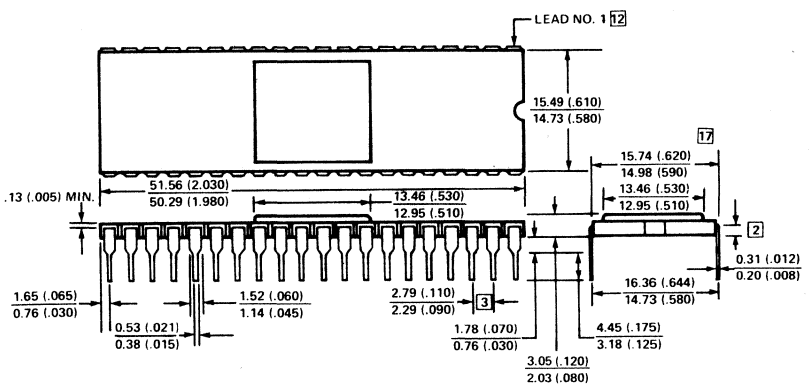
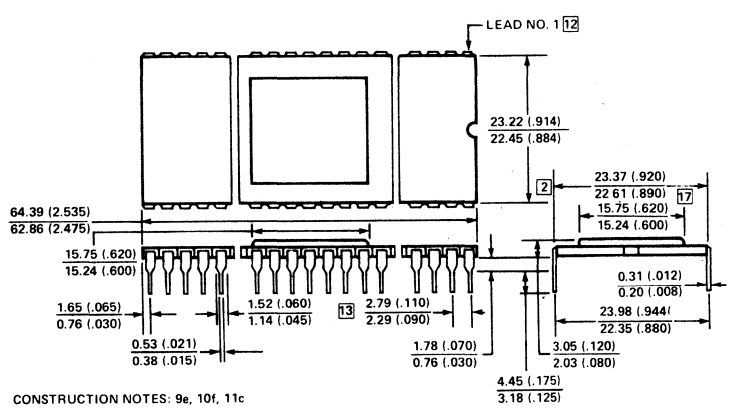


CONSTRUCTION NOTES: 9e, 10f, 11c

IZA Package



CONSTRUCTION NOTES: 9e, 10f, 11c

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